Special reprint
from
AEÜ ARCHIV FÜR ELEKTRONIK UND ÜBERTRAGUNGSTECHNIK
ELECTRONICS AND COMMUNICATION
Band 25 (1971), pp. 477–478

Nonblocking Switching in Integrated PCM Networks

by MASAYUKI TANAKA *

This paper deals with methods of nonblocking switching in integrated PCM networks. At first some known methods are briefly explained and then a new method by means of increased clock frequency is described.

PCM-Durchschaltung ohne innere Blockierung

Der vorliegende Aufsatz behandelt Durchschaltemethoden ohne innere Blockierung in integrierten PCM-Netzen. Zuerst werden einige bereits bekannte Verfahren kurz erläutert. Dann wird eine neue Methode der Durchschaltung ohne innere Blockierung mittels erhöhter innerer Taktfrequenz beschrieben.

1. Some Known Methods for Nonblocking Switching

Recently in various countries the PCM transmission technique is coming more and more into use for short-haul telephone networks, primarily because of its economy.

The transmitted PCM signals are demodulated at the entrance of an exchange and switched in the analogue form by an SDM switching network. If not only the transmission but also the switching is performed by means of TDM, we can save PCM modulators and demodulators in transit exchanges and the cumulative quantizing noise is avoided. Furthermore such a telephone network could be used at the same time as a data network (exact clock synchronization provided). This integrated PCM transmission and switching technique is expected, in the future, to be more economical than the conventional technique for local networks.

This paper deals in particular with the switching problem in integrated PCM networks. In PCM switching it is sometimes impossible, to switch a channel from an incoming PCM highway to a channel of the desired outgoing PCM highway, because no coincident free outgoing channel is available. This is called internal blocking. Up to now, some methods are already known for nonblocking switching, i.e. switching without internal blocking.

These methods presume that synchronizing circuits keep up the bit and frame synchronization between all incoming and outgoing highways within the exchange in question.

A frame of highways can be built up from n time slots. A speech memory can interchange the order of time slots in a frame arbitrarily. As a speech memory we could use, for example, a shift register or a magnetostrictive delay line.

1.1. Speech memory matrix

The most simple method for nonblocking switching uses a speech memory for each pairing of an incoming and an outgoing highway (Fig. 1).

1.2. Modified speech memory matrix according to [1]

In all the speech memories of one row in Fig. 1 the same incoming information is stored simultaneously. Therefore the h_B speech memories per row (according to Fig. 1) can be replaced by *one* memory. Each of its n storage positions is provided with h_B gates. Each gate has access to one of the h_B outgoing highways. Fig. 2 shows this principle.

1.3. Rearrangement according to [2] *and others*

The LCT (Laboratoire Central de Télécommunications) developed the rearrangement method for nonblocking switching (Fig. 3).

This method requires, as is shown in Fig. 3, one input speech memory per incoming highway and furthermore one output speech memory per outgoing highway. A certain time slot (channel) of an incoming highway is connected with a certain time slot of an outgoing highway. These

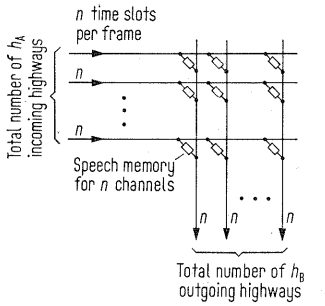

Fig. 1. Speech memory matrix.

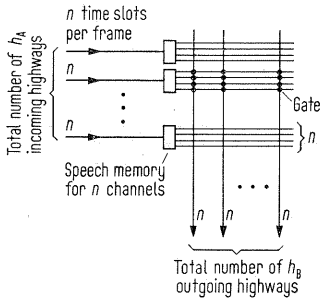

Fig. 2. Modified speech memory matrix.

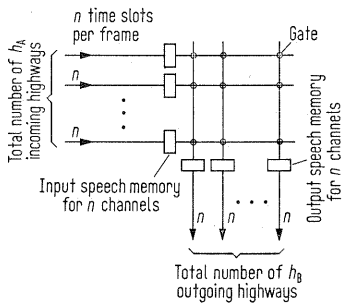

Fig. 3. Rearrangement.

two time slots must not have necessarily the same ordinal number. Between the input and output memory another time slot can be chosen, which is not constantly allocated during the holding time but can be rearranged if further arriving calls require this operation to avoide internal blocking. Output speech memories could be omitted, if the information about channel rearrangements is sent via a separate control channel to the destination exchange. By means of such rearrangement nonblocking switching can be achieved. The control processing unit of the exchange has to carry out the complicated logical operation of rearrangement.

* Dipl.-Ing. M. TANAKA, c/o Institute for Switching and Data Technics, University of Stuttgart, D-7 Stuttgart 1, Breitscheidstrasse 2.

2. The New Method

2.1. Principle

The new nonblocking switching method is based on the idea that the intermediate highway clock frequency f_L is chosen higher than the clock frequency f_H of incoming and outgoing highways. Fig. 4 shows a two-stage PCM switching arrangement, having input and output speech memories.

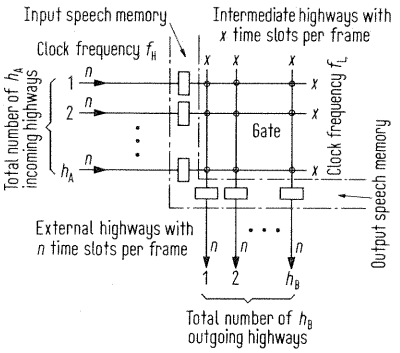

Fig. 4. Increased internal clock frequency.

The structure of this network is similar to that for rearrangement in Fig. 3. The difference is that the clock frequency of the intermediate highways is not identical with that of incoming or outgoing highways, respectively. A frame of highways or of intermediate highways has n or x time slots, respectively. Therefore each speech memory operates in this case with different write-in and read-out clock frequencies.

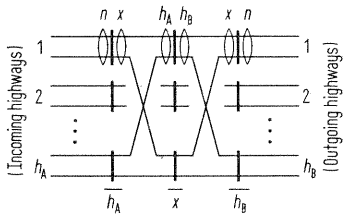

Fig. 5. Equivalent space division switching array.

In Fig. 5 the space division switching array is shown, which is equivalent to the time division switching arrangement in Fig. 4 [3].

From Fig. 5 it can be seen, that the switch is obviously a *nonblocking* one for values of x, where

$$x \geqq 2n - 1 . \tag{1}$$

For SDM systems and PAM local exchanges this method has been published by C. CLOS [5], [6]. For integrated PCM networks, this idea is technically easy to realize. We choose the clock frequency f_L of the intermediate highways so that

$$f_L \geqq \left(2 - \frac{1}{n}\right) f_H . \tag{2}$$

The eq. (2) can be derived as follows: One frame of an intermediate highway has x time slots. One frame of an incoming or outgoing highway has n time slots. Each time slot consists of B bits. The duration per frame must be the same in external and intermediate highways. It holds therefore

$$x B \frac{1}{f_L} = n B \frac{1}{f_H} . \tag{3}$$

From eqs. (1) and (3) we get eq. (2).

The frequency f_L is used as the read-out clock frequency of the input speech memories as well as the write-in clock frequency of the output speech memories. The synchronized clock frequency f_H of incoming and outgoing highways is used as the write-in clock frequency of the input speech memories and as the read-out clock frequencies of the output speech memories. With regard to the circuit technique, it is generally favourable to double the frequency f_H. Therefore we can choose

$$f_L = 2 f_H . \tag{4}$$

More generally we can also use any multiple of f_H, where

$$f_L = (2 + k) f_H, \quad k = 0, 1, 2, \ldots . \tag{5}$$

As compared with the other methods, this method requires special speech memories, but it saves for example the complex logical operation required for rearrangement.

2.2. Reduction of gates

The intermediate clock frequency f_L can furthermore be applied in order to reduce the number of gates in a switching array.

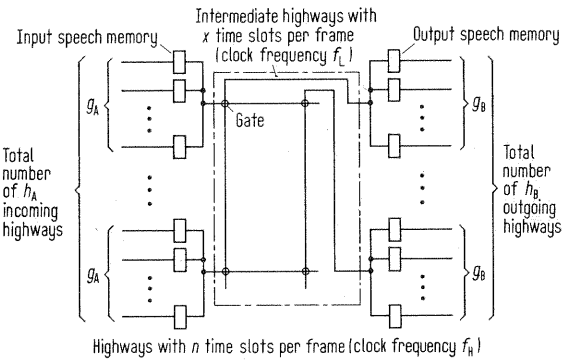

Fig. 6. Reduction of gates.

As is shown in Fig. 6, the h_A incoming or the h_B outgoing highways are subdivided into smaller groups, each having g_A or g_B highways, respectively. As observed from the side of intermediate highways, each of these highway groups can be considered as *one* highway with $g_A n$ or $g_B n$ time slots, respectively. The g_A input or g_B output memories per group are read out or written in with the intermediate clock frequency f_L. Analogously to the principle mentioned above, nonblocking switching is achieved, if

$$x \geqq g_A n + g_B n - 1 . \tag{6}$$

From eq. (6) follows the intermediate clock frequency

$$f_L \geqq \left(g_A + g_B - \frac{1}{n}\right) f_H . \tag{7}$$

For technical reasons, it will be convenient to choose f_L analogously to eq. (5), i.e.

$$f_L = (g_A + g_B + k) f_H , \quad k = 0, 1, 2, 3, \ldots . \tag{8}$$

Arranging the highways in this way and increasing the clock frequency of intermediate highways suitably, the number of switching gates is reduced by the factor $g_A g_B$.

References

[1] INOSE, H. and SAITO, T., Three-stage time-division switching networks by time slot interchange principle. J. Inst. Elect. Commun. Engrs. Japan **49** [1966], 409–417.

[2] LE CORRE, J., Anwendung der Pulscodemodulation in einem integrierten Fernsprechnetz (3. Teil: Vermittlungstechnik). Elekt. Nachrichtenwesen **38** [1963], 27–37.

[3] HUBER, M., On the congestion in TDM systems. 4. ITC London 1964, Doc. 104.

[4] DUERDOTH, W. T., HUGHES, C. J., and BOND, D. J., Trunking systems for PCM exchanges. Proc. Instn. Elect. Engrs. **114** [1967], 1623–1629.

[5] CLOS, C., A study of nonblocking switching networks. Bell Syst. tech. J. **32** [1953], 406–424.

[6] CLOS, C., Number of gates required for time division switching. 5. ITC New York 1967, Preprints, 236–237.