DESIGN OF ECONOMIC PCM-ARRAYS WITH A PRESCRIBED GRADE OF SERVICE

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ABSTRACT

This paper deals with the design of economically structured PCM switching arrays for traffic distribution. The presented switching arrays are symmetrically structured, and have one up to six stages and use different combinations of time-stages T and space-stages S, respectively. It is shown how such arrays can be designed for a required grade of service having a prescribed number of terminations and a prescribed carried traffic per time-slot. Their relative costs per termination equal to that per time-slot are calculated. These are costs for the gates and costs for memory bits, i.e. speech memories and all control memories.

All presented PCM switching arrays are mapped into the corresponding space division multiplex (SDM) arrays. This allows a simple comparison with SDM link systems and an easy calculation of the Point-to-Point Loss.

The paper concludes comparing the traffic behaviour and costs of the various PCM switching arrays.
Finally new "PCM CHARTS" are developed as useful means for the design of economic PCM switching arrays.

A second paper of this congress / 14 / compares traffic equivalent PCM and SDM switching arrays, resp., with regard to their economic design, their traffic behaviour and their costs per termination

1. INTRODUCTION

Due to the decreasing costs of digital techniques, PCM switching becomes more and more an economic alternative to space division multiplex switching. Therefore, the aim of this paper is to give a systematic survey of suitable switching arrays using different types and sequences of stages within the array, namely time-stages T and space-stages S.

2. ELEMENTS OF A PCM SWITCHING ARRAY

2.1 The Space Stage

A space stage is composed by space switches (SS) consisting of matrices for time-multiplex lines (ML). Each switching matrix has h incoming and j outgoing MLs, having M time-slots each. The number of outgoing MLs may be greater or less than the number of incoming ones.

The space-stage only allows the coincident switching of time-slots (TS) from each incoming ML to each outgoing ML. Switching is performed by logical gates, forming the crosspoints of the matrices. They are controlled by control memories. The cheapest realization is achieved if a control memory controls the gates of an incoming ML, if $h < j$. A control memory has as many storage places as there are TS on the ML; each storage place needs $\lceil \mathrm{ld}\, j \rceil$ bits, where $\lceil\ \rceil$ means the next greater integer value.
To simplify the figures, a short notation for the SS is introduced as shown in Fig.1 below.

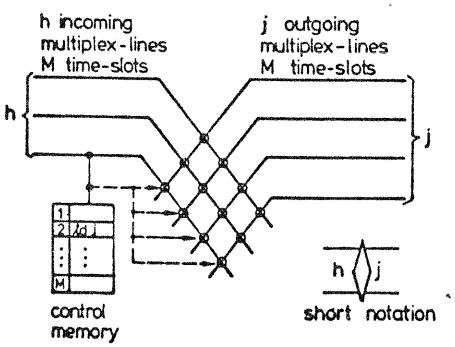


Fig. 1: The Space Switch

2.2 The Time Stage

A time-stage is composed of a number of time-slot interchanges (TSI), consisting of speech memories and control memories.
A TSI allows the switching of each of the M time-slots of the incoming MLs to each of the M^* time-slots of the outgoing MLs. M^* may be greater or less than M. Time-slot interchanging is performed by the speech memory and the respective control memory. The control memory controls either writing into the speech memory or reading out from it. This function of random addressing is depicted in Fig.2 by a double arrow. Reading or writing on the other side of the speech memory is done cyclically according to the time-slot counter.
The cheapest realization is achieved if the control memory controls that side of the speech memory where the number of time-slots is greater.
To simplify the figures a short notation for the TSIs is introduced, as shown in Fig.2 below.

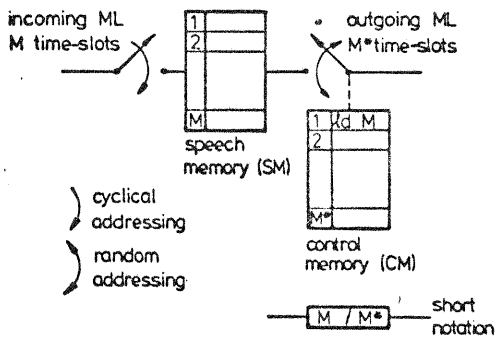


Fig. 2: The Time-Slot Interchange

3. SWITCHING MODE AND ARRAY STRUCTURE

PCM switching is always four-wire equivalent, i.e. a PCM Highway consists always of two multiplex-lines (ML), one for each speech direction. Therefore, two time-slots, one in each multiplex-line, have to be provided for one speech connection.
The structure of a PCM switching array depends on the decision which of the two following switching modes should be applied:
- Separated Switching, or
- Combined Switching.

3.1 Separated Switching

Separated switching (SSW) means that only connections from incoming Highways to outgoing Highways ("from left to right") can be established. This leads to an array structure where two identical, but separated arrays for the two speech directions have to be provided, see Fig.3.

On the left hand side of the two identical arrays all incoming Highways, carrying only one-way traffic, terminate, each speech direction (ML) on an array of its own. The same holds for the outgoing Highways terminating on the right hand side. If the two paths for the two speech directions in both arrays are chosen identically, it is sufficient to provide control memories only for one network; the other one can be controlled by these memories, too.
This corresponds exactly to the unidirectional operation mode of many SDM link systems for traffic distribution.

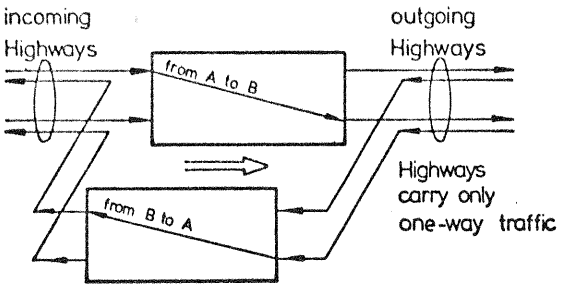


Fig. 3: Separated Switching Mode

3.2 Combined Switching

Combined switching (CSW) means that connections between all Highways connected to the (one and only) array can be established; the Highways may carry two-way traffic as well as one-way traffic.
The incoming speech directions of all Highways terminate on the left hand side of the array, the outgoing speech directions on the right hand side, see Fig.4. For each speech connection one has therefore to establish in any case two paths through the same combined switching array.

The manner how these two paths are allocated within the array has a remarkable influence on the costs. Suitable path allocation principles will be presented in the following chapter.

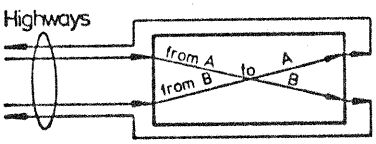


Fig. 4: Combined Switching Mode

3.3 Path Allocation Principles for Combined Switching

Combined switching allows various path allocation principles to be applied in order to save control memories for gates as well as for speech memories. If the two paths of one speech connection (from A→B and B→A) are switched symmetrically to the median vertical line, the control memories on the left hand side can control the elements on the right hand side, too.
It is necessary for all path allocation principles to have symmetrically structured PCM switching arrays, i.e. the types and the numbers of stages have to be identical on both sides of the median vertical line.
This prerequisite holds for all investigations and switching arrays discussed in the following.
Two different principles are possible,
- the symmetrical path allocation, and
- the quasi symmetrical path allocation.

The implementation of these principles varies, depending on the type of the first and the last stage of the switching array (T or S-stage).

3.3.1 Path Allocation within T..T Arrays

Symmetrical path allocation means that additionally to the symmetrical switching, for both paths of one connection likewise numbered time-slots are used between the first and the last T-Stage. Symmetrical path allocation has the restriction that connections between speech paths within the same Highway cannot be established.
Quasi symmetrical path allocation, however, allows such connections.
For this purpose the two speech paths of one connection use an even/odd time-slot relation instead of likewise numbered TS /22/.
Both allocation principles allow to save half of the control memories, if the number of stages is even; if not, control memories can be saved for all stages except for the middle one.

3.3.2 Path Allocation within S..S Arrays

Symmetrical path allocation means that the two speech directions of one connection lead symmetrically over the same time-slot interchange in the middle T-Stage. Quasi symmetrical path allocation differs, concerning the paths in the middle T-Stage. Now, these two paths do not lead through the same TSI, instead they lead through two related TSIs, which can be controlled by one control memory. Thus, half of the control memories of the middle stage can be saved, too.

For switching within the STSTS and STSSTS array, having no middle T-Stage, quasi symmetrical path allocation is applied between the two T-stages as described above.

4. INVESTIGATED PCM ARRAYS

With T-Stages and S-Stages, a great variety of PCM switching arrays can be designed. Among all these arrays only few are symmetrically structured, i.e. the types and numbers of stages on the left and right hand side of the median vertial line are identical. Only these symmetrical arrays allow savings in control memories if a path allocation principle for combined switching is implemented. Arrays consisting only of space-stages, will not be regarded as they have a very poor traffic behaviour.
Furthermore, systems with consecutive time-stages are not considered, because they do not improve the traffic efficiency.
Thus, the one to six-stage arrays described in the following remain the only to fulfill the prerequisites.
For each array design formulae are given which are derived in a related paper of this ITC /14/. These formulae allow the building of economic PCM switching arrays.
Furthermore, the mapping of PCM arrays into equivalent SDM arrays is presented using some examples. Mapping is advantageous in order to calculate the grade of service of the PCM switching arrays.
Like in SDM arrays also in PCM arrays an expansion in the first stage is possible to obtain a desired probability of loss. The realization of this expansion will be discussed in the following chapter.

4.1 Expansion of PCM Switching Arrays

It is known from SDM arrays that the loss probability is influenced by an expansion in the first stage and a corresponding concentration in the last stage; all multiples in the intermediate stages switch 1:1. This expansion leads to different realizations in PCM switching arrays depending on the type of the first and the last stage (S or T).
If both are T-stages, expansion can be performed by increasing the number of time-slots within the PCM array. This is, however, only possible up to a maximum clock frequency which is assumed to be about 8 MHZ, for the time being. This clock frequency allows one ML to carry 120/128 TS if the voice samples are transmitted in serial and 960/1024 TS if parallel transmitting is applied.
If the first and the last stage are S-Stages, expansion means to increase the number of outgoing MLs per SS in the first stage (cf. Fig.1).

This is exactly the same method as in SDM arrays.

The following assumptions hold for all presented PCM arrays:
- the PCM switching arrays are symmetrically structured and have as many incoming MLs as outgoing ones,
- expansion is always performed in the first stage, concentration in the last stage; all intermediate stages switch 1:1,
- the maximum clock frequency for switching is assumed to be 8.192 MHZ.

From this it follows:
- serial transmitting allows one ML to carry 120/128 TS,
- parallel transmitting to carry 960/1024 TS.

4.2 One Stage Switching Array: The T-Stage

The T-Stage is only one time-slot interchange, consisting of a speech memory and a control memory (cf. Fig.5). To allow switching between more than one PCM Highway a certain number of them has to be multiplexed before switching into one ML; a maximum of 960/1024 TS per ML can be achieved; this corresponds to 32 PCM 30/32 systems.
The T-Stage is strictly nonblocking.
As it is known, this way of "T-Stage switching" is economic, at least up to 960/1024 terminations. If more than 960/1024 terminations (or TS, resp.) have to be switched the costs increase remarkably. A correct cost comparison with multistage PCM arrays seems to be very difficult and therefore has not been performed.

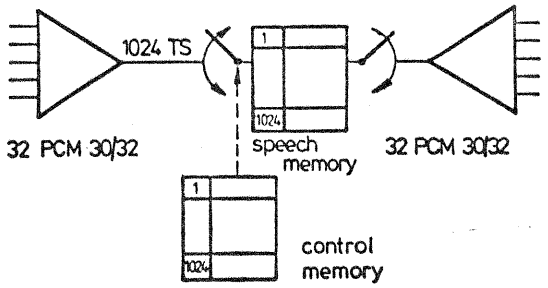


Fig. 5: The T - Stage

4.3 Three Stage Switching Arrays

4.3.1 The STS Array

Fig. 6a shows the PCM array and Fig.6b its mapped array. The mapping rules are as follows:

One time-slot interchange of the T-Stage becomes one multiple with M inlets and M outlets; the MLs on the left and right hand side of the TSI carry the same number of time-slots.

A space switch becomes a column of M multiples, each having h_1 inlets and j_1 outlets; j_1 has to be chosen such that the desired probability of loss is achieved. An expansion factor β is introduced for which holds $\beta = j_1/h_1$.

The mapping of the incoming and outgoing MLs, connected to the first and last stage, resp., is such that the M time-slots of each ML terminate at M different multiples.

From this it follows that different marking methods can be applied:
- Point-to-Point marking, PPL calculation /9/
- Point-to-Point marking with multiple marking attempts, PPLM calculation /13/
- Point-to-Group marking, CLIGS calculation /1,2/.

Design Formula:

$$h_1 = j_3 = HW \qquad j_1 = h_3 = \beta \cdot h_1$$

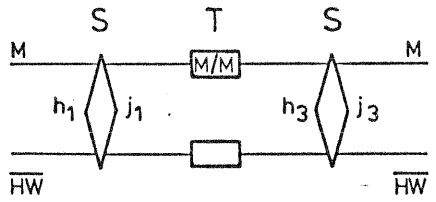


Fig. 6a: The STS Array

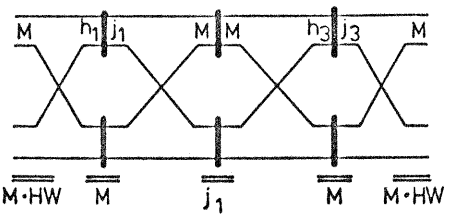


Fig. 6b: The Mapped STS Array

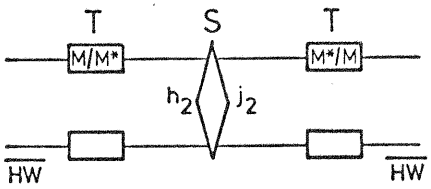
The latter two marking methods are possible, as one trunk-group, i.e. one PCM multiplex-line can be reached via M different multiples of the last stage. It is well known that Point-to-Group marking leads to the lowest probability of loss, but requires the maximum time for path searching.
It is possible to make this array strictly non-blocking, if j_1 is chosen to $(2h_1-1)$ /5/.

4.3.2 The TST Array

Because of the TSIs in the first and the last stage, Point-to-Point selection is the only possible selection mode, see Chapter 4.4. Figure 7 shows the TST array. Expansion is performed by increasing the number of internal time-slots M^*. If M^* is chosen to $M^* = 2M-1$ the array becomes strictly nonblocking /5/.
The mapping of a T..T array will be discussed in the following chapter. Instead of the whole mapped array, the short notation of the equivalent SDM array is shown in Fig.7.

Design Formula:

$$h_2 = j_2 = HW \qquad M^* = \beta \cdot M$$



Short Notation:

$$\frac{M \mid M^*}{h_2} \quad \frac{h_2 \mid j_2}{M^*} \quad \frac{M^* \mid M}{j_2}$$

Fig. 7: The TST Array

4.4 The Four Stage Switching Array: TSST

The four stage TSST array, see Fig. 8a, is the first to allow forming of blocks. Fig. 8b shows the mapped array. The same mapping rules hold, as above. One TSI of the first and last stage, resp., becomes one multiple with M inlets and M^* outlets or vice versa; normally M^* is greater than M because of the necessary expansion.

A space switch again becomes a column of M^* multiples with h_2 inlets and j_2 outlets each, if e.g. the second stage is regarded.

The blocks which are formed between stages 1 and 2 as well as 3 and 4 of the PCM array appear also as blocks within the mapped array. The incoming and outgoing MLs terminate at one TSI; from this it follows that the equivalent trunk group in the mapped array terminates also on only one multiple. Therefore, only Point-to-Point selection is possible, as one outgoing ML can only be reached via one multiple of the last stage.
The dashed lines between stages 2 and 3 have to be provided if combined switching (cf. Chapter 3.2) is applied. This is necessary for this switching mode only, as thus the number of possible connections remains constant between all blocks on the left and the right hand side, including likewise numbered blocks (one connection requires two paths).

The design formula follows in this case from the prerequisite that all intermediate stages switch 1:1 and the number of incoming and outgoing MLs is the same, namely HW.

This four stage array can easily be extended from a smaller initial size to the planned final size, if the principle of constant block size is applied /9,12/. In this case the SS have a priori the final size. For intermediate sizes of the 4-stage array with less blocks more than one ML leads from a block on the left hand side to a block on the right hand side.

Design Formula:

$$h_2 = j_2 = h_3 = j_3 = \sqrt{HW} \qquad M^* = \beta \cdot M$$

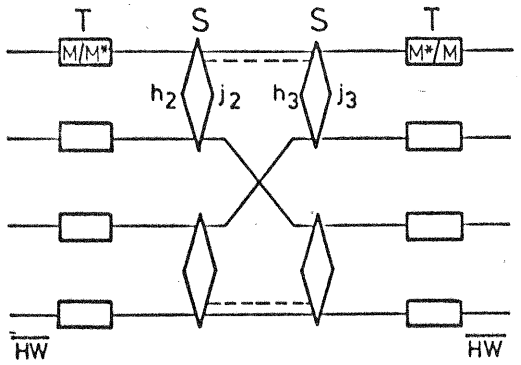


Fig. 8a: The TSST Array

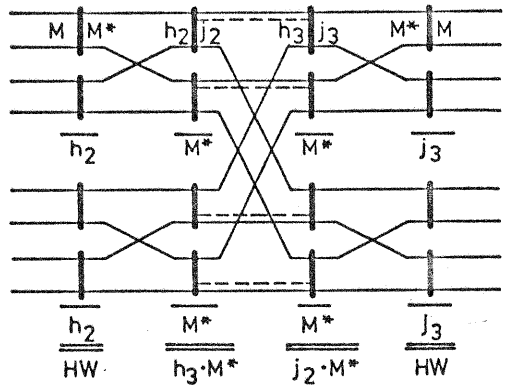


Fig. 8b: The Mapped TSST Array

4.5 Five Stage Switching Arrays

There are four five-stage arrays that fulfill the requirement of being symmetrical: the TSSST, the SSTSS, the STSTS and the TSTST array.

The last one, however, does not increase the traffic capacity compared with the four stage array.

4.5.1 The TSSST Array

Fig. 9a shows the PCM array and Fig. 9b the mapped equivalent SDM array. The same design rules as discussed above are applied. Blocks are formed between stages 1 and 2 as well as between stages 4 and 5. The appearance of the blocks in the equivalent SDM array is the same as in Chapter 4.4. The presentation of the middle stage is such, that multiples, representing the same time-slot number, are adjacent.
The structure of the presented mapped SDM array holds for all five-stage arrays. There are only differences in the number of inlets and outlets of the multiples as well as in the mapping of the incoming and outgoing MLs.

The other two five-stage arrays (Fig. 10a, 11) have S-Stages in the first and the last stage. Therefore, in the mapped SDM array the incoming and outgoing MLs of stage one and five, resp., terminate at a column of M multiples (cf. Fig. 10b, 11).

The TSSST array can be extended in the same way like the four-stage array if the space switches are designed for the final size.

Design Formula:

$$h_2 = j_2 = h_3 = j_3 = h_4 = j_4 = \sqrt{HW}$$

$$M^* = \beta \cdot M$$

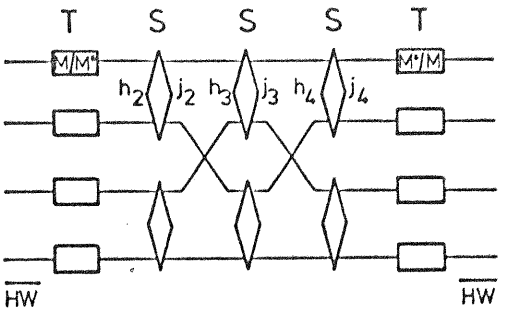


Fig. 9a: The TSSST Array

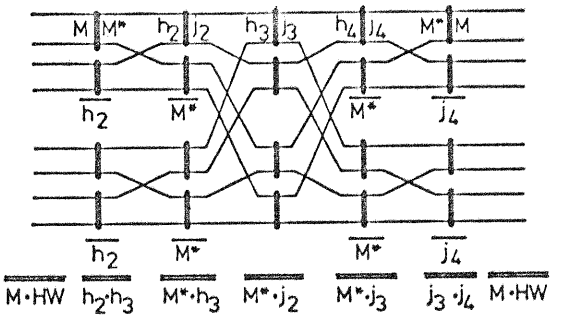


Fig. 9b: The Mapped TSSST Array

4.5.2 The SSTSS Array

This array allows forming of blocks between stages 2, 3 and 4 (cf. Fig.10a). Expansion in the first stage is performed by increasing the number of MLs: $j_1 = \beta \cdot h_1$.
If, in contradiction to the prerequisites, also the second stage is expanded, the array can become strictly non-blocking (the values are: $j_1 = 2h_1 - 1$, $j_2 = 2h_2 - 1$) /5/.
The array allows very good extension strategies if the blocks in the middle stages and the space switches are designed for the final size. It is even possible, again in contradiction to the prerequisites, to make only the internal block strictly non-blocking. Then this block could have a control unit of its own and path searching could be simplified because the whole array could be regarded like a three-stage array /19/. Fig.10a shows the PCM array and Fig.10b the equivalent SDM array.

Design Formula:

$$h_1 = j_2 = h_2 = j_4 = h_4 = j_5 = \sqrt{HW} \qquad j_1 = h_5 = \beta \cdot h_1$$

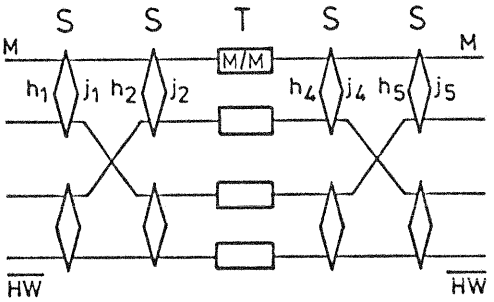


Fig. 10a: The SSTSS Array

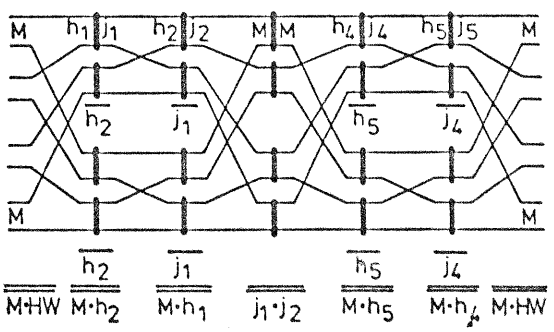


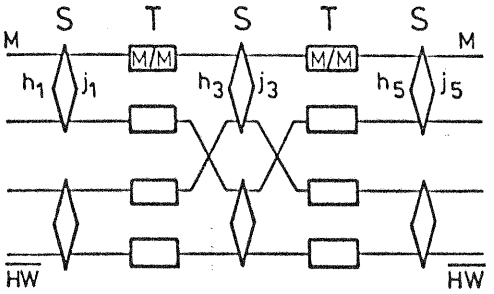
Fig. 10b: The Mapped SSTSS Array

4.5.3 The STSTS Array

Fig.11 shows the STSTS array and the short notation of the mapped array. Again blocks are formed between stages 1 and 2 as well as 4 and 5.
The extension strategy of this array is the same as above. Quasi symmetrical path allocation is applied between the two T-Stages, if combined switching is provided.

Design Formula:

$$h_1 = h_3 = j_3 = j_5 = \sqrt{HW} \qquad j_1 = h_5 = \beta \cdot h_1$$



Short Notation:

$h_1 \mid j_1$	$M \mid M$	$h_3 \mid j_3$	$M \mid M$	$h_5 \mid j_5$
M	j_1		h_5	M
$M \cdot h_3$	$j_1 \cdot h_3$	$M \cdot j_1$	$h_5 \cdot j_3$	$M \cdot j_3$

Fig. 11: The STSTS Array

4.6 Six Stage PCM Switching Arrays

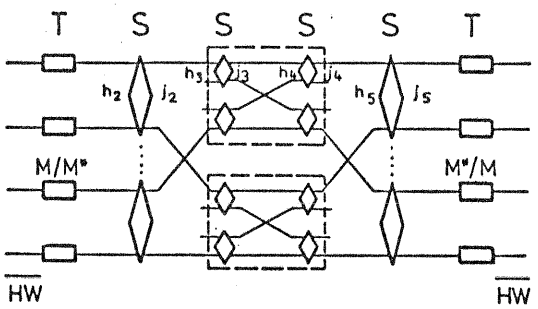
4.6.1 The TSSSST Array

There are different possibilities for the structure of this type of array. The presented array has the minimum amount of costs and can easily be extended, if the blocks and space switches are designed for the final size. As the first and the last stage is a T-stage only Point-to-Point selection is possible. Fig.12 shows the PCM array, the short notation of the mapped array and the design formula.

Design Formula:

$$h_2 = j_2 = h_3 = j_3 = h_4 = j_4 = h_5 = j_5 = \sqrt[3]{HW}$$

$$M^* = \beta \cdot M$$



Short Notation:

$M \mid M^*$	$h_2 \mid j_2$	$h_3 \mid j_3$	$h_4 \mid j_4$	$h_5 \mid j_5$	$M^* \mid M$
h_2	M^*			M^*	j_5
$h_3 \cdot h_2$	$h_3 \cdot M^*$	$j_2 \cdot M^*$	$h_5 \cdot M^*$	$j_4 \cdot M^*$	$j_4 \cdot j_5$
HW	$h_4 \cdot h_3 \cdot M^*$	$h_4 \cdot j_2 \cdot M^*$	$j_3 \cdot h_5 \cdot M^*$	$j_3 \cdot j_4 \cdot M^*$	HW

Fig. 12: The TSSSST Array

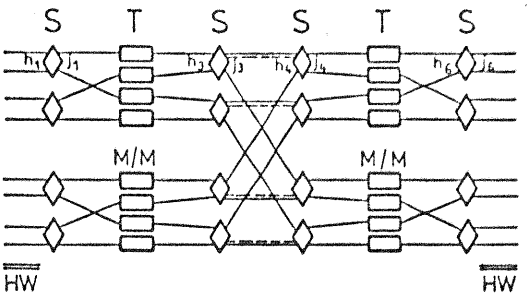
4.6.2 The STSSTS Array

Blocks can be formed within the first three and the last three stages (cf. Fig.13). Interconnection between the blocks is performed between stages 3 and 4.
The dashed MLs are necessary for combined switching in order to have the same number of possible connections from each block on the left hand side to each block on the right hand side. Between the two T-stages quasi symmetrical path allocation is applied. The extension strategies for this array are the same as discussed above

Design Formula:

$$h_1 = h_3 = j_3 = h_4 = j_4 = j_6 = \sqrt[3]{HW}$$

$$j_1 = h_6 = \beta \cdot h_1$$



Short Notation:

$h_1 \mid j_1$	$M \mid M$	$h_3 \mid j_3$	$h_4 \mid j_4$	$M \mid M$	$h_6 \mid j_6$
M	j_1			h_6	M
$M \cdot h_3$	$j_1 \cdot h_3$	$M \cdot j_1$	$M \cdot h_6$	$h_6 \cdot j_4$	$M \cdot j_4$
$M \cdot h_3 \cdot h_4$	$j_1 \cdot h_3 \cdot h_4$	$M \cdot j_1 \cdot h_4$	$M \cdot h_6 \cdot j_3$	$h_6 \cdot j_4 \cdot j_3$	$M \cdot j_4 \cdot j_3$

Fig. 13: The STSSTS Array

Interleaved wiring /9,16/ which can be used in SDM switching arrays to improve the grade of service is not possible because the considered PCM systems must be symmetrically structured.
Therefore, the PPL method, which allows the calculation of the Point-to-Point loss, was slightly modified for 5- and 6-stage arrays /16/.

Simulations show that the PPL method offers good results for separated switching as well as for combined switching.

5. IMPORTANT FEATURES OF PCM SWITCHING ARRAYS

When the choice of a structure and the number of Highways to be connected to has been made, the number of MLs terminating in one matrix of block is the only variable remaining free. This variable, however, is responsible for the number of blocks and has a great influence on the costs of the whole array.
In the related paper /14/ it is presented how this variable has to be chosen to obtain minimum costs for the whole array. The design formulae that have been given for each array result from this optimal choice.

For the following comparisons concerning the quality of the PCM switching arrays, only Point-to-Point selection will be considered.

5.1 Calculation of the Costs of a PCM Switching Array

The costs for a PCM array are the sum of the costs for all logical gates in the crosspoints of the space switches, the costs for the control memories of the SSs and the costs for the TSIs, i.e. costs for the speech memories and the respective control memories. The costs for the control memories depend on whether a path allocation principle is applied or not. The formulae for the calculation of the costs are given in the annex.
For all formulae it is assumed that quasi symmetrical path allocation for T..T arrays as well as for S..S arrays is applied.
To obtain a uniform manner of presentation a cost ratio (CR) is introduced which is the ratio between the costs for a gate and the costs for a storage bit.

The additional hardware elements, necessary to control the function of the memories and gates can be taken into account by choosing an appropriate value for CR.

For the costs it holds:

COSTS=CR * number of gates + number of bits
(bits for speech and all control memories)

To summarize the formulae:
The parameters that influence the costs of the PCM switching array are:
- the type of the array
- the number of Highways to be connected to
- the number of TS per Highway
- combined or separated switching
- serial or parallel switching
- the cost ratio CR

Fig. 14 shows a comparison among the costs of the presented arrays. The number of TS per ML is 30, a cost ratio of 5 is assumed and combined switching is performed in serial.

All arrays are expanded such that for a prescribed carried traffic per TS Y/TS = 0.8 Erl. the Point-to-Point loss is $B_{pp} \sim 0.1$ %.

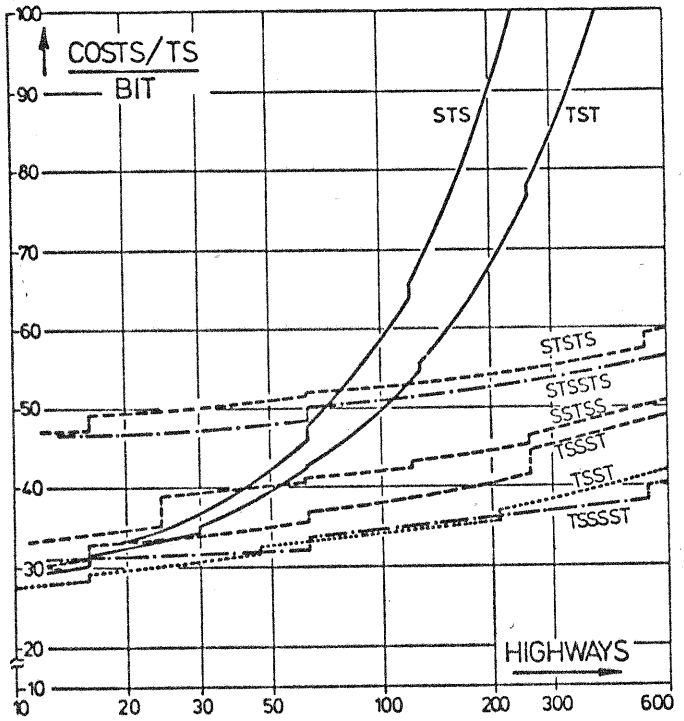


Fig. 14: Relative Costs per Time-Slot for Different Highway Numbers, Y/N = 0.8 Erl., B_{pp} = 0.1%, CR = 5, M = 30, Combined, Serial Switching

The curves show that both three-stage arrays become rather expensive for increasing Highway numbers. This comes from the large space switches heaving HW^2 gates. The discontinuities in these curves as well as in the other ones follow from the control bits for addressing the space switches. Whenever the dual coded address requires an additional bit such a discontinuity appears.

Among the other multistage arrays these arrays are the cheapest which have a T-Stage as the first and the last one; those with a S-Stage are more expensive.
There are two reasons for the T..T arrays to be less expensive:

- The TSIs in the first and last stage are in their mapped form SDM multiples, having a size of about 30|40. Large multiples like these in the first stage favour the grade of service.
- Expansion is performed by increasing the number of internal TS which is the cheapest expansion mode.

These reasons do not hold for the S..S arrays.
The economic multiple size in the first stage is relatively small. Therefore, often a remarkable expansion is necessary, in order to obtain the prescribed probability of loss; this increases the costs.

To summarize the results of Fig.14:
For the above prerequisites it holds that T...T arrays are the most economic ones, having costs of 30...50 bits/TS (per termination, resp.).

5.2 Influence of the Number of TS per ML on the Loss Probability and the Costs

The relative costs for a PCM switching array can be reduced if, having a constant total number of terminations, the number of TS within one ML is increased and consequently the number of MLs decreased. The savings in costs lie in the logical gates, as their costs generally remain constant whether they have to switch 30 or 120 TS. The principle of realization is to multiplex several MLs with e.g. 30 TS each, into one ML with e.g. 120 TS.
Fig. 15 shows, as an example this "multiplexing before switching" for the two types of three-stage arrays.

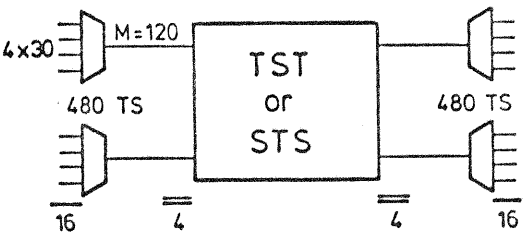


Fig. 15a: Multiplexing Before Switching

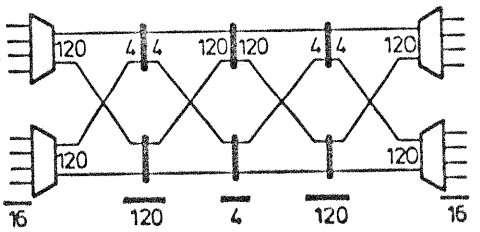


Fig. 15b: The Mapped TST Array

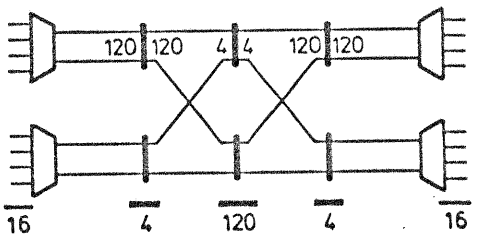


Fig. 15c: The Mapped STS Array

Fig. 15 b,c show the mapped SDM arrays of the TST and STS PCM array. The increased number of TS has quite different effects on the two array types.
For the mapped TST array it holds that the multiples in the first and the last stage become greater, from 30|30 to 120|120. This decreases the loss probability, Fig.16 shows this effect.
Curve 1 holds for the array with M=30 TS per ML, curve 3 for M=120 TS per ML. Additionally, curve 2 shows the traffic behaviour for M=60 TS/ML.
If the relative costs are calculated, the following values hold (CR=5) for the TST array:

- For M=30 TS/ML the relative costs are 28 bits/TS,
- for M=120 TS/ML the relative costs are 25 bits/TS.

It should be noticed that the probability of loss as well as the costs/TS decrease if the number of TS/ML is increased from 30 to 120 TS/ML.

The effect is different for the STS array. For 120 TS/ML the multiples in the first stage become smaller, see Fig. 15c. The loss probability increases; compare curves 4 and 6. However, the costs still decrease (CR=5):
- For M = 30 TS/ML the relative costs are 22 bits/TS,
- for M =120 TS/ML the relative costs are 17 bits/TS.

The loss probability for M=60 is additionally depicted.

Therefore, a comparison is necessary between STS arrays, having M=30 and 120 TS/ML, which are expanded such that they have approximately the same probability of loss for the same prescribed traffic per line (here $Y/n \sim 0.8$ Erl. and $B_{pp} \sim 2\%$).
Figure 16 shows the resulting curves 7,8 and the short notation of these expanded arrays. Their calculated costs are now:

- For M = 30 TS/ML 28 bits/TS,
- for M =120 TS/ML 26 bits/TS.

These costs show that "multiplexing before switching" may be favourable also for STS arrays, because of decreasing relative costs. Additionally, a smaller increase of loss in case of overload is obtained for M=120 TS/ML (cf. curves 7,8; Fig.16).
Further informations about the relative costs of STS and TST arrays, resp., can be found in Fig.17 and in the PCM-CHARTS.

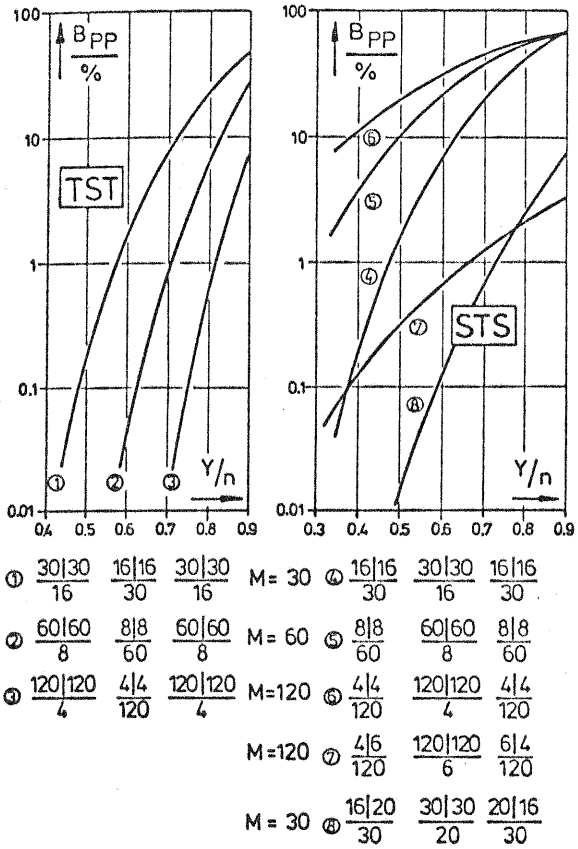


Fig. 16: Probability of Loss for Various TST and STS Arrays

In the following a comparison concerning the costs is presented between arrays which have a prescribed probability of loss and a constant number of terminations for a prescribed carried traffic per termination.

The constant number of terminations is n=4320; the traffic per termination is prescribed to 0.8 Erl. and the Point-to-Point loss to 0.1 %. The presented arrays use combined switching as well as separated switching.

It should be noted that the number of terminations is always equal to the number of TS for both switching modes. The calculated relative costs are depicted in Fig. 17 versus different numbers of Highways having M=30, 60 and 120 TS/ML. The linked values hold for the same total number of Highways connected to the array.

The first result to be seen is:
The relative costs of all PCM arrays are reduced if the number M of TS/ML is increased, while the total number of connected terminations remains constant. This holds for combined switching, denoted in the figure by circles as well as for separated switching, denoted in the figure by squares. The decrease of the costs is essentially due to the fact that the space switches become smaller as well as the costs per gate remain constant independently whether 30 or 120 TS have to be switched. The number of control memory bits for the gates is reduced, for the speech memories it is increased. Due to this increase it may sometimes be possible that the savings of the space switches are compensated by additional costs for the TSIs. This appears in particular if the SS and the CR are small.

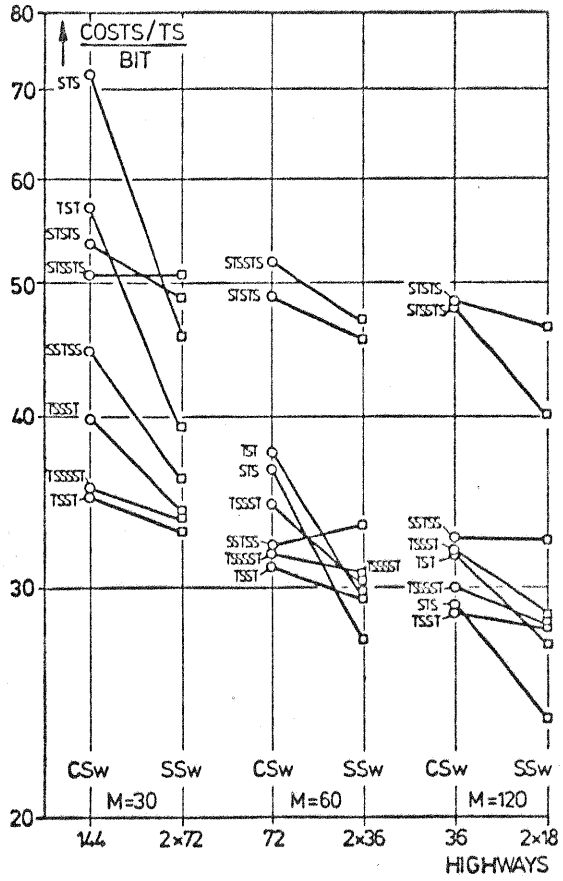


Fig. 17: Comparison of the Relative Costs per Time-Slot for Different Switching Modes and Various TS Numbers per Highway, n = 4320, Y/TS = 0.8 Erl., B_{PP} = 0.1%, CR = 5, Serial Switching
CSw: Combined Switching ○
SSw: Separated Switching □

Second result:
The figure shows that separated switching is generally cheaper than combined switching, represented by the falling lines between the circles and the squares. However, separated switching does not allow to establish connections between all Highways.
The decrease of the costs is again due to the fact that the SS become smaller as only half of the Highways are connected to one array (constant number of terminations provided).

There are some exceptions, however, e.g. the SSTSS array with M=60; there are savings in the number of gates but additional costs are necessary for control memories, that compensate the savings.

Third result:
The cost relation among the discussed arrays changes with the number of TS per ML.

For combined switching with 144 Highways the values are the same as in Fig.14 for HW=144.

For M=30, the 3-stage arrays are rather expensive, the 4-stage array is the cheapest.

For M=60 the STSTS and STSSTS array become most expensive. Again the reasons are the small SS and the great expansion necessary to obtain the prescribed loss probability. These two arrays remain expensive also for the other values of M, as this effect cannot be reduced.

For M=120 the costs of all arrays are smaller. The consequence is, if "multiplexing before switching" is not too expensive, it should be applied.

5.3 Influence of the Cost Ratio

The influence of the cost ratio is the last to be discussed. Up to now all comparisons have been based on CR=5=const. The influence of a various CR on the arrays having 144 Highways is shown in Fig.18. Of course, the costs of all arrays increase with an increasing cost ratio. The strongest increase suffer the three-stage arrays; the smallest increase holds for the T..T arrays. The decision, which cost ratio has to be assumed in practice, depends on the momentary technological standard as well as on the additional hardware costs for the control of the elements.

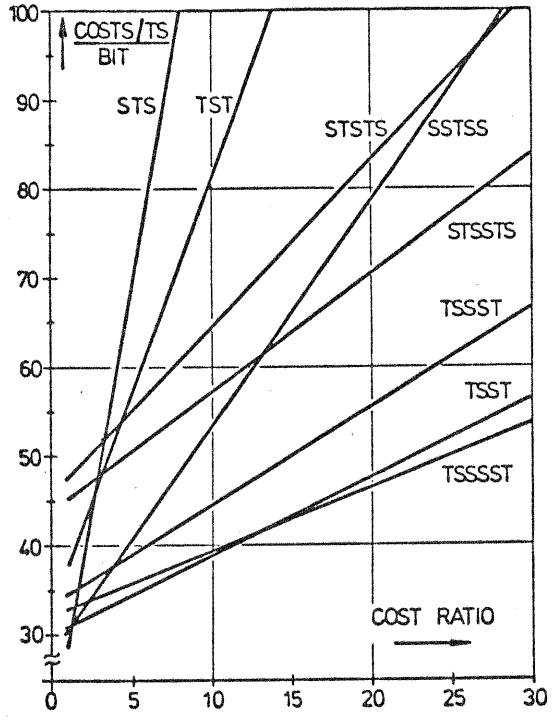


Fig. 18: Influence of the Cost Ratio CR
HW = 144, M = 30, Y/TS = 0.8 Erl., B_{pp} = 0.1%
Combined, Serial Switching

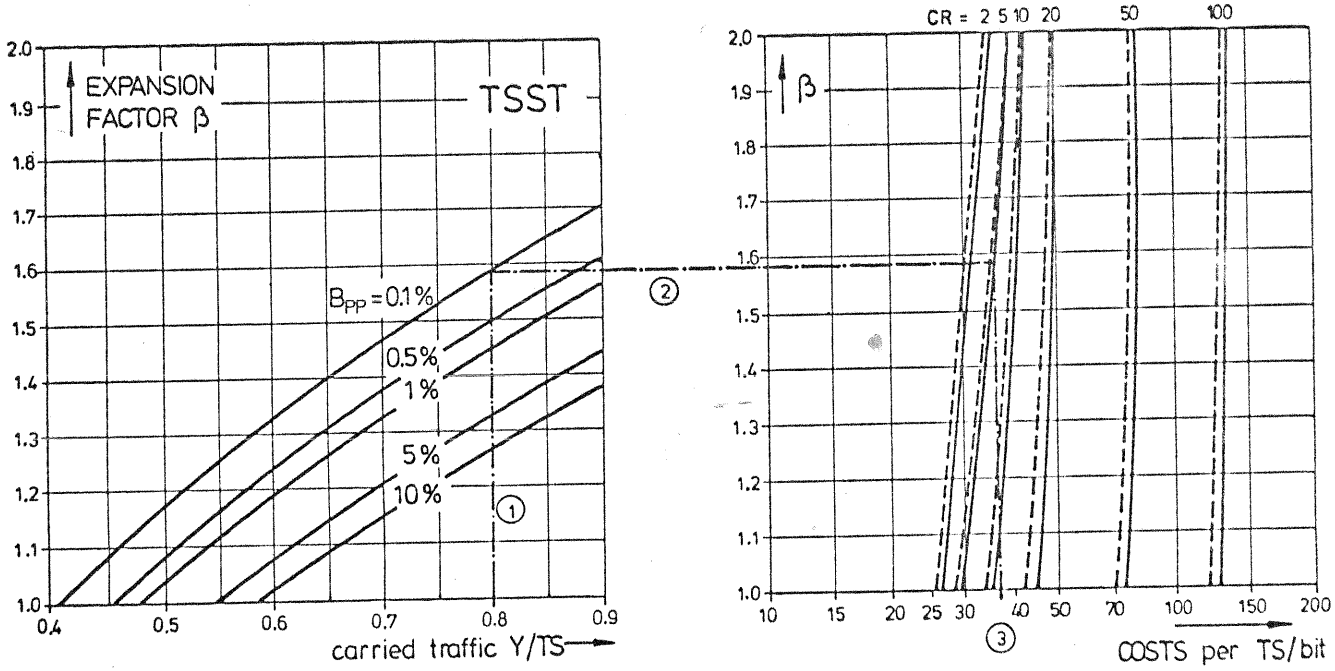
6. DESIGN OF ECONOMIC PCM SWITCHING ARRAYS BY MEANS OF THE PCM-CHARTS

In order to support field engineers in choosing the best suited PCM switching arrays for a certain application, a booklet with a large number of PCM-CHARTS will be edited. These PCM-CHARTS allow the design of economic switching arrays for various numbers of Highways and different values of M time-slots (TS) per multiplex line.
When the desired probability of loss for the prescribed carried traffic per time slot Y/TS (equal to the carried traffic per termination) is chosen, the array can be constructed.
Its resulting relative costs for different cost ratios can also be found in the charts. Fig.19 shows a PCM chart of one four-stage array.
The left chart shows the expansion of the array versus the carried traffic per TS, the probability of loss is the curve parameter. The curves hold for a PCM array using combined switching having 196 Highways and for an array using separated switching having 2·196 Highways.
The right chart shows the necessary costs for a given expansion; parameter for the curves is the cost ratio CR.
The bold line holds for combined switching, the dashed line for separated switching.
It should be noted that the array for separated switching has the double number of terminations.

The use of the charts will be shown by means of the following example.

A four-stage PCM-array is to be designed. The final size should allow to connect 196 Highways with M=30 TS each; combined switching is performed and CR be 5.
The required probability of loss for a prescribed Y/TS of 0.8 Erl is B_{pp} = 0.1 %.

Step 1: The necessary expansion can be found in the left chart; its value is about 1.6. This value, together with h_2=14 allows the design of the PCM array, see Fig.20. The additional "horizontal" MLs are necessary as combined switching is required. The expansion is performed by increasing the number of internal TS from 30 to 48.
Step 2: The resulting costs for different cost ratios can be found in the right chart.
Step 3: For CR=5 the costs are about 35 bits/TS.



COMBINED SWITCHING 1x196 HWs = 30·196 terminations h_2 = 14 MLs ——— COMBINED SWITCHING
SEPARATED SWITCHING 2x196 HWs = 2·30·196 terminations M = 30 TS/ML — — — SEPARATED SWITCHING

Fig. 19: Example for a PCM CHART of one TSST Array

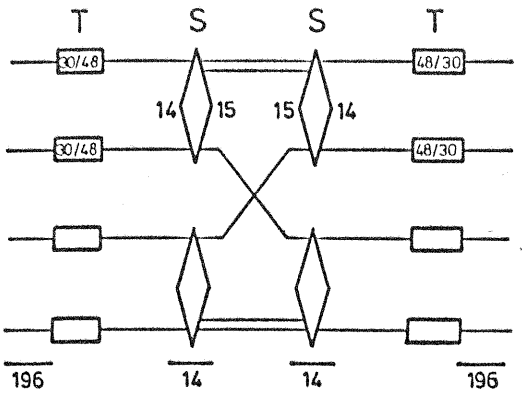


Fig. 20: Design Example for the TSST Array Y/TS = 0.8 Erl., B_{pp}= 0.1%, Comb.Switch.

7. SUMMARY

Symmetrical PCM switching arrays having one up to six stages, have been discussed in the paper. It was shown how the PCM arrays can be mapped into equivalent SDM arrays to simplify the calculation of their probability of loss. The relative costs of the PCM arrays have been calculated applying different switching modes. Design formulae are given which are derived in the related paper /14/. The paper concludes in presenting new PCM-CHARTS for the quick and economic design of PCM switching array.

ACKNOWLEDGMENT

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8. ANNEX

Formulae are given to calculate the amount of gates (G), the amount for their control memories (CMG), the number of speech memories (SM) and their control memories (CMSM). The equations have a general form in order to allow their application also if e.g. additional MLs have to be provided. The prerequisite of symmetrically structured arrays is already implemented.

Abbreviations and prerequisites:

G	: number of gates	
CMG	: number of control memory bits for the gates	
SM	: number of speech memory bits	
CMSM	: number of control memory bits for the SMs	
M	: number of time-slots per multiplex-line	
E	: separated switching	E = 2
	combined switching	E = 1
P	: switching in serial	P = 1
	parallel switching	P = 8
ß	: expansion factor $j_1:h_1$, M* : M	
	expansion is always performed in the first and the last stage, intermediate stages switch 1:1	
ld a	: logarithmus dualis $\log_2 a$	
Q	: allocation priciple within S..S arrays	
	symmetrical allocation	Q = 1
	quasisymmetrical allocation	Q = 0.5

- the number of incoming and outgoing ML is identical
- switching arrays are structured symmetrically
- the forming of blocks is as discussed above

TST:

$G = h_2^2 \cdot E \cdot P$

$CMG = h_2 \cdot ß \cdot M \cdot ld\ h_2$ *)

$SM = h_2 \cdot M \cdot 2 \cdot 8 \cdot E$

$CMSM = h_2 \cdot ß \cdot M \cdot E \cdot ld\ M$

STS:

$G = h_1 \cdot j_1 \cdot 2 \cdot E \cdot P$

$CMG = h_1 \cdot M \cdot E \cdot ld\ j_1$

$SM = j_1 \cdot M \cdot 8 \cdot E$

$CMSM = j_1 \cdot M \cdot Q \cdot ld\ M$

TSST:

$G = HW \cdot j_2 \cdot 2 \cdot E \cdot P$

$CMG = HW \cdot ß \cdot M \cdot E \cdot ld\ j_2$

$SM = HW \cdot M \cdot 2 \cdot 8 \cdot E$

$CMSM = HW \cdot ß \cdot M \cdot E \cdot ld\ M$

TSSST:

$G = (HW \cdot j_2 \cdot 2 + h_3 \cdot j_3 \cdot j_2) \cdot E \cdot P$

$CMG = HW \cdot ß \cdot M \cdot E \cdot ld\ j_2 + j_2 \cdot h_3 \cdot ß \cdot M \cdot ld\ h_3$

$SM = HW \cdot M \cdot 2 \cdot 8 \cdot E$

$CMSM = HW \cdot ß \cdot M \cdot E \cdot ld\ M$

SSTSS:

$G = (HW \cdot j_1 \cdot 2 + h_2 \cdot j_2 \cdot j_1 \cdot 2) \cdot E \cdot P$

$CMG = (ld\ j_1 + ß \cdot ld\ j_2) \cdot HW \cdot M \cdot E$

$SM = j_1 \cdot j_2 \cdot M \cdot 8 \cdot E$

$CMSM = j_1 \cdot j_2 \cdot M \cdot Q \cdot ld\ M$

STSTS:

$G = (HW \cdot j_1 \cdot 2 + h_3 \cdot j_3 \cdot j_1) \cdot E \cdot P$

$CMG = (E \cdot ld\ j_1 + ß \cdot ld\ j_3) \cdot HW \cdot M$

$SM = HW \cdot ß \cdot M \cdot 2 \cdot 8 \cdot E$

$CMSM = HW \cdot ß \cdot M \cdot E \cdot ld\ M$

TSSSST:

$G = (HW \cdot j_2 \cdot 2 + 2 \cdot h_3^2 \cdot j_3 \cdot j_2) \cdot E \cdot P$

$CMG = (HW \cdot ß \cdot M \cdot ld\ j_2 + j_2 \cdot h_3 \cdot ß \cdot M \cdot ld\ j_3) \cdot E$

$SM = HW \cdot M \cdot 2 \cdot 8 \cdot E$

$CMSM = HW \cdot ß \cdot M \cdot E \cdot ld\ M$

STSSTS:

$G = (HW \cdot j_1 \cdot 2 + h_3^2 \cdot j_3 \cdot j_1) \cdot E \cdot P$

$CMG = (HW \cdot M \cdot ld\ j_1 + HW \cdot ß \cdot M \cdot ld\ j_3) \cdot E$

$SM = HW \cdot ß \cdot M \cdot 2 \cdot 8 \cdot E$

$CMSM = HW \cdot ß \cdot M \cdot E \cdot ld\ M$

*) whenever ld a is used, it has to be checked whether the result is an integer value; if not, the next greater integer value has to be chosen for the calculation of the number of bits.

Example:
In order to show the use of these formulae, a TSSST array will serve as an example for the calculation of the different values.
In Fig.21 the considered array is depicted; combined and serial switching is applied (E=1, P=1). The expansion is chosen such that B_{pp}=0.1% for Y/TS= 0.8 Erl. is achieved.

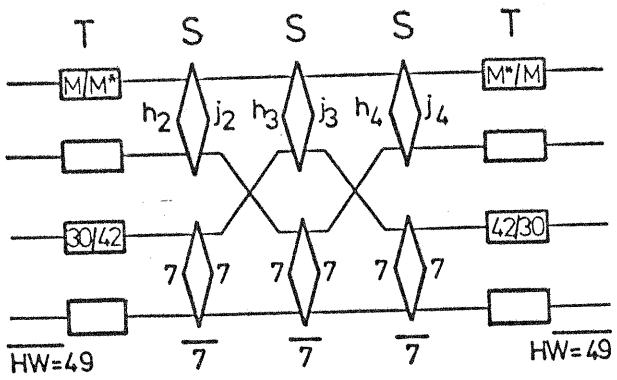

Fig.21: TSSST Array as Example for the Calculation of the Relative Costs

$G=(HW\cdot j_2\cdot 2+h_3\cdot j_3\cdot j_2)\cdot E\cdot P=(49\cdot 7\cdot 2+7\cdot 7\cdot 7)\cdot 1\cdot 1 = 1029$

$CMG=HW\cdot \beta\cdot M\cdot E\ ldj_2+j_2\cdot h_3\cdot \beta\cdot M\cdot ldh_3=49\cdot 42\cdot 1\cdot 3+7\cdot 7\cdot 42\cdot 3=12348$

$SM=HW\cdot M\cdot 2\cdot 8\cdot E = 49\cdot 30\cdot 2\cdot 8\cdot 1 = 23520$

$CMSM=HW\cdot \beta\cdot M\cdot E\cdot ldM = 49\cdot 42\cdot 1\cdot 5 = 10290$

Assuming a cost ratio CR=5, the resulting relative costs are: (compare also Fig.14)

Costs per TS=(1029·5+12348+23520+10290)/49·30
= 34.92 bits/TS.

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