DIGITAL INTEGRATED CIRCUITS

by

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SUMMARY:

The present paper is concerned with the monolithic semiconductor technique for digital integrated circuits. After an introduction to the various types and aims of integration the bipolar planar silicon process is briefly described. The main part of this paper is devoted to the different families of digital integrated circuits featuring the present situation. For each family the basic functions, advantages, and disadvantages are described. An outlook to new technologies and new fields of application concludes the paper.

CONTENTS:

1. INTRODUCTION

Since the first experiments with semiconductor effects in 1948 made by SHOCKLEY, BARDEEN, and BRATTAIN semiconductor technologies have spread over all fields of communication. In the fifties semiconductor devices found their application almost exclusively in linear amplifiers, whereas in the sixties semiconductor circuits have been used to a great extent in digital electronic computers; in fact, they made possible the computer-era at all. As far as we can see, the seventies will be characterized by application of large scale integrated microelectronic circuits which realize complete functions of complex structures.

1.1 Types of integration technologies

Within the integrated circuits mainly three types of different technologies can be distinguished, see table 1. In this paper only

SEMICONDUCTOR MONOLITHIC:	Transistors, diodes, and resistors are diffused into one single piece of silicon. Interconnections are made by thin-film metal.
THIN-FILM MONOLITHIC:	All elements are formed by thin-film deposition of metal on a single substrate.
THIN-FILM HYBRID:	Passive elements are deposited as thin-films. Semiconductor active devices are soldered or welded to the substrate.

Table 1: Main types of integration technologies, according to [1]

the most important group, the semiconductor monolithic group, will be treated. However, some new technologies which will come up to date in near future will be addressed briefly.

1.2 Scales of integration

By integration we understand the fabrication of whole circuits on a single chip. Several chips joined together form the module, which is defined as the smallest batch fabricated unit that can

be fully tested and replaced. By defining a circuit as a small functional group of components, e.g. one NAND gate, or one JK flip-flop, we can classify the scale of integration as follows, see table 2.

SMALL SCALE INTEGRATION (SSI):	<10	circuits per module
MEDIUM SCALE INTEGRATION (MSI):	10 to 100	circuits per module
LARGE SCALE INTEGRATION (LSI):	>100	circuits per module

1 circuit = small functional group of components, e.g. one logic NAND gate, or one JK flip-flop.

1 module = smallest batch fabricated unit that can be fully tested and replaced.

Table 2: Scales of integration, according to [1]

1.3 Aims of integration

The basic aims of integration can be outlined by the following headlines:

- efficient mass production
- higher reliability
- better performance
- minimum cost
- minimum size
- new possibilities for circuit realizations.

Today, we cannot foresee all the advantages that integration will bring in future. Especially the last point will be of importance. A typical example is the development of large scale integrated active memories. To that development we come back at the end of this paper.

2. THE BIPOLAR PLANAR SILICON PROCESS

Most of today's integrated circuit production is based on the planar silicon process. Therefore, let us do a short excursion to the various fabrication steps of integrated microelectronic circuits.

2.1 Crystal preparation

At first, the semiconductor crystal (silicon) is melted. From the melted crystal a single crystal is pulled what is called the p-substrate. The single crystal is cut into wafers of 0.2 mm thickness and about 30 mm in diameter containing 200 up to 1000 chips. Finally, the wafers are polished to have a smooth surface for further fabrication steps.

2.2 Mask fabrication

Normally, four different masks are needed for the diffusion processes of subcollector, isolation, base, and emitter (collector). Three more masks are needed additionally for opening the contact holes, etching of the metal interconnection pattern, and finally for opening of the contact holes in a protective sputtered quartz overlayer for chip wiring. The chip masks for the several photolithographic processes are reduced 500-times and multiplied to form the wafer mask. Both is done by step-and-repeat camera methods.

2.3 Subcollector diffusion

In a first step the wafers are oxidized. A very thin layer of silicon dioxide SiO_2 is thermally grown on the wafer surface. In the planar process this layer is typical and will be used for etching of the several diffusion masks, and metallization masks, respectively. Contrarily to the fabrication of single transistors a highly conductive layer is needed underneath the collector to reduce the collector resistance and parasitic currents. In single transistors the collector is located underneath the chip. In integrated circuits this is not possible, because all electrodes have to be at the same chip side for the wiring metallization. The subcollector can be realized by a highly doped buried layer

that is diffused into the substrate before the lower doped collector layer is epitaxially deposited later.

Fig.1 shows the cross-section of a bipolar planar silicon integrated circuit. For the diffusion of the subcollector a hole is

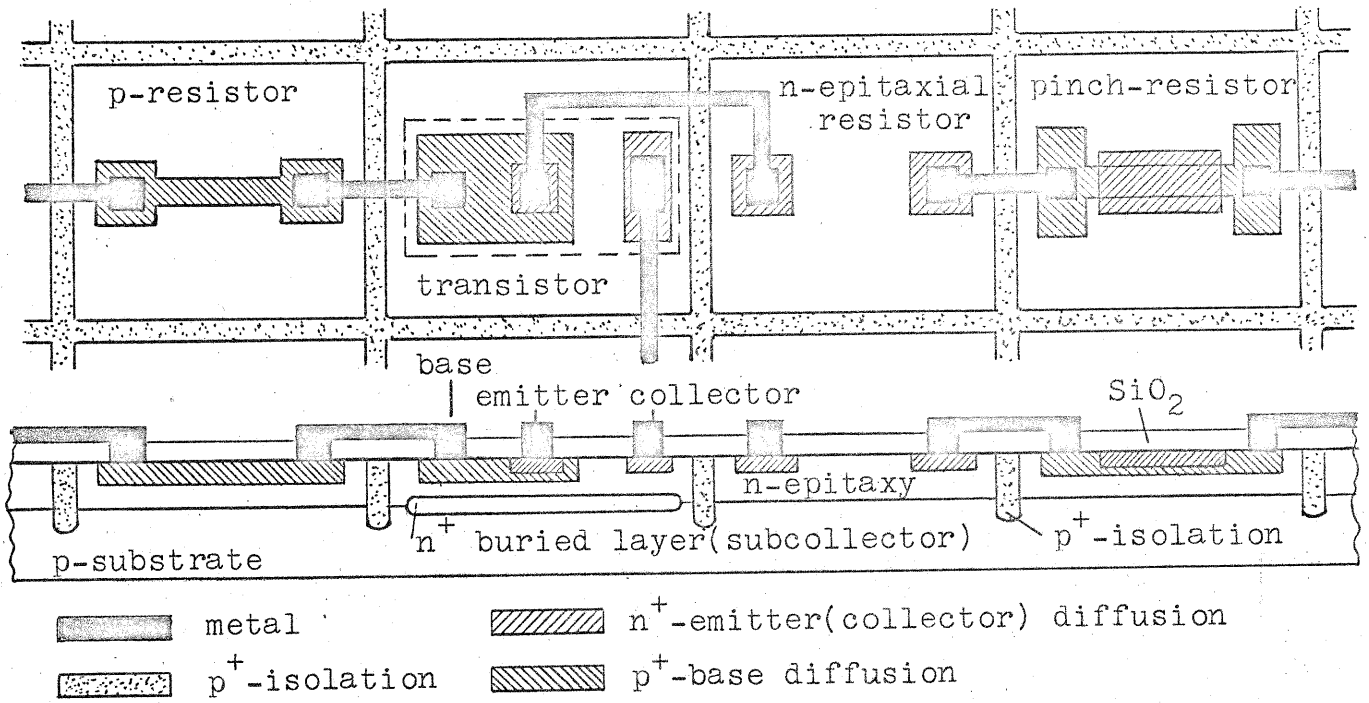


Fig.1: Cross-section of a bipolar planar silicon integrated circuit, according to [1]

etched into the silicon dioxide layer by a photolithographic method. Then arsenic As is diffused into the holes of the chips at a temperature of 1200 °C. By this process very high doped n^+-swimming islands are spread over the wafer.

2.4 Epitaxial growth and thermal growth

After etching the rest of silicon dioxide a single crystal silicon layer is epitaxially grown. This can be done in a silicon chlorate $SiCl_4$ gas atmosphere at a temperature of 1170 °C. The equation for the chemical reaction is given by

$$SiCl_4 + 2H_2 \rightleftharpoons Si + 4HCl \ .$$

At the beginning the process follows according to the dashed arrow. The epitaxial process, however, follows later according to the arrow from the left to the right. The high temperature is needed that the silicon atoms Si form a single crystal again. By this

the n^+-swimming islands become completely buried into the single crystal silicon. The epitaxially grown silicon is low n-doped to reduce the collector resistance. Finally, the surface of the whole wafer is covered again with thermally grown silicon dioxide.

2.5 Photolithographic processes and diffusion processes

To etch the holes for the different diffusion processes a standard photoresist technique is used to expose the silicon dioxide at the desired locations. Etching is done with hydrofluoric acid HF.

Now, in another three similar steps, the p^+-isolation diffusion, the p^+-base diffusion, and the n^+-emitter(collector) diffusion are made. The p^+-isolation is done in bor B atmosphere at a temperature of 1200 ^{o}C as long until the diffusion goes through the n-epitaxial layer into the p-substrate. Doing so the former continuous n-epitaxy is split into many single n-boxes which are surrounded by p-material. In the transistor boxes, as shown in fig. 1, the n-epitaxial region defines the collector zone of the transistor.

The diffusion processes have two phases, a pre-diffusion and an after-diffusion phase. During the pre-diffusion phase the whole impurity content is diffused into the very surface region. During the successive after-diffusion phase the impurity spots penetrate deeper into the substrate at which the impurity density decreases. By this the density and depth of the diffusion can be controlled if the temperature is maintained constant by at least 1 ^{o}C. Pre-diffusion lasts about 1 hour, while after-diffusion lasts up to 4 hours.

2.6 Metallization and chip mounting

Ohmic contacts are achieved by the same mask and photolithographic processes as for doping and successive evaporation of aluminium. After the chip functional testing, which is done today automatically with computer aid, the good chips are marked and the wafer is cut into the single chips. On the aluminium layer the terminal wires are bonded. Then the chips are joined together to form the module which is encapsulated finally.

The package configurations used for integrated circuits are the TO-5 package, the Dual-in-Line package, and the ceramic flat pack.

2.7 Some problems in the development of integrated circuits

The minimum dimension of integrated circuits is limited by two basic facts: firstly, the tolerances of the fabrication process, and secondly, the minimum size for the emitter to carry a certain current. Therefore, a high degree of exactness in the fabrication process is needed.

The fabrication of diodes is achieved by using emitter-base or collector-base junctions of transistors. By special arrangements, such as short-circuiting of the collector and base terminals, special characteristics, such as low break-down voltage or low offset voltage, can be achieved.

Resistors can be produced by different technologies. For low resistance values we can use the p-region or the region of a n-epitaxial layer. Higher values for the resistors can be achieved by using a p-layer which is overlaid by a n-layer. Both layers have to be reverse biased so that the current only can flow through the very thin p-layer. A resistor of this kind is the n-overlaid p-resistor (pinch resistor) which takes values of about 100 kOhm.

Another problem in integrated circuit production is the isolation. The most popular method for isolation is the diffusion of a highly doped p^+-layer which reaches through the n-epitaxial layer into the p-substrate. By reverse biasing of the substrate it can be attained that all electrodes of the different boxes form reverse biased pn-junctions to the substrate. Other methods use silicon dioxide layers or non-conductive substrates for isolation.

An important aspect in integrated circuit design is to avoid parasitic effects. They may happen if the substrate is not enough reverse biased against other electrodes. The four-layer pnpn-structure may then act as a thyristor. Therefore, the p-substrate must be connected with the most negative point of the circuit. In many integrated circuit realizations the negative power supply is directly connected with the p-substrate. Similar is the problem that resistors do not become conductive with the substrate. To avoid this the n-boxes must be connected with the most positive point of the circuit. The isolated boxes itself have to be as small as possible to reduce parasitic capacitances.

Another problem arises in the fabrication of two or more diodes with a common p-layer for integrated logical circuits, e.g. the input gate of the Diode-Transistor Logic (DTL) family. Between the n-, p-, and n-layers a lateral transistor effect may happen; then the dimensioning must be so that the current gain of that lateral transistor effect is comparatively small.

For a more detailed discussion of problems in integrated circuit production see [2].

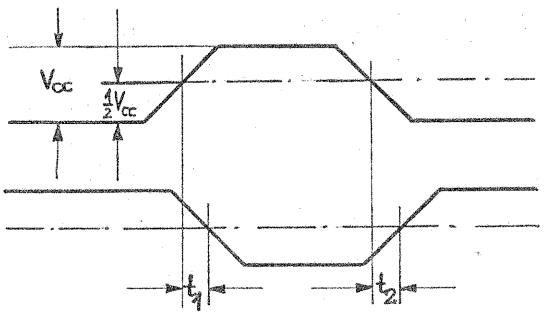
3. FAMILIES OF DIGITAL INTEGRATED CIRCUITS

In this section a summary of the most important logic circuit families will be given featuring the present situation. For each family a typical part of the circuit will be shown which characterizes the family. The basic advantages and disadvantages of the circuit family in question will be mentioned.

Before starting we want to introduce some definitions for digital integrated circuits, see fig.2

fan-in:	maximum number of inputs
fan-out:	maximum number of outputs
positive logic:	logic "0" has low potential and logic "1" has high potential
nagative logic:	logic "0" has high potential and logic "1" has low potential

propagation delay t_{pd}



input signal

output signal

$$t_{pd} = \frac{t_1 + t_2}{2}$$

Fig.2: Definitions for digital integrated circuits

3.1 Direct-Coupled-Transistor Logic (DCTL) Resistor-Transistor Logic (RTL)

In fig.3 the basic configuration of a NOR gate in DCTL is shown. Typical for this logic are the base resistors which are to avoid a non-symmetric current distribution between parallelled transistors, the so-called current-hogging problem [3], [4]. A certain disadvantage is the low threshold voltage which varies between 0.5 and 1 volt. This threshold voltage is additionally dependent on the temperature. Therefore, these circuits do not have a high noise immunity. Typical values of the propagation delay are 10 to 40 ns.

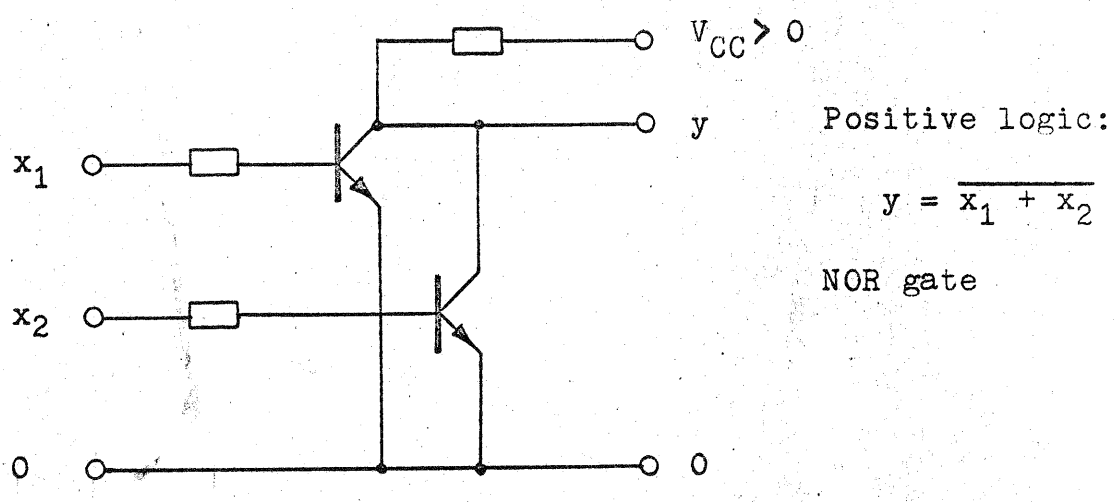


Fig.3: Direct-Coupled-Transistor Logic (DCTL)
Resistor-Transistor Logic (RTL)

3.2 Diode-Transistor Logic (DTL)

Fig. 4 shows a basic DTL circuit which contains the input logic gate, an offset diode, and an inverter gate at the output.

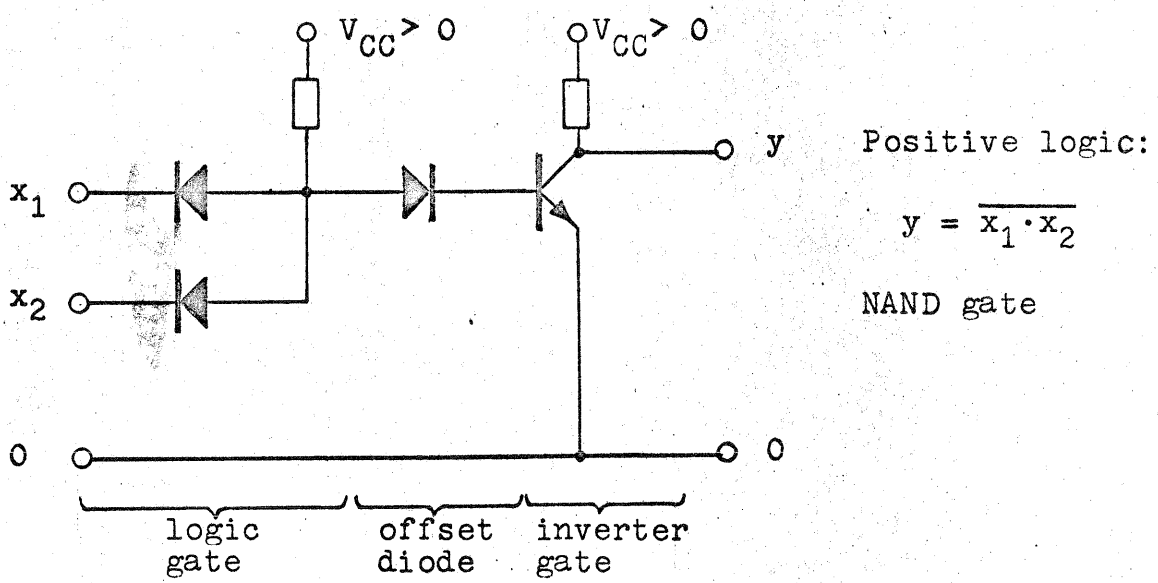


Fig.4: Diode-Transistor Logic (DTL)

The name for this logic family, which has been used already in conventional non-integrated circuits, originates from the logic diode gate at the input. The offset diode is used to increase the noise immunity by the amount of the offset voltage of that diode. For high noise immunity up to 6 volts a Zener diode can

be used. This special type of the DTL family is named DTLZ [5]. The DTL has a typical propagation delay of 20 to 100 ns. During the past the DTL has probably been the most used family for digital applications [6].

Another special type of this logic family is the Load-Compensated Diode-Transistor Logic (LCDTL) which is shown in fig.5 [7].

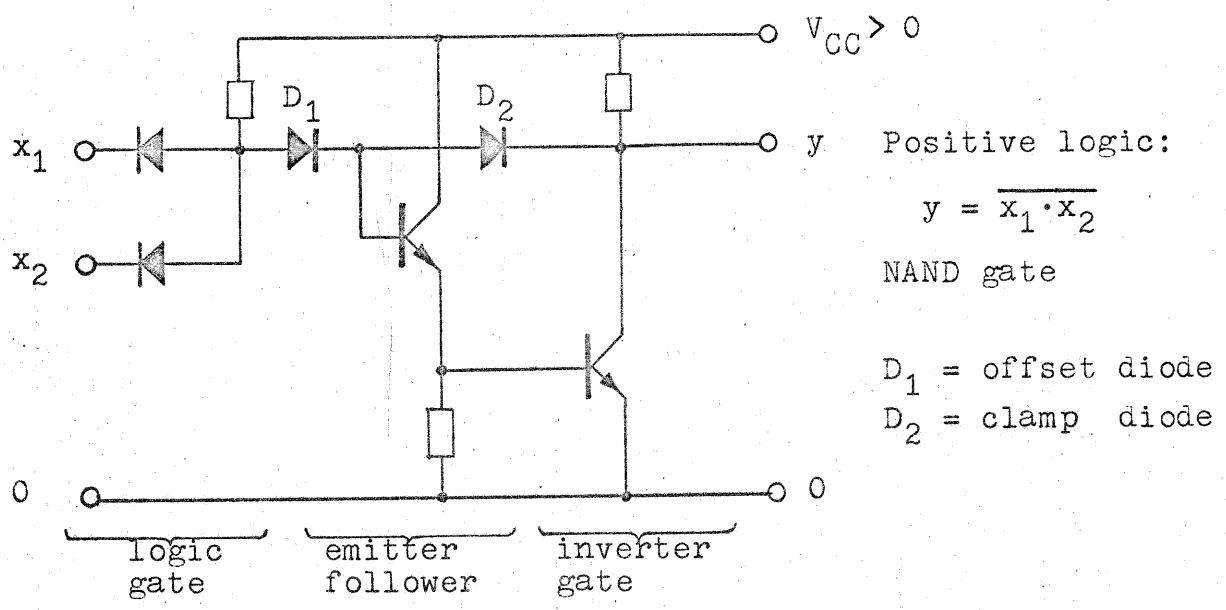
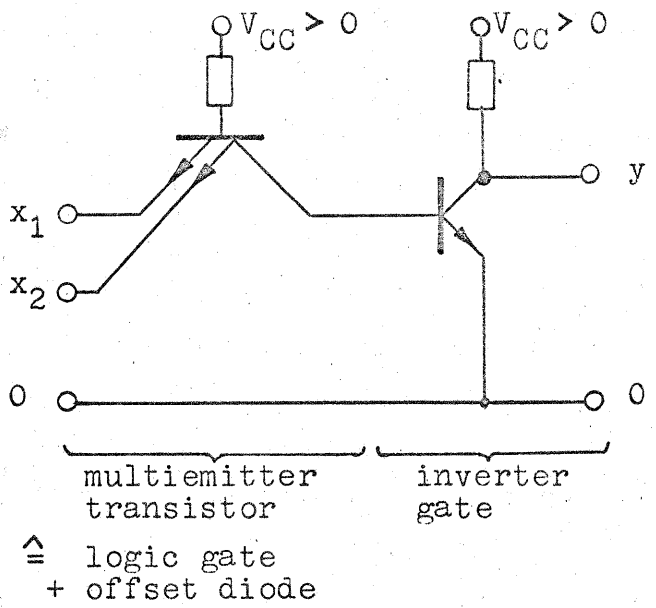


Fig.5: Load-Compensated Diode-Transistor Logic (LCDTL)

The output of the offset diode goes to a collector circuit (emitter follower) which drives the output inverter gate. The emitter follower draws just enough current from the power supply to sustain the load current. The circuit is load-compensated in this sense, that the driving current increases as the load current increases at the output. For the output inverter gate additionally a clamp diode is used to avoid the saturation of that transistor. This logic is slightly faster than DTL and has a high fan-out capability.

3.3 Transistor-Transistor Logic (TTL)

The logic circuit and the offset diode of the DTL circuit fig.4 can be combined to a multiemitter transistor. Fig.6 shows the basic circuit of the TTL family [3], [4]. The logic function of that circuit is equivalent to the logic function of the DTL circuit fig.4.



Positive logic:

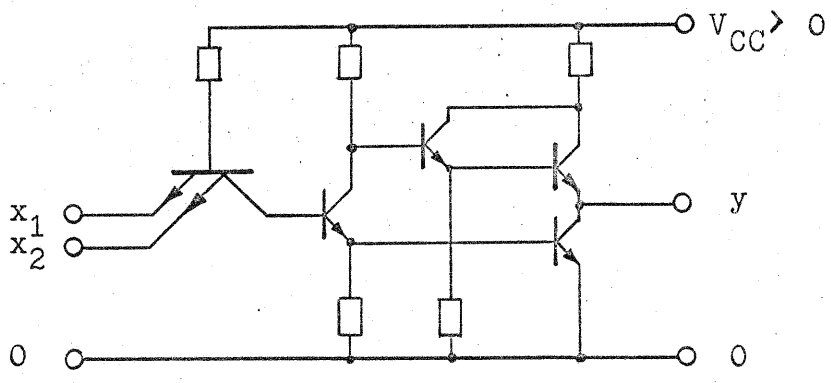
$$y = \overline{x_1 \cdot x_2}$$

NAND gate

Fig.6: Transistor-Transistor Logic (TTL)

If at least one input is at zero voltage (logic "0") the multiemitter transistor functions as a saturated common emitter circuit in normal mode of operation. The collector of the multiemitter transistor is approximately at zero voltage and the output inverter transistor operates in the cutoff state. The output is then at V_{CC}-level (logic"1"). If all inputs are at high voltage (logic "1") the multiemitter transistor functions as common emitter circuit in inverted mode of operation, i.e. the collector-base diode is conductive and the output inverter transistor operates in the saturated state. The output is then at zero level (logic "0").

Practical TTL circuits use in addition a DARLINGTON transistor circuit at the output to reduce the output impedance and to improve the speed even for capacitive load [8], [9]. In fig.7 such a practical TTL circuit is shown.



Positive logic:

$$y = \overline{x_1 \cdot x_2}$$

NAND gate

Fig.7: TTL circuit with output DARLINGTON transistor circuit

TTL circuits have very low propagation delay, bacause the charges for the output circuit are not delivered by passive diodes but by an active transistor. Typical values of the propagation delay are 4 to 15 ns. TTL has large fan-out capability (up to 50) and is fully compatible with the DTL family. At the end of 1968 TTL was probably the most used logic circuit family for digital applications.

3.4 Current-Mode Logic (CML)
Emitter-Coupled-Transistor Logic (ECTL)
Emitter-Coupled-Current-Steered Logic (ECCSL)

The DCTL, DTL, and TTL families, which we have discussed above, work according to the saturated mode principle, i.e. the transistor is steered from the cutoff state into the saturated state. In the following we will say the transistor is OFF, if it is non-conductive, and the transistor is ON, if it is conductive. Fig.8 shows the basic circuit and the collector current - collector-to-emitter voltage characteristic for the saturated switching mode. The transistor is OFF, if the input voltage is low. Then only the collector-cutoff current I_{CBO} flows and the output is approximately at V_{CC}-level. The transistor is ON, if the input voltage is high. The collector current is approximately given by $I_C = V_{CC}/R$. The output voltage is the collector-to-emitter saturation voltage $V_{CE(SAT)}$, which has a small amount of about 200 mV.

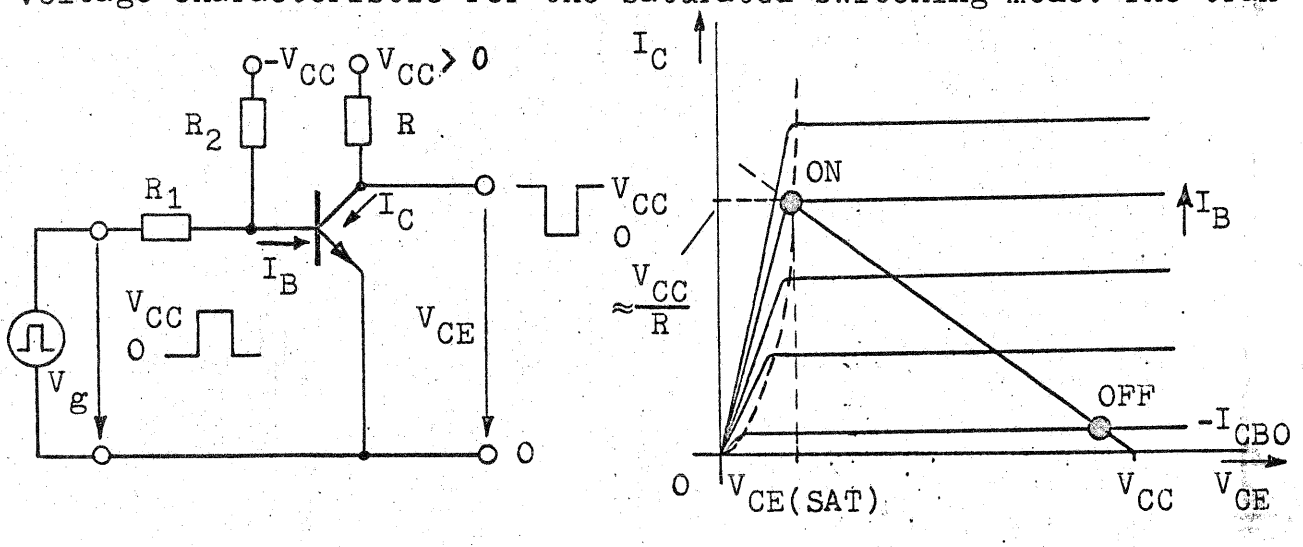


Fig. 8: Saturated switching mode

For current switching mode usually two transistors T_1 and T_2 are needed, as shown in fig. 9. Transistor T_2 is biased by the constant voltage $V_{CC}/2$, while transistor T_1 is steered by voltages which are symmetrically to the $V_{CC}/2$ -level:

$$V_{g(ON)} \geq \frac{V_{CC}}{2} + (V_{BE(SAT)} - V_{BE(FL)}) \qquad T_1 \text{ is ON, } T_2 \text{ is OFF,}$$

$$V_{g(OFF)} \leq \frac{V_{CC}}{2} - (V_{BE(SAT)} - V_{BE(FL)}) \qquad T_1 \text{ is OFF, } T_2 \text{ is ON,}$$

where $V_{BE(SAT)}$ is the base-to-emitter saturation voltage and $V_{BE(FL)}$ is the base-to-emitter floating voltage. The difference

$$(V_{BE(SAT)} - V_{BE(FL)})$$

takes values of about 700 mV and does not depend on temperature. Both transistors are feedbacked by the common-emitter resistor R_E which is characterizing for the current-mode.

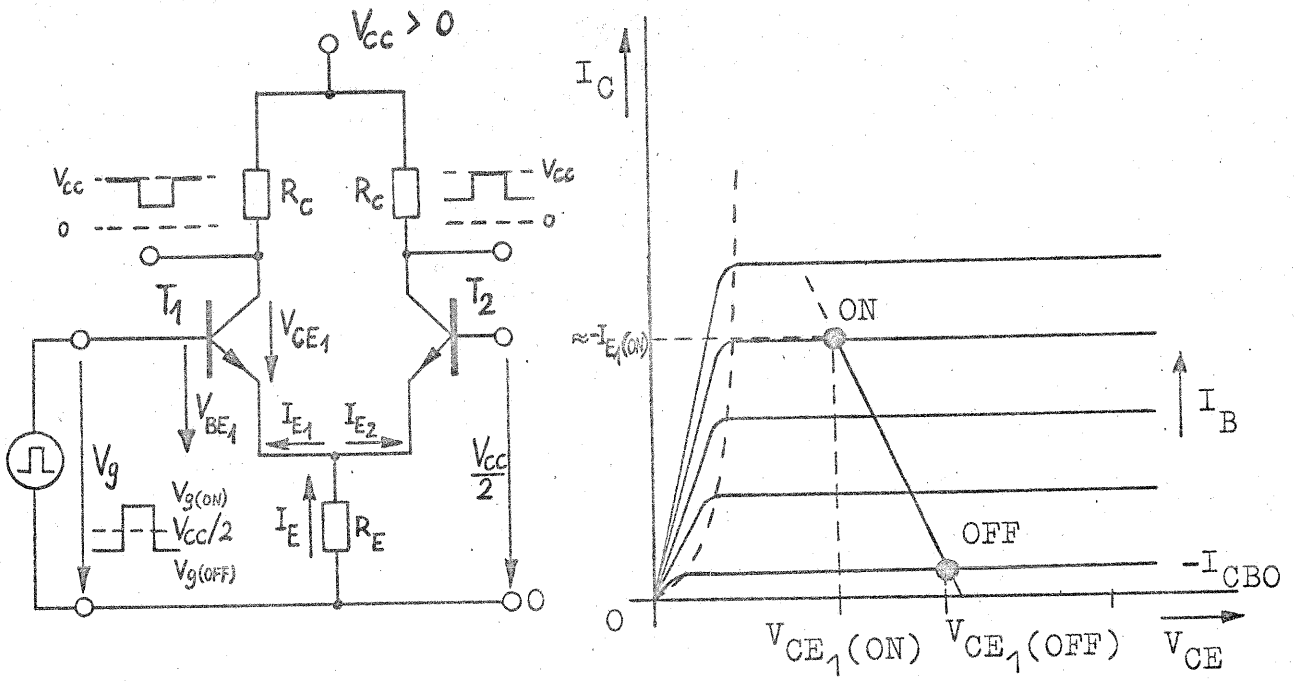


Fig. 9: Current switching mode

Many realizations of the current switch use a constant current source instead of the common-emitter resistor R_E. As proved below, R_E realizes a constant current source only approximately. A quite better solution is that with a transistor circuit. Below we will give an example of such a realization.

The basic function of the current switch can be described as follows. When the input voltage is low T_1 is non-conductive and T_2 is conductive (OFF-state). Then

$$I_{E_1(OFF)} \approx 0,$$

$$I_{E_2(OFF)} \approx \frac{V_{BE(SAT)} - \frac{V_{CC}}{2}}{R_E} .$$

The collector-to-emitter voltage of T_1 is

$$V_{CE_1(OFF)} \approx \frac{V_{CC}}{2} + V_{BE(SAT)} .$$

When the input voltage is high T_1 is conductive and T_2 is non-conductive (ON-state). Then

$$I_{E_1(ON)} \approx \frac{V_{BE(SAT)} - V_{g(ON)}}{R_E} ,$$

$$I_{E_2(ON)} \approx 0.$$

The collector-to-emitter voltage of T_1 is

$$V_{CE_1(ON)} \approx V_{CC} - \left(\frac{V_{CC}}{2} - V_{BE(FL)} \right) . \frac{R_E + R_C}{R_E} .$$

From the above equations one can see that

$$I_{E_1(ON)} \approx I_{E_2(OFF)} ,$$

in other words, an approximately constant current is switched over from one transistor to the other and vice versa. This property dominates in all current-mode realizations and has given the name for them. We can further see that for convenient choice of R_E and R_C the ON-operating point of T_1 can be placed in the active region. For transistor T_2 similar conditions can be derived. The fact that current switching mode avoids the saturated region causes, that no storage time occurs when the transistor is turned off. Current-mode logic circuits have the lowest propagation delay of all digital integrated circuits.

Fig. 10 shows the basic OR (NOR) gate in current-mode logic CML [3], [4]. Other names for this logic family are emitter-coupled-transistor logic (ECTL) and emitter-coupled-current-steered logic (ECCSL). Transistor T_1 of fig.9 is replaced by

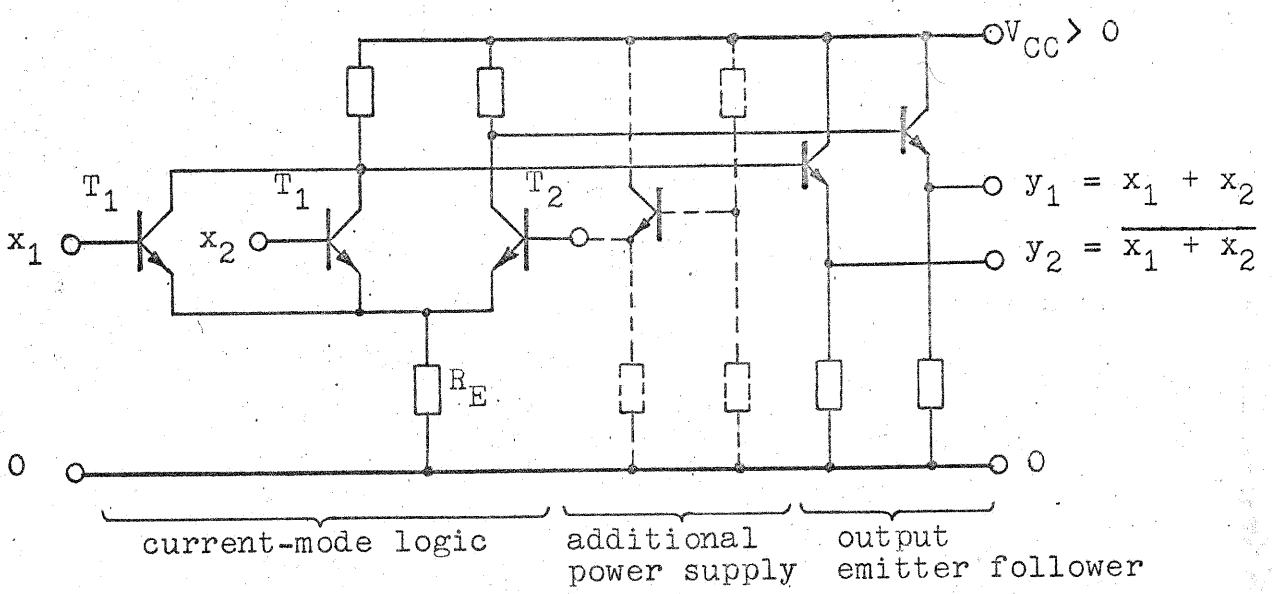


Fig. 10: Basic OR (NOR) gate in Current-Mode Logic (CML)

the logic gate input transistors , while transistor T_2 has the same function as in fig. 9. At the output an emitter follower circuit is added which provides high current capability, i.e. a high fan-out. The additional need of a second power supply $V_{CC}/2$ seems to be a disadvantage for this logic family. In integrated ECTL circuits, however, this voltage is generated from the power supply voltage V_{CC} by a transistor and additional three resistances, as shown in fig. 10, so that this is no objection to ECTL [8].

Another realization of ECTL uses emitter followers at the input. The (complementary) outputs are formed by the collector terminals of the current switch [10]. In Fig. 11 the basic part of this circuit is shown, containing the emitter follower logic input gate, the current switch, and the constant current source. The second power supply is realized by a transistor circuit again. This realization provides high current capability required to drive very low impedance terminated transmission lines. The original realization [10] uses additionally a current switch as constant current source which can also be steered by an emitter follower input gate. By this a two-stage logic with higher logic

power can be realized. The basic element, which has the logic function $y = a_1 + a_2 + \bar{b}_1 \cdot \bar{b}_2$, can be used for the realization of all logic functions as well as for storage elements (flip-flops).

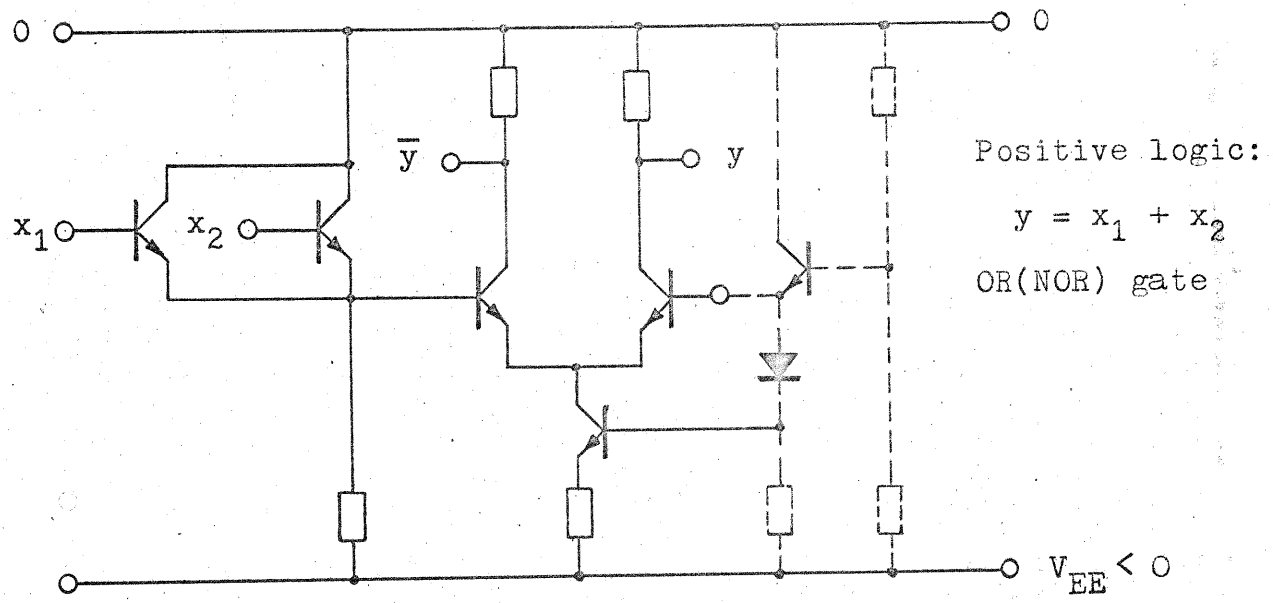


Fig. 11: ECTL realization with input emitter followers and constant current source

The advantages of the ECTL family can be outlined as follows:

- transistors do not work in the saturated region
- very low propagation delay (typical values are 1.5 to 4 ns)
- high fan-out capability
- at the same time the logic signal and its complement are available
- the threshold voltage does not depend on the temperature.

The disadvantages of ECTL circuits are a higher power dissipation (at each time one transistor is conductive) and a smaller difference between the logic "0" and the logic "1" levels than in saturated mode logic families.

ECTL digital integrated circuits are used today in ultra-high-speed computer applications. The constant power supply drain simplifies power distribution and minimizes power supply noise. The complementary outputs reduce the number of gates which is required to realize a specific function. Today ECTL circuits are on the market which have 8 OR/NOR functions, or one half adder, or a flip-flop within one package.

3.5 Metal-Oxide-Silicon Field-Effect-Transistor Logic (MOSFETL)

Insulated gate field-effect-transistors (MOSFET) are unipolar devices in which the number of carriers is controlled by an electric field. FETs may be either n-channel or p-channel types depending on whether the (majority) carriers are electrons or holes. Enhancement types (either n- or p-channel) are at zero bias voltage non-conductive, they become conductive if they are positive (n-channel) or negative (p-channel) biased. Depletion types (either n- or p-channel) are at zero bias voltage conductive, they become non-conductive if they are negative (n-channel) or positive (p-channel) biased. For digital applications the enhancement type MOSFET is advantageous because it allows direct coupling without level-shifting networks.

In fig. 12 a cross-section of a n-channel enhancement type MOSFET is shown. On a p-silicon substrate highly doped n^+-regions are diffused which form the source (S) and the drain (D) regions, respectively. The channel is formed by the region between both

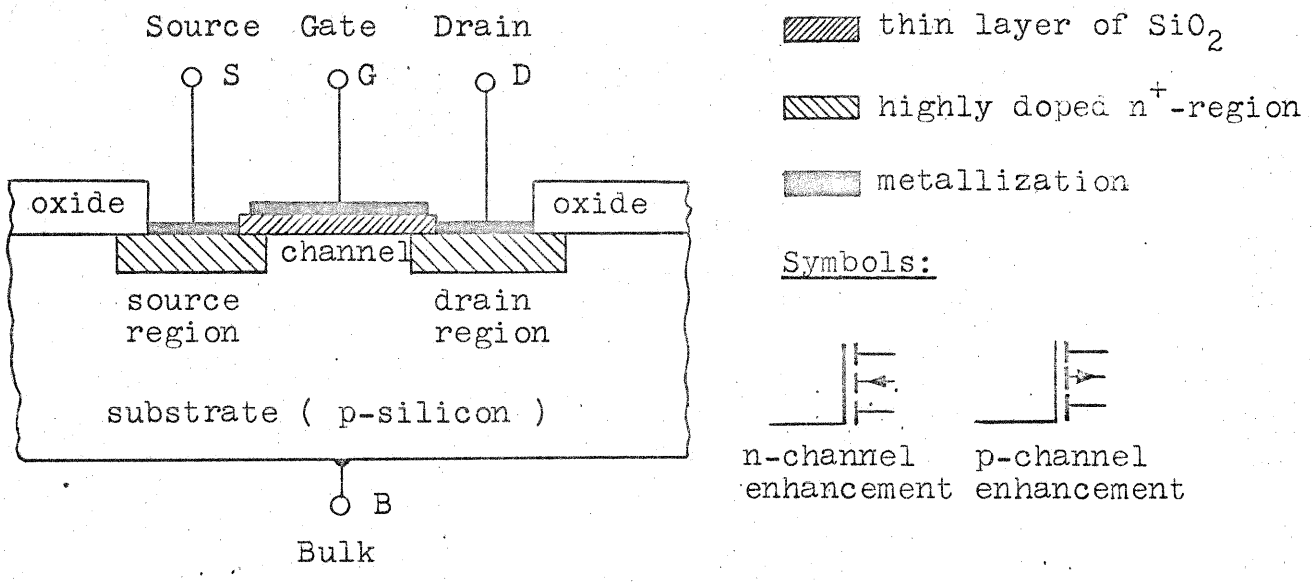


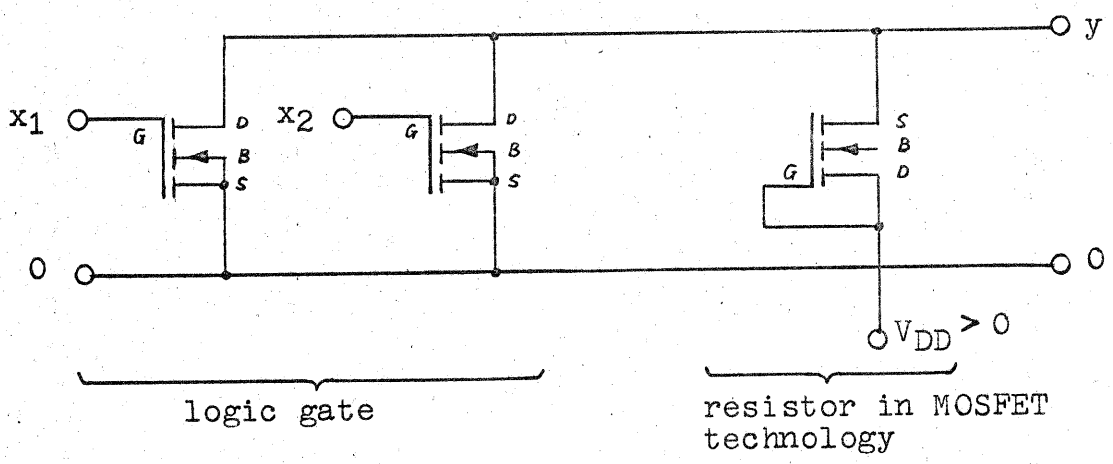
Fig. 12: Cross-section of a n-channel enhancement type Metal-Oxide-Silicon Field-Effect-Transistor (MOSFET)

source and drain. Along the channel a very thin silicon dioxide layer is deposited which is connected with the gate (G). The silicon dioxide layer acts as a dielectric of a capacitor which one electrode is the gate and the other electrode is the channel region.

At zero gate-to-source voltage only few carriers are available for conduction. Source and drain form back-to-back diodes. The drain-to-source current is approximately zero. When the gate-to-source voltage is increased charges are induced near the silicon dioxide dielectric which form an ohmic path between source and drain. The drain-to-source current increases rapidly.

The working of the p-channel enhancement type MOSFET is similarly. At zero gate-to-source voltage the channel is non-conductive. When a negative gate-to-source voltage is applied the drain-to-source current increases.

In fig. 13 a simple example of a MOSFET logic is shown [11] . The whole NOR gate is built only from n-channel enhancement type MOSFETs.



Positive logic: $y = \overline{x_1 + x_2}$ NOR gate

Fig. 13: MOSFET Logic (MOSFETL)

MOSFET digital integrated circuits can be fabricated by a quite similar planar silicon process as described above for bipolar devices. The fabrication requires fewer process steps but must be of better cleanliness than for the bipolar process.

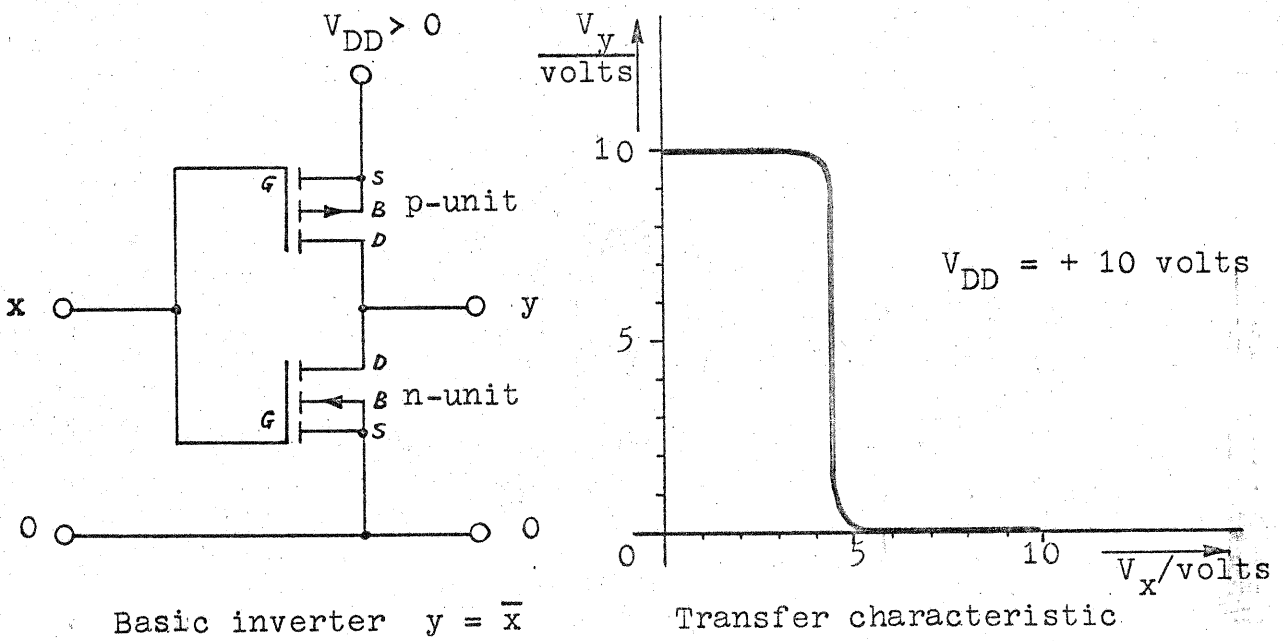
The basic advantages of MOSFET logic are:

- transistors, resistors, capacitors, and diodes can be made by the same technology
- fabrication process needs fewer steps
- very large scales of integration can be achieved (today more than 600 MOSFET elements per mm^2)
- direct coupling
- propagation delay about 40 ns.

As disadvantages we state a higher power supply voltage and a low dynamic fan-out (current-driving) because of the low transconductance. The static fan-out of MOSFET elements, however, is very high.

3.6 Complementary-Symmetry MOSFET Logic (COSMOSFETL)

This logic family is part of the greater group of Complementary-Transistor Logic (CTL), which has been suggested for bipolar transistors some years ago. By combining pnp and npn transistors high circuit speed and high noise immunity levels can be achieved. For application of that principle to unipolar devices both n-channel and p-channel enhancement type MOSFETs are combined. In fig. 14 the basic inverter circuit is shown [8].

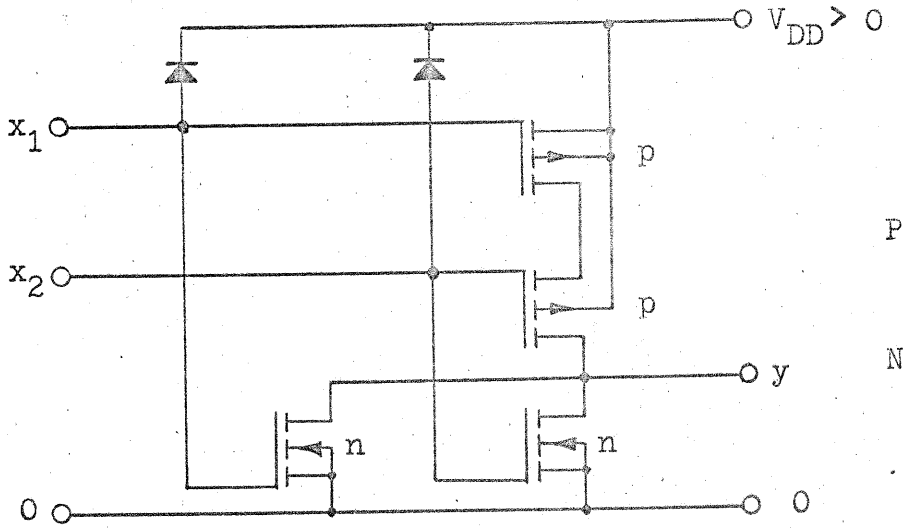


Basic inverter $y = \overline{x}$ Transfer characteristic

Fig. 14: Complementary-Symmetry MOSFET Logic (COSMOSFETL)

When the input voltage is at zero level the p-unit is ON and the n-unit is OFF. Then at the output we have the high level V_{DD}. When the input is at high level the n-unit is ON and the p-unit is OFF. Then the output is at zero level. By this an inverter gate is realized with the property that in each state one transistor is non-conductive. The power consumption of that gate is therefore extremely low. The realization of the different logic functions as well as flip-flops is based on this basic inverter gate.

In fig. 15 an example of a NOR gate in COSMOSFETL is given. The realization of storage elements is achieved by feedbacked logic gates as shown below.



Positive logic:

$$y = \overline{x_1 + x_2}$$

NOR gate

Fig. 15: NOR gate in COSMOSFETL

The most striking advantages of this circuit family are:

- all advantages of MOSFETL
- very sharp transfer characteristic
- upto 45 % noise immunity
- equal logic levels of input and output
- compatibility with other logic families
- extremely low power dissipation (some pW per gate !)
- extremely high input impedance (10^{12} ohms)
- 20 - 30 ns propagation delay
- high static fan-out capability
- wide variations of power supply voltage (6 to 14 volts).

The COSMOSFET logic family is since 1968 on the market. Fully integrated many stage counters, shift registers, non-destructive-readout memories and several types of logic circuits and flip-flops within one package are available.

For a more detailed discussion of the COSMOSFET logic family see [8], [12].

In a short annex we want to point to the realization of storage elements (flip-flops). In fig. 16 the basic configuration of a clocked storage element is shown. The flip-flop circuit con-

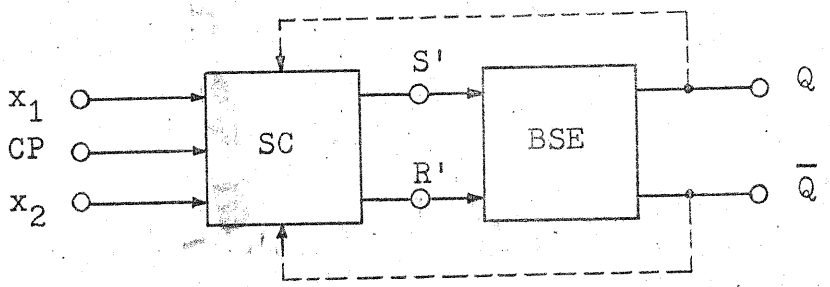
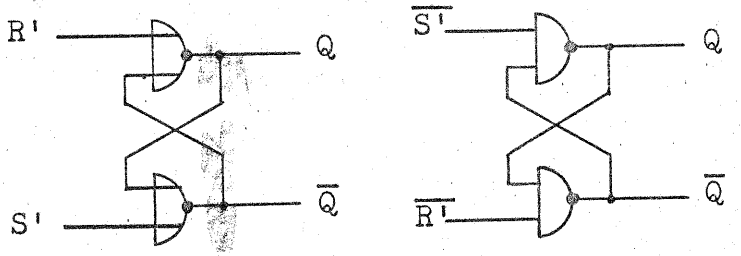


Fig. 16: Basic configuration of a clocked flip-flop

tains a basic storage element (BSE), which has two stable states, and a steering circuit (SC), which sets the BSE according to the input information x_1 and x_2 dependent on the clock pulse (CP).

The BSE can be realized by two feedbacked NOR or NAND gates. In fig.17 both realizations are shown together with the truth table.

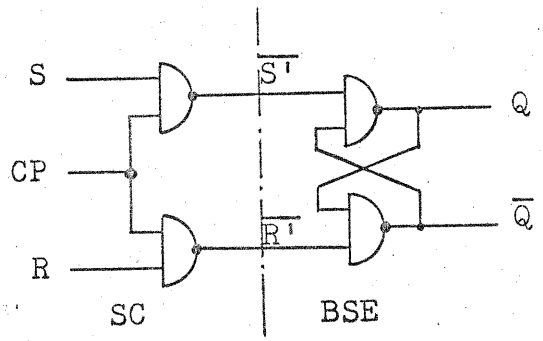


truth table

S'^n	R'^n	Q^m	time
0	0	Q^n	m > n
1	0	1	
0	1	0	
1	1	irregular	

Fig. 17: Realizations of the basic storage element (BSE)

In fig. 18 an example of a clocked flip-flop is given with the logic function of a SR flip-flop. Such types of flip-flops are



truth table

S^n	R^n	Q^{n+1}
0	0	Q^n
1	0	1
0	1	0
1	1	irregular

Fig. 18: Staticizor SR flip-flop

called staticizor, because the flip-flop can be set during the whole phase when the clock pulse is at logic "1". In general, staticizors cannot be used for synchronuous applications such as synchronuous counters or shift registers. For such applications two staticizors are combined to a master and a slave of the flip-flop, respectively. The master-slave principle is shown in fig. 19.

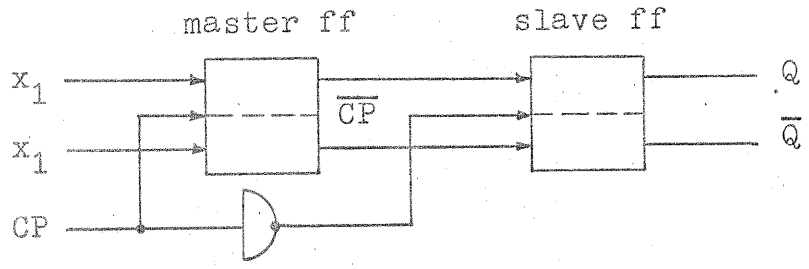
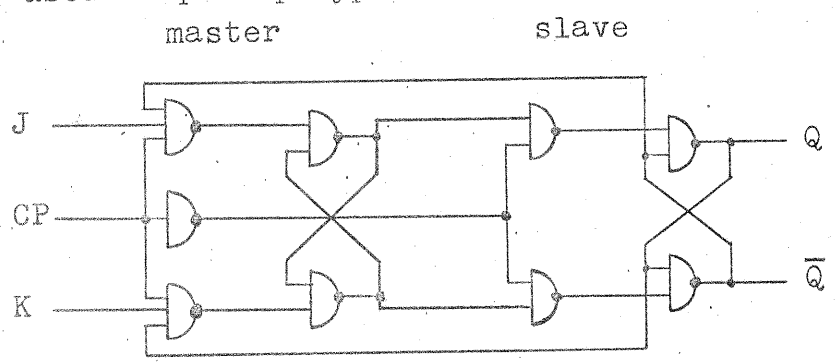


Fig. 19: Master-slave principle

When the clock pulse is "1" the input information is taken into the master flip-flop. During this phase the clock input of the slave is at "0" and therefore the slave does not take the information from the master. When the clock pulse is at "0" the master flip-flop is blocked and the slave flip-flop takes the information from the master flip-flop. Such arrangements can be used for chain circuits as in counters and shift registers.

To get the most general flip-flop type additionally the output of the flip-flop must be feedbacked to the steering circuit SC, as shown in fig. 16. A well known flip-flop of this type is the JK flip-flop which is shown with its truth table in fig. 20. Today, the JK master-slave flip-flop is the most used flip-flop type.



truth table

J^n	K^n	Q^{n+1}
0	0	Q^n
1	0	1
0	1	0
1	1	$\overline{Q}^n$

Fig. 20: Master-slave JK flip-flop

4. OUTLOOK TO NEW TECHNOLOGIES AND NEW FIELDS OF APPLICATION

Above we have discussed the main families of digital integrated circuits. A lot of new technologies were suggested during the last years. Some of these circuits are still in development, others have been given up. Some of those new developments shall be addressed briefly.

For some applications it seems advantageous to combine unipolar devices with bipolar devices. As an example for an amplifier the high input impedance of a MOSFET can be combined with a npn power transistor at the output.

Another example is the production of large scale integrated active memories. The main problem in this development is the power dissipation. The storage cells can be realized, for example, by a bipolar transistor flip-flop. These flip-flops, however, need continuous current to store the information (this is not necessary for magnetic storage cells). Therefore, power dissipation is high. New developments use two different modes for the storage cells to reduce power dissipation. The majority of the cells is in low-power stand-by mode, while the addressed cells are powered-up. An example for such storage cells and their organization is given in [1].

Another proposal for active memories [1] uses COSMOSFET flip-flops as storage cells which have very low power dissipation. The disadvantages are comparatively low speed and low current-driving capability. Therefore, it has been proposed to perform the COSMOSFET storage cells by bipolar support circuits.

Another group of new integrated circuits are the gallium-arsenide devices. They are a combination of a laser-diode made from gallium-arsenide which emits light to a photosensitive pn-junction. This pn-junction is connected with an integrated amplifier The fabrication process of those devices, however, is not yet simple to handle.

The latest integrated circuit technology, announced in [13], is the bipolar planar germanium technology. On a p^+ subcollector p-type germanium is epitaxially grown. Emitter (collector) and base are formed in a single operation by evaporating metals doped

with n- and p-type impurities on the epitaxial layer. During a subsequent heating, these dopants diffuse out of the metal at different rates and form the emitter (collector) and base, respectively. This technology is called the post-alloy diffusion process. The high carrier mobility in germanium and germanium's better high-frequency performance at a temperature of $-100^{\circ}C$ cause that such circuits have a propagation delay of only 150 picoseconds. These circuits must be densely packed on very small chips so that signal delays on the interconnection lines are in the same magnitude as the propagation delay time. Such integrated circuits will be applied to the ultra-high-speed time-sharing computers of tomorrow.

The progress of semiconductor technology goes still on. The future will prove what extent of integration and what circuit speed are possible.

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