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TDM Versus SDM Switching Arrays—Comparison

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Abstract—**In the first paper at the 9th ITC [8], PCM (TDM) switching arrays having up to six stages and up to about 100 000 terminations were investigated with regard to their standardized costs per termination as a function of the cost ratio "gate to memory-bit."**

In this context, the following were considered:

- **the influence of the number and sequence of stages (*T*-stages, *S*-stages),**
- **the number of terminations,**
- **the degree of multiplexing (30, 120 time slots per multiplex line).**

Furthermore, new PCM charts for the quick design of economic PCM switching arrays were developed.

The second paper completes these studies by comparisons between PCM switching arrays and their equivalent SDM switching arrays. Handy formulas for the best possible economic design of PCM and SDM arrays, respectively, are presented and derived.

The loss versus the carried traffic of PCM arrays having $S = 3$ up to six stages and with $M = 30$ and 120 time slots per highway are compared with each other and with equivalent SDM link systems.

Furthermore, the relative costs per termination are calculated for these PCM and SDM array structures and drawn versus the size of these arrays.

I. INTRODUCTION

As mentioned in the abstract, this paper completes the extensive PCM array investigations in [8]. The rapid decrease of costs for digital switching components makes it worthwhile to compare SDM and PCM switching arrays with each other. As a basis of such comparisons, PCM switching arrays, as well as their equivalent SDM switching arrays, have to be designed optimally, i.e., as cost saving as possible.

Section II presents two different sets [boundary conditions 1) and 2)] of design formulas for "optimal" SDM and PCM switching arrays, respectively, based on two different boundary conditions.

In Section III the traffic behavior, i.e., the point-to-point loss B_{PP} versus the carried traffic per termination is discussed for such least-cost PCM and equivalent SDM structures.

In Section IV the standardized costs per termination (CPT) are considered under various assumptions for the costs of metallic 4-wire crosspoints on the one side and for gates and memory-bits on the other side. They are calculated for switching arrays having $S = 3$ to six stages and up to about 100 000 terminations. A traffic of 0.8 Erlangs per termination and a point-to-point loss of 0.1 percent are fixed parameters of these graphs.

In Section V the design formulas of type 1 and type 2 are derived for both SDM and PCM arrays.

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II. FORMULAS FOR THE COST SAVING DESIGN OF SDM AND PCM SWITCHING ARRAYS

A. General Remarks

The formulas being discussed in this section, and being derived in the annex, hold for the structural parameters of switching arrays in cases of many operation modes, namely, for

1) two-sided arrays with unidirectional or bidirectional traffic flow;

2) 4-wire arrays with unidirectional traffic flow "from left to right," using one 4-wire array or two "separated" parallel arrays (one array per speech direction); and

3) 4-wire arrays with "combined" switching (PCM or SDM) of bidirectional traffic through one unidirectionally operated array.

As far as the expression "termination" is used, note that *one* termination always includes, in the case of 4-wire switching, *both* speech directions which belong to one speech connection (cf. [7]).

In deriving such formulas for least-cost switching array structures, this paper starts from two different boundary conditions. This holds for SDM arrays as well as for PCM (TDM) arrays. The basic idea of these two boundary conditions [named boundary conditions 1) and 2)] shall first be explained briefly by means of a symmetrical two-sided SDM link system.

Another two methods for the structural design of "crosspoint minimal" switching arrays are mentioned in Sections II-H and II-I. The reasons why their application is not suitable here are explained.

B. Boundary Condition 1)

Design a two-sided link system having S stages and N outlets per side (i.e., $= 2N$ terminations). Furthermore, a "single linkage" (SL) structure is desired (cf. Fig. 1, Section V-A).

Condition 1) prescribes for SDM arrays that the desired crosspoint saving structure has the smallest possible requirement of crosspoints per line (trunk, inlet, respectively).

$$\mathrm{CPL} = k_1 + \beta(k_2 + \cdots k_j + \cdots k_S) \tag{1}$$

where

$$\beta = \frac{k_1}{i_1} = \frac{i_S}{k_S}$$

means the "expansion factor" for the multiples i_1 /k_1 in stage 1.

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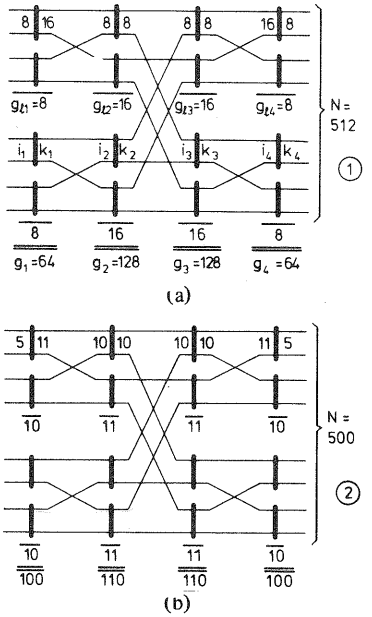

Fig. 1. (a) Four-stage array, mode SDM 1. (b) Four-stage array, mode SDM 2.

Hereby, the transparency function

$$T = \prod_{j=1}^{S-1} k_j(1 - a_{j+1}) \cdot k_S \tag{2}$$

is assumed to have a constant value, as a boundary condition for the derivation of the design formulas. In (2) k_j means the number of outlets per multiple in the stages 1, 2, ···, j, ···, $S - 1$; and a_{j+1} denotes the carried traffic per link from a stage j to $(j + 1)$.

The design formulas derived with this boundary condition have already been applied in [2] as well as for the "NIK charts" [5]. They allow the quick design of crosspoint saving SDM link systems. These formulas are listed in Table I (part SDM 1). As to the derivation, see Section V. More details can be found in [7].

C. Boundary Condition 2)

Condition 2) for SDM switching arrays does not use the "transparency condition" according to (2). Instead, one starts from the desired number N of inlets (outlets) per side. Regarding the above mentioned condition of a "single-linkage structure" (SL) these N inlets per side can be accessed from "the midst" of the symmetrical switching array (cf. Fig. 1), if

$$N = \prod_{j=1}^{[S/2+1]} i_j . \tag{3}$$

The notation $[S/2 + 1]$ means the next lower integer value, e.g., for $S = 4$ as well as for $S = 5$, it holds that $[S/2 + 1] = 3$. The design formulas based on boundary condition 2) are listed in Table I, part SDM 2. As to the derivation, see Section V-D.

TABLE I

SDM 1	SDM 2
S ≥ 2:	S = 2: like SDM 1
$i_j = \sqrt[[S_2+1]]{N}$ $j=1...S-1$	S = 3:
$k_j = \sqrt[[S_2+1]]{N}$ $j=2...S$	$i_1=k_3=\sqrt[2]{N/2}$
$k_1=i_S=\beta\cdot i_1 \geq k_j$	$i_2=k_2=\sqrt[2]{2\cdot N}=2\cdot i_1$
	$k_1=i_3=\beta\cdot i_1$
	S = 4:
	$i_1=k_4=\sqrt[3]{N/4}$
	$i_2=k_2=i_3=k_3=\sqrt[3]{2\cdot N}=2\cdot i_1$
	$k_1=i_4=\beta\cdot k_1$

D. Example for the Use of the Formulas Sets SDM 1 and SDM 2

Design a two-sided SDM array having S = four stages and $N \approx 500$ inlets (outlets) per side (cf. Fig. 1). Furthermore, $B_{PP} \approx 0.15$ percent is desired for a carried traffic $Y/N = 0.8$ Erlangs per termination. *The SDM 1 formulas yield*

$$i_j = \sqrt[[S/2+1]]{N} = \sqrt[3]{500} \approx 8, \text{ i.e.,}$$

$$i_1 = i_2 = i_3 = k_2 = k_3 = k_4 = 8.$$

Therefore, finally $N = i_j^3 = 512$.

Furthermore, $k_1 = i_4$ is obtained by an iterative loss calculation such that the desired point-to-point loss B_{PP} is achieved, e.g., for $B_{PP} \approx 0.15$ percent one obtains $k_1 = i_4 = 16$, i.e., an expansion factor $\beta = k_1/i_1 = 2$ is necessary.

The number of crosspoints per line (CPL) (trunk, inlet, respectively) amounts to CPL = 64, i.e., 32 per termination. *The SDM 2 formulas yield*

$$i_1 = k_4 = \sqrt[3]{\frac{N}{4}} = 5$$

and

$$i_2 = i_3 = k_2 = k_3 = \sqrt[3]{2 \cdot N} = 10.$$

Therefore, one obtains $N = i_1 \cdot i_2 \cdot i_3 = 500$.

If, again, $B_{PP} \approx 0.15$ percent is prescribed, $k_1 = i_4$ is determined as above by iteration. One gets $k_1 = i_4 = 11$, i.e., an expansion factor $\beta = 2.2$ [see Fig. 1(b)] and one requires CPL = 66 crosspoints per line (trunk, respectively), i.e., 33 per termination.

Fig. 2 shows the loss B_{PP} versus the carried traffic Y/N per termination for both arrays. The loss curves lie very close to each other.

The array 1) according to the mode SDM 1 has a slightly steeper increase of loss due to the somewhat smaller crosspoint requirement and consequently better link efficiency.

The small difference in the crosspoint requirement according to calculation mode SDM 1 and SDM 2, respectively, has

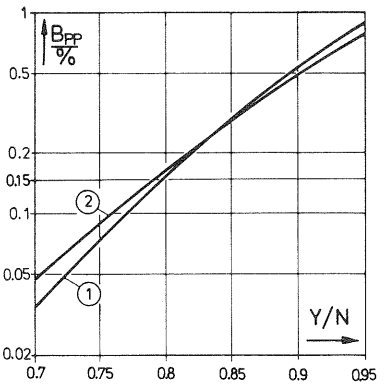

Fig. 2. Probability of loss.

been found also for many other examples. Whether mode SDM 1 or SDM 2 yields slightly more or less CPL can also depend on rounding effects.

However, it is typical that the design mode SDM 2, which does not regard *a priori* a prescribed transparency, results in a slightly greater necessary expansion factor β in stage 1) (here $11/5 = 2.2$ instead of $16/8 = 2.0$).

E. Boundary Conditions 1) and 2) Applied to PCM Switching Arrays

Here only the structure of the multiplex link lines within a PCM switching array need be considered and not the structure of the individual link paths as in an SDM link system.

According to the same basic ideas as for SDM 1 and SDM 2, one obtains the formula sets PCM 1 and PCM 2, respectively, for gate minimal arrays. In contrast to SDM switching systems one has to distinguish here between switching arrays of various sequences of time and space stages.

Table II contains the formulas for the design modes PCM 1 and PCM 2. The methods PCM 1 and PCM 2 differ only in the case of switching arrays with more than two space stages. As to the derivation, see Sections V-C and V-E.

TABLE II

PCM 1	PCM 2
S = 3: TST $h_2=j_2=HW$ $M^*=\beta\cdot M$	S = 3: TST, STS S = 4: TSST like PCM 1
S = 3: STS $h_1=j_3=HW$ $j_1=h_3=\beta\cdot h_1$	S = 5: TSSST $h_2=j_2=h_4=j_4=\sqrt[2]{HW/2}$ $h_3=j_3=2\cdot h_2$ $M^*=\beta\cdot M$
S = 4: TSST $h_2=j_2=h_3=j_3=\sqrt[2]{HW}$ $M^*=\beta\cdot M$	S = 5: SSTSS like PCM 1 (only 2 space stages contribute to the HW-access)
S = 5: TSSST $h_2=j_2=h_3=j_3=h_4=j_4=\sqrt[2]{HW}$ $M^*=\beta\cdot M$	S = 5: STSTS $h_1=j_5=\sqrt[2]{HW/2}$ $h_3=j_3=2\cdot h_1$ $j_1=h_5=\beta\cdot h_1$
S = 5: SSTSS $h_1=h_2=j_2=h_4=j_4=j_5=\sqrt[2]{HW}$ $j_1=h_5=\beta\cdot h_1$	S = 6: TSSSST $h_2=j_2=h_5=j_5=\sqrt[3]{HW/4}$ $h_3=j_3=h_4=j_4=2\cdot h_2$ $M^*=\beta\cdot M$
S = 5: STSTS $h_1=h_3=j_3=j_5=\sqrt[2]{HW}$ $j_1=h_5=\beta\cdot h_1$	S = 6: STSSTS $h_1=j_6=\sqrt[3]{HW/4}$ $h_3=j_3=h_4=j_4=2\cdot h_1$ $j_1=h_6=\beta\cdot h_1$
S = 6: TSSSST $h_2=j_2=h_3=j_3=h_4=j_4=h_5=j_5=\sqrt[3]{HW}$ $M^*=\beta\cdot M$	
S = 6: STSSTS $h_1=h_3=j_3=h_4=j_4=j_6=\sqrt[3]{HW}$ $j_1=h_6=\beta\cdot h_1$	

F. Examples for the Use of Design Modes PCM 1 and PCM 2

1) *Five-Stage TSSST PCM Array:* Fig. 3 shows two five-stage PCM switching arrays of the type TSSST with $N \approx 1500$. The array in Fig. 3 is designed according to mode PCM 1. The values in parentheses hold for the design according to mode PCM 2.

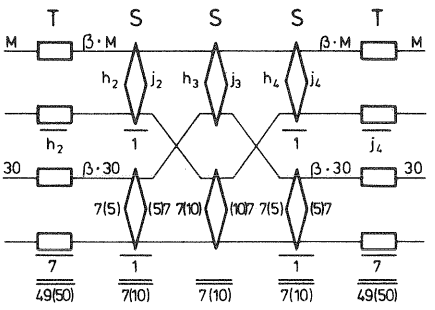

Fig. 3. TSSST array, modes PCM 1, PCM 2.

For both arrays the design modes consider here only the three space stages in the middle and their matrices.

The mode PCM 1 yields, for 49 multiplex lines (ML) per side of the array, uniform matrices with $h_2 = j_2 = h_3 = j_3 = h_4 = j_4 = 7$. These 49 ML's correspond to $N = 49 \cdot 30 = 1470$ speech paths.

The mode PCM 2 yields two different matrix sizes, namely, $h_2 = j_2 = h_4 = j_4 = 5$ and $h_3 = j_3 = 10$. Therefore, 50 ML's are connected to the TSI's of the T-stages on both sides.

The fact should be focused upon that an expansion between inlets and outlets of the first stage (and a corresponding concentration in the last stage) is performed in both cases only by increasing the number of "internal time slots" per internal multiplex line (ML). The number of ML's and the size of the matrices remain constant.

Fig. 4 shows diagrams for these two TSSST arrays. In the diagrams on the left-hand side, the point-to-point loss B_{PP} is prescribed with 0.1 percent or 1.0 percent, respectively. The curves show the necessary expansion β in the first stage versus the carried traffic per termination. (Here β means the ratio

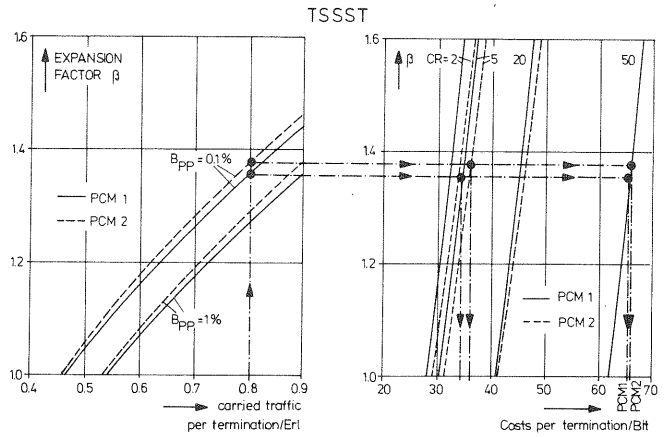

Fig. 4. Comparison of the relative costs of the TSSST array, mode PCM 1, PCM 2.

"internal to external number of time slots" per multiplex line.)

As one can see, the expansion factor β for the type PCM 2 is somewhat greater for all values Y/N. This compensates the fact that the design mode PCM 2 minimizes the gate requirement without regarding the "transparency condition" according to (2).

The right-hand chart yields the corresponding relative costs per termination for each triple $Y/N, \beta, B_{PP}$. The costs of one memory-bit (including its control) are used as the unit for the relative costs. Various cost ratios CR are provided, where

$$CR = \frac{\text{costs per gate}}{\text{costs per memory-bit}}. \tag{4}$$

The marked example gives for $Y/N = 0.8$ Erlangs and for $B_{PP} = 0.1$ percent the costs for both arrays. In this example, the array according to PCM 1 is slightly cheaper than that one designed with mode PCM 2. The difference decreases as the cost ratio CR increases.

2) *Six-Stage TSSSST PCM Array:* As a further example, a six-stage array is considered. It is designed according to the two modes PCM 1 and PCM 2, respectively.

Here 125 and 108 highways, respectively, were chosen, leading to optimal, i.e., gate minimizing, arrays [see Fig. 5(a) and (b)].

The diagram, being analogous to Fig. 4, is presented in Fig. 6. Here, too, the necessary expansion β is greater for the PCM array designed according to mode PCM 2. Its resulting relative costs per termination are slightly smaller in this case.

Regarding the small differences of costs, as well as the advantage of uniform matrices in all space stages, the following sections will consider only switching arrays being designed according to mode SDM 1 and PCM 1, respectively.

G. Remarks on the Application of the Design Formulas to 4-Wire Arrays Using Combined or Separated Switching

The operating principles for combined or separated switching, respectively, have been explained in detail in the first paper [8].

The design formulas are applicable for both array types. However, one has to consider that a combined switching array

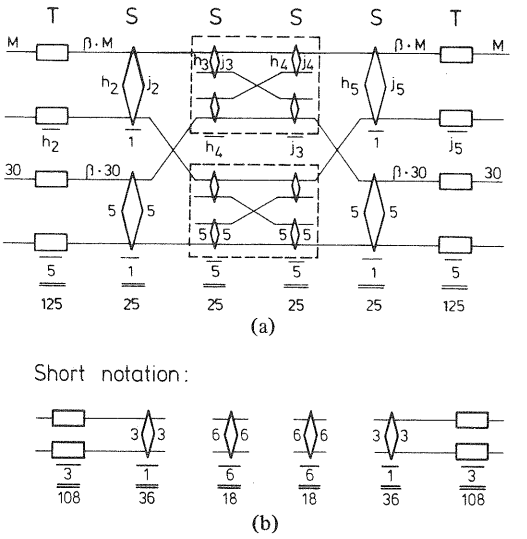

Fig. 5. (TSSSST array, mode PCM 1. (b) TSSSST array, mode PCM 2.

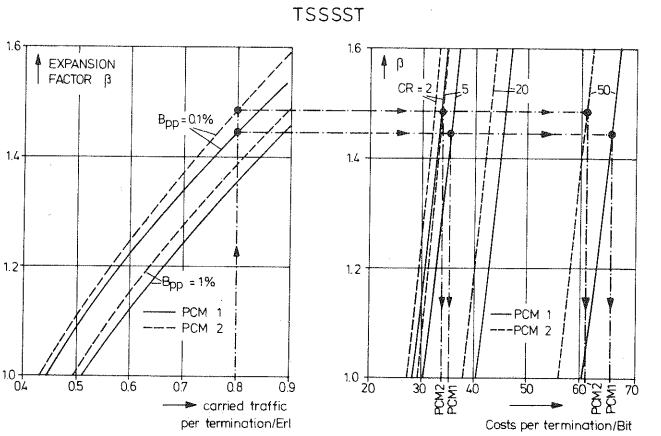

Fig. 6. Comparison of the relative costs of the TSSSST array, mode PCM 1, PCM 2.

having N 4-wire terminations allows a maximum of $N/2$ simultaneous 4-wire connections.

In contrast to this an array for separated 4-wire switching having N inlets and N outlets (i.e., 2 N terminations) allows a maximum of N simultaneous connections "from left to right."

Without regard to these different traffic capacities, both array types can equally be designed using the same formula.

H. Overall Cost Optimization of PCM Switching Arrays

A further method for designing an "optimal" PCM switching array is to minimize the costs of gates and speech memories *and* the respective control memories as a whole. This can be done by differentiating the *overall* cost formula of a PCM switching array with respect to the inlets and outlets of the space switches. Also this principle is applicable for PCM arrays having three and more space stages (like method PCM 2). The design for arrays with less than three space stages is already determined by the demand of a symmetrical structure.

This overall cost optimization was applied to all PCM arrays having more than two space stages. Here, the minimum costs depend on the size of the space switches *and* their respective

control memories; the number of the time-slot interchanges (TSI) of the T-stages has no influence.

The result is, that the difference of the costs between only gate minimal arrays and overall least-cost arrays is negligible.

There are two reasons:

1) Strictly optimal values for the size of the space switches and the control memories can normally not be observed, because only integer values of inlets h and outlets j can be realized. The same holds for the memory-bits per storage place. Therefore, the practical realization is generally more expensive than the theoretical cost minimum.

2) Overall cost minimization generally yields smaller space switches in the first S-stage than even the gate minimal solution (mode 2). As a rule, the expansion factor therefore has to be remarkably increased in order to achieve a prescribed high grade of service. Consequently, the costs increase and the desired savings may again be compensated.

Overall cost minimization has been checked for many PCM arrays. The result was always as described above. Therefore, this third optimization principle will not be applied.

I. The Optimum Link (CPE) Method [1]

This method for the structural design of SDM link systems yields the utmost minimum requirement of crosspoints per Erlang for SDM link systems with prescribed transparency T according to (2). However, the condition of a "single linkage" (SL) structure, as required here, cannot be observed. (Details are discussed in [7].)

III. LOSS VERSUS CARRIED TRAFFIC

A. General Remarks

In this section PCM switching arrays of the types TST, TSST, TSSST, SSTSS, and TSSSST are considered. The loss B_{PP} versus the carried traffic per inlet is drawn for PCM arrays being designed according to the mode PCM 1 and assuming $M = 30$ or 120 time slots per multiplex line (ML).

Furthermore, equivalent SDM systems designed according to mode SDM 1 with a minimum requirement of crosspoints per termination are presented. Interleaved wiring is applied for SDM arrays having $S > 4$ stages. The selected arrays consider smaller systems with $S = 3$ stages, medium ones with $S = 4$, and larger ones with $S = 5, 6$ stages.

For all examples the characteristic traffic per inlet is assumed to be 0.8 Erlangs. All arrays were expanded individually such that a point-to-point loss probability (one attempt only) in the range of $B \approx 0.1$ percent was achieved. The loss curves have been checked by simulation runs.

B. Results

The loss differences between equivalent SDM and PCM arrays result only from two reasons:

1) the necessity to have an integer number of inlets/outlets per stage;

2) the different sizes of the first stage multiples cause different link loads for a certain loss; the higher the link load is, the steeper is the increase of loss.

This is evident for all $T \cdots T$ arrays, with $M = 120$ time slots per multiplex line. They have the steepest increase of loss because the internal TS carry a high traffic load (Figs. 7-9 and 11). This means that the sensitivity against overload is greater. On the other hand, a solution with $M = 120$ time slots per ML will often be cheaper (cf. Section IV).

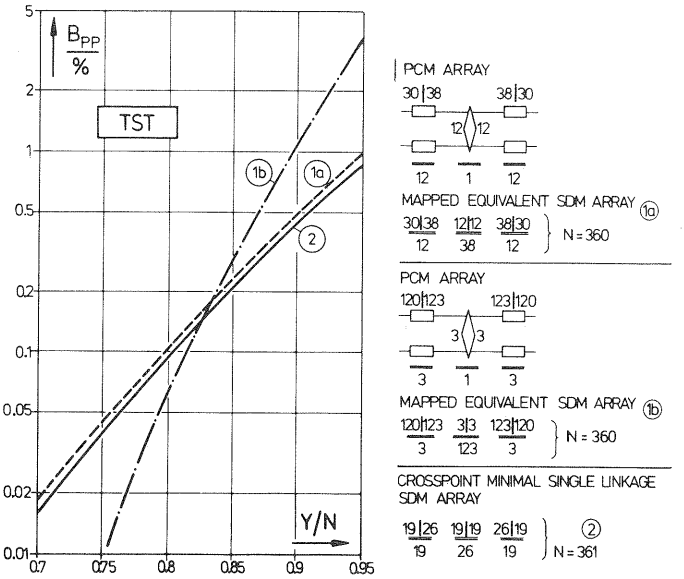

Fig. 7. Point-to-point loss versus the carried traffic per termination for three-stage PCM and equivalent SDM arrays.

In Fig. 10 the SDM array has larger first stage multiples than the corresponding PCM arrays (SSTSS). Consequently, this SDM array has the better link efficiency and therefore, the steepest increase of loss versus the carried traffic.

In Fig. 9 the curves for SDM arrays are shown having a first stage expansion of 15|19 and 15|20, respectively. The desired point 0.8/0.1 percent lies in between. The same holds for the curves (2a) and (2b) in Fig. 11 where the two SDM systems have an expansion 9|14 and 9|15, respectively.

IV. COSTS PER TERMINATION

A. General Remarks

The diagrams in Figs. 12-17 show the (standardized) costs per termination (CPT) for SDM and PCM switching arrays. Both types have a carried traffic $Y/N = 0.8$ Erlangs per termination and a point-to-point loss $B_{PP} = 0.1$ percent (one attempt) as fixed diagram parameters. The curves for the PCM arrays are based on a cost ratio "gate to memory-bit" of $CR = 5$. One cent (U.S. currency) per memory-bit can be assumed to be a reasonable price for the time being, if the costs for the control of the memories are included.

For SDM 4-wire systems the costs per 4-wire crosspoint are assumed to lie between \$1 and \$5 (U.S. currency), i.e., a relative price of about 100-500 compared with 1 memory-bit. If, e.g., 30 crosspoints per termination were required, with a cost of \$2 each, the diagram would show standardized costs of 6000 per termination.

Regarding this very high price relation between metallic crosspoints and memory-bits, one has to consider that PCM systems cause a lot of additional costs per termination which cannot simply be included into these diagrams!

These additional costs result among others from higher

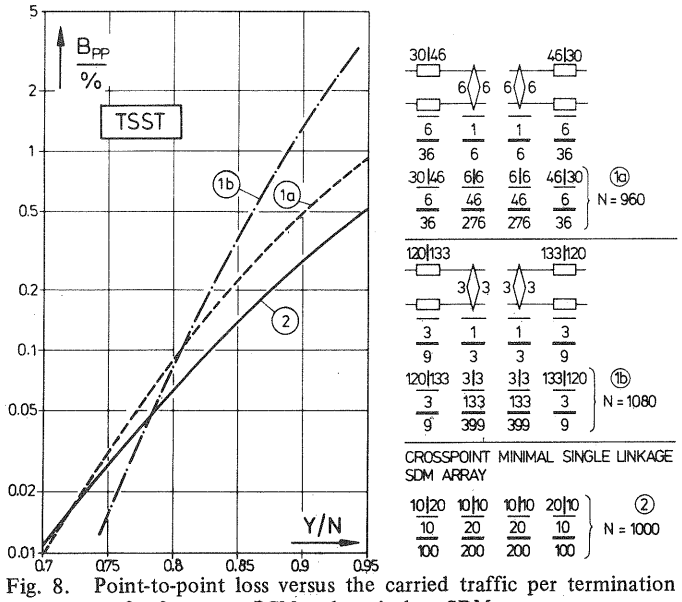

Fig. 8. Point-to-point loss versus the carried traffic per termination for four-stage PCM and equivalent SDM arrays.

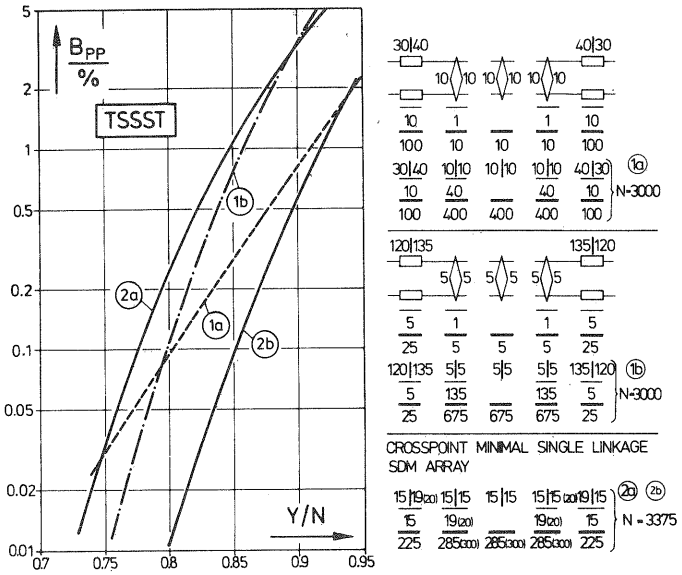

Fig. 9. Point-to-point loss versus the carried traffic per termination for five-stage PCM and equivalent SDM arrays.

peripheral costs, such as the BORSHT functions, the codec's, etc.

B. Results

The six diagrams deal with the following PCM array types: TST, STS, TSST, TSSST, SSTSS, and TSSSST. They show the relative costs per termination (CPT) in the unit "bit" versus the number N of terminations of the system (N = 600 ··· 20 000 ··· 100 000). In all diagrams the least expensive SDM arrays are based on a price per metallic crosspoint of 100, 250, 500 bits (see curves 1, 2, and 3).

The least expensive PCM arrays (CR = 5) are drawn for a realization with M = 30, 120 time slots per multiplex line, and for separated switching (see curves 4 and 5).

The significant results of Figs. 12-17 can be summarized as follows.

1) In any case PCM switching arrays have much lower costs per termination than SDM switching arravs.

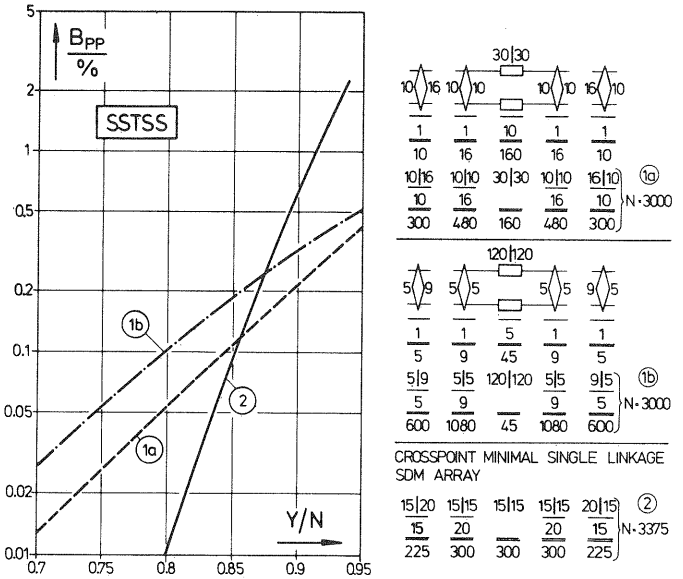

Fig. 10. Point-to-point loss versus carried traffic per termination for five-stage PCM and equivalent SDM arrays.

2) Switching with M = 120 TS per ML instead of M = 30 TS (i.e., serially with 8 Mbits/s) leads to a decrease of CPT of about 10 to 30 percent referred to the pure switching array costs.

3) The compared SDM switching arrays show a significant decrease of CPT as the number of stages increases.

4) PCM arrays having three stages compete with arrays having $S \geqslant$ four stages as long as the number of terminations does not exceed $N \approx 3000$ (with M = 30). Using M = 120 TS per ML, three-stage arrays up to at least 20 000 terminations may still be economic.

5) PCM arrays with four to six stages do not have significantly different costs per termination. However, the complexity of path allocation and central control increases with the number of stages.

Therefore, the rule of thumb for the economic design of PCM switching arrays reads: choose a small number of stages combined with a high number of time slots per multiplex line.

APPENDIX

DERIVATION OF THE DESIGN FORMULAS FOR CROSSPOINT OR GATE SAVING SDM AND PCM SWITCHING ARRAYS

A. Prerequisites

As prerequisites for the design modes hold:

- the arrays are symmetrically structured (I)
- expansion and the corresponding concentration are performed in the first and the last stage, respectively (II)
- the intermediate stages switch 1:1 (III)
- only structures with "single linkage" (SL) wiring are considered. (IV)

"SL" is defined as follows, e.g., for S = four stages (cf. Fig. 1, and [9]).

$k_1 = g_{12} = g_{13} = i_4$ (width of the connection graph)

$g_{11} = i_2$; $k_3 = g_{14}$

$k_2 = g_3/g_{13} = g_4/g_{14}$; $i_3 = g_1/g_{11} = g_2/g_{12}$.

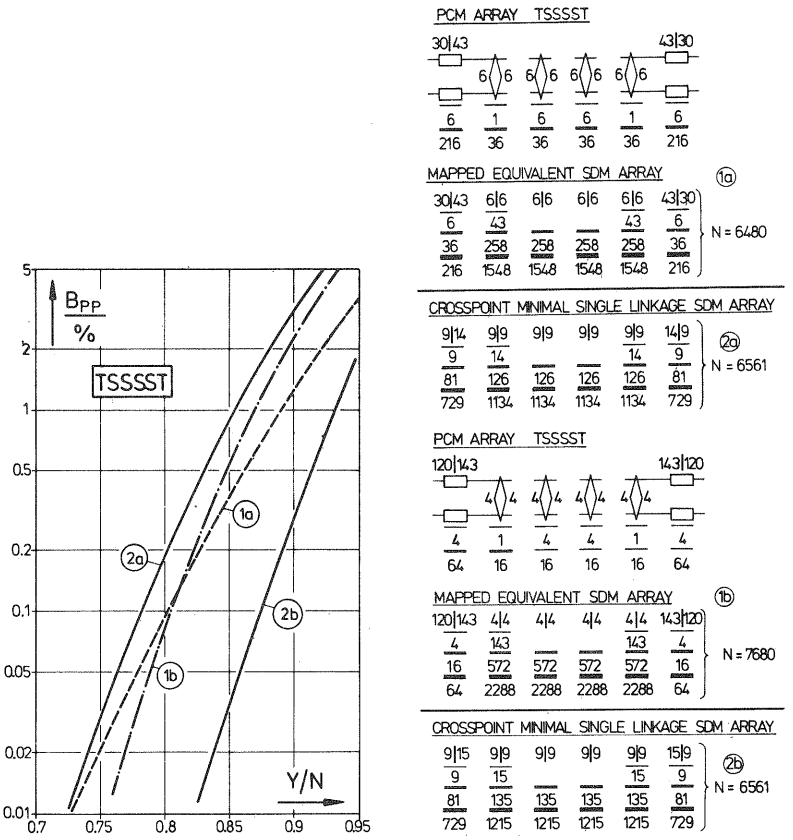

Fig. 11. Probability of loss for the TSSSST PCM array and equivalent SDM arrays.

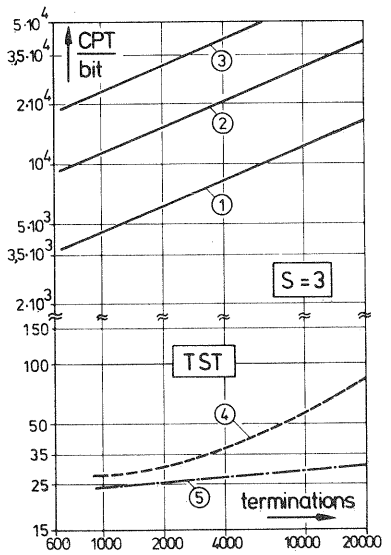

Fig. 12. Cost comparison between three-stage PCM and SDM arrays.

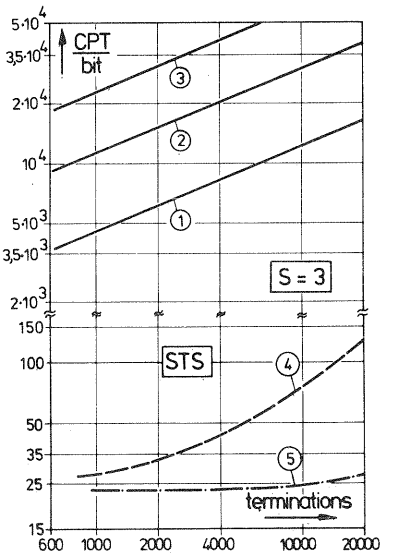

Fig. 13. Cost comparison between three-stage PCM and SDM arrays.

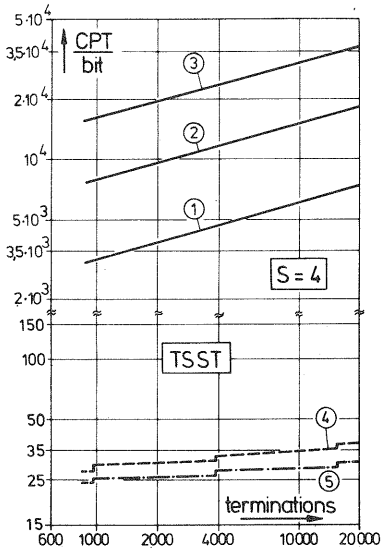

Fig. 14. Cost comparison between four-stage PCM and SDM arrays.

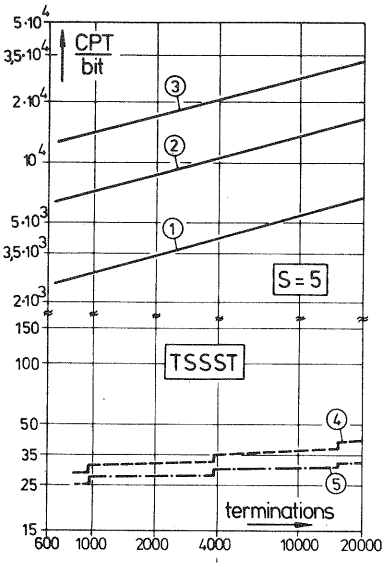

Fig. 15. Cost comparison between five-stage PCM and SDM arrays.

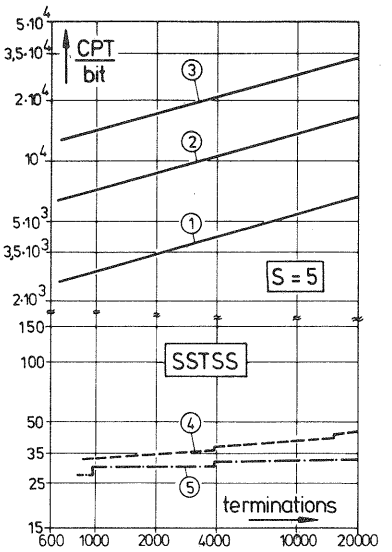

Fig. 16. Cost comparison between five-stage PCM and SDM arrays.

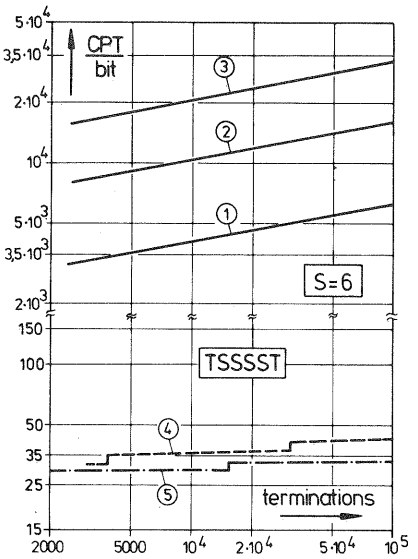

Fig. 17. Cost comparison between six-stage PCM and SDM arrays.

In case of SL wiring, the following formula holds for the number of lines (trunks) per side of a SDM link system.

$$N = \prod_{j=1}^{[S/2+1]} i_j. \tag{A1}$$

B. The Crosspoint Minimization Mode SDM 1

The derivation of the structural parameters i_j and k_j of an SDM switching array has to achieve a minimum number CPL being defined as in (1).

The boundary condition T = constant according to (2) can be simplified, because the carried traffics a_{j+1} per link ($j = 1 \cdots (S-1)$) are the same between all stages and independent of the size of the multiples (see prerequisite III). Hence, (2) can be replaced by the product

$$P = \prod_{j=1}^{S} k_j$$

with

$$k_1 = \frac{P}{\prod_{j=2}^{S} k_j} \tag{A2}$$

and be used as boundary condition. Therefore, the partial derivation of CPL with respect to k_j yields ($j = 2 \cdots S$)

$$\frac{\partial CPL}{\partial k_j} = \frac{-P}{\prod_{j=2}^{S} k_j} \cdot \frac{1}{k_j} + \beta = 0.$$

From this follows

$$k_j = \frac{P}{\prod_{j=2}^{S} k_j} \cdot \frac{1}{\beta}, \qquad j = 2 \cdots S \tag{A3}$$

and

$$i_1 = i_2 = \cdots i_j \cdots = i_{S-1} = k_2 = k_3 = \cdots k_j \cdots = k_S \qquad \text{(A4)}$$

for the assumed symmetrical structures (see prerequisite I).

From the SL condition (A1) and from (A4) follows, for the number of inlets per multiple in stages $1, 2, \cdots j \cdots (S-1)$,

$$i_j = \sqrt[[S/2+1]]{N}. \qquad \text{(A5)}$$

For a certain prescribed total of carried traffic Y of the link system, the traffic per inlet in stage 1) amounts to $a_1 = Y/N$ and the uniform traffic per link between stages 1) and 5) is

$$a_j = a_1 \cdot \frac{i_1}{k_1} = a_1 \cdot \frac{1}{\beta}. \qquad \text{(A6)}$$

Finally, the expansion factor for stage 1) is $\beta = k_1/i_1$ and therefore $k_1 = i_S$ must be determined iteratively, in order to achieve the prescribed probability of point-to-point loss B_{PP} [2].

C. The Gate Minimization Mode PCM 1

Here, the network consists of multiplex link lines between the first and the last stage of a PCM switching array (e.g., see Fig. 2). A minimum requirement of gates in the space stage matrices of a PCM switching array must be achieved. The number of gates per incoming external multiplex line amounts to

$$\text{GPM} = j_1 + \beta(j_2 + j_3 + j_i + \cdots j_S). \qquad \text{(A7)}$$

Again, $\beta = j_1/h_1$ means the expansion factor in stage 1) if an $S \cdots S$ array is considered; elsewhere $\beta = 1$.

Only those stages S must be included into the sum GPM which are *space* stages!

The grade of access from the incoming to the outgoing external ML's via the intermediate ML's and their space matrices depends on the product

$$P^* = \prod_{i=1}^{S} j_i$$

and with

$$j_1 = \frac{P^*}{\prod_{i=2}^{S} j_i}. \qquad \text{(A8)}$$

Only those indexes i (of space stages) must be regarded which contribute to this access "from left to right" or vice versa.

Consider a constant value P^* which must be achieved with a minimum number of GPM.

The partial derivation of GPM with respect to the inlets j of all concerned space matrices leads to a uniform size

$$j_i = h_i. \qquad \text{(A9)}$$

From the known number of HW multiplex lines per side and from the prerequisites III and IV follows (analogously to SDM arrays)

$$h_i = j_i = \sqrt[[S/2+1]]{HW}. \qquad \text{(A10)}$$

D. The Crosspoint Minimization Mode SDM 2

The boundary condition for this mode is the prescribed number of lines (trunks) N to be connected per side of an SDM link system and observing the prerequisite IV. As an example, the derivation is shown for $S =$ four stages. It holds

$$N = i_1 \cdot i_2 \cdot i_3 = k_2 \cdot k_3 \cdot k_4 \qquad \text{(A11)}$$

[see Fig. 1(b)].

Equation (A11) does not include i_4 and k_1, respectively. These values follow from the symmetry condition I, i.e.,

$$k_1 = i_4, \quad \text{and } i_1 = k_4 \qquad \text{(A12)}$$

with prerequisite II $k_1 = \beta \cdot i_1$.

As the same prerequisites I–IV hold, one obtains, with (A12) and (1)

$$\text{CPL} = 2k_1 + \beta \cdot k_2 + \beta \cdot k_3 \qquad \text{(A13)}$$

and with (A12) in (A11)

$$k_1 = \frac{N \cdot \beta}{k_2 \cdot k_3}. \qquad \text{(A14)}$$

Partial derivation $\delta\text{CPL}/\delta k_j = 0$ yields

$$k_2 = k_3 = \frac{2N}{k_2 \cdot k_3} \qquad \text{(A15)}$$

where prerequisite III follows with

$$i_2 = k_2 = i_3 = k_3 \qquad \text{(A16)}$$

with (A14), (A15), and (A12)

$$k_2 = \frac{2}{\beta} \cdot k_1 = 2i_1 \qquad \text{(A17)}$$

with (A11), (A16), and (A17)

$$N = i_1 \cdot k_2 \cdot k_3 = 4 \cdot {i_1}^3 \qquad \text{(A18)}$$

and, hence,

$$i_1 = \sqrt[3]{\frac{N}{4}} \qquad \text{(A19)}$$

with (A17)

$$i_2 = \sqrt[3]{2 \cdot N}. \qquad \text{(A20)}$$

E. The Gate Minimization Mode PCM 2

This mode yields formulas which correspond to those of mode SDM 2; see Table II.

Remark: All above derivations can be found more detailed in the PCM charts [7].

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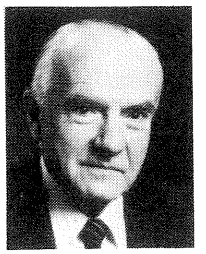

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Klaus Rothmaier, for a photograph and biography, see p. 935 of the July 1981 issue of this TRANSACTIONS.

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Reinhard Scheller, for a photograph and biography, see p. 935 of the July 1981 issue of this TRANSACTIONS.