Institute of Switching and Data Technics
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PCM - CHARTS

for the Design of Economic PCM Switching Arrays
operating in the Point-to-Point Selection Mode

by
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PREFACE

The 138 PCM CHARTS of this CHART book allow the quick manual design of economic PCM switching arrays with three up to six stages and various numbers of highways.
The application of the PCM CHARTS is outlined in chapter 2.
This CHART book consequently continues the series of dimensioning tables for practical application edited by the Teletraffic Research Team of the University of Stuttgart:

- Table of the Modified Palm-Jacobaeus Loss Formula (MPJ)
  1963, Lotze, A., Wagner, W., ISBN 3-922403-00-X
- Tables for Variance Coefficient D and Overflow Traffic R of One Stage Gradings with Limited Access. Calculation of Secondary Routes in Case of Offered Overflow Traffic
  1965, Lotze, A., Schehrer, R., ISBN 3-922403-01-8
- Tables for Overflow Variance Coefficient and Loss of Gradings and Full Available Groups
  1966,(second edition), Botsch, D., Lotze, A., Schehrer, R., ISBN 3-922403-02-6
- Delay Tables for Limited and Full Availability According to the Interconnection Delay Formula (IDF)
  1968, Thierer, M., ISBN 3-922403-03-4
- Alternate Routing Tables for the Economic Dimensioning of Telephone Networks
  1973, Herzog, U., Lörcher, W., Lotze, A., Schehrer, R., ISBN 3-922403-04-2
- Tables on Delay Systems
  1976, Kühn, P., ISBN 3-922403-05-0
- NIK CHARTS for the Design of Link Systems Operating in the Point-to-Point Selection Mode or Point-to-Group Selection Mode
  1976, Lotze, A., Röder, A., Thierer, G., ISBN 3-922403-06-9

The authors hope that also the present volume of the PCM CHARTS will be a useful tool to many telephone engineers.

All Tables and CHARTS may be ordered from

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1. INTRODUCTION

These PCM CHARTS allow the quick manual design of economic PCM switching arrays with three up to six stages and various numbers of highways. The following symmetrical array types consisting of time-stages (T) and space-stages (S) and leading to economic solutions are considered:

TST, STS, TSST, TSSST, SSTSS, TSSSST.

Two different numbers of time-slots (TS) per multiplex-line (ML) are regarded.

CHARTS 1 - 71 hold for M = 30 TS/ML, chamois pages
CHARTS 72 - 138 hold for M =120 TS/ML, green pages.

The second chapter outlines the application of the PCM CHARTS. For those being interested in more details the chapters 3 to 8 explain the background of the PCM CHARTS, i.e. the array structures, the path allocation principles, the loss calculation and the derivation of the design formulae for minimum cost arrays; see also /17,19/.

When the size of a PCM switching array, the carried traffic per time-slot and the desired probability of loss are prescribed, suitable PCM arrays of different types can be designed by means of the diagrams. Their resulting costs per time-slot for different cost ratios between gates and memory bits can also be found in the CHARTS.

2. APPLICATION OF THE PCM CHARTS

2.1. General Remarks

The six array types mentioned in chapter 1 are described in detail in chapter 4. They are symmetrically structured and have as many incoming as outgoing multiplex-lines. According to the optimization algorithm dealt with in chapter 8 all space switches (SS) have a certain constant size in all intermediate stages and switch 1:1. In order to achieve a desired probability of the Point-to-Point loss B_{pp} for a prescribed carried traffic per time-slot Y/TS the switching arrays may be expanded in stage 1 and correspondingly concentrated in the last stage.

Depending on the type of the first and last stage, S or T, the realization of this expansion differs:

- if it is a T stage, expansion is performed by increasing the number M* of internal time-slots compared to the number M of incoming time-slots per multiplex-line (internal clock frequency increased).
  Therefrom an expansion factor is defined:

$$\beta = M^*/M$$

- if it is a S stage, expansion is performed by increasing the number of internal multiplex-lines, i.e. the number j_1 of multiplex-lines leaving a space switch of the first stage is greater than the number h_1 of incoming multiplex-lines per space switch, therefrom it holds

$$\beta = j_1/h_1$$

PCM switching is always four-wire equivalent, i.e. each PCM highway consists of two multiplex-lines, one for each speech direction. Therefore two different switching modes can be distinguished namely

Separated Switching and Combined Switching (c.f. 2.1.1 and 2.1.2).

Each PCM CHART consists of two diagrams. The diagram on the left hand side holds for the design with regard to the prescribed carried traffic per TS and the desired probability of loss. The parameter H_i yields the size of the space switches. The relative costs per TS can be found in the diagram on the right hand side.

These relative costs per TS of all arrays have been calculated for various cost ratios CR. CR represents the relation between the costs of a logical gate and a memory bit. Additional hardware elements for the control of the arrays can be taken into account by choosing an appropriate value for CR.

All PCM CHARTS are valid for serial transmission of the 8 bit voice samples and furthermore for quasisymmetrical path allocation in case of Combined Switching (see chapter 6.).

2.1.1. Separated Switching

Separated Switching (SSw) means that only connections from incoming highways to outgoing highways ("from left to right") can be established.
This leads to an array structure, where two identical, but separated arrays for the two speech directions have to be provided, see Fig.1.

On the left hand side of the two identical arrays all incoming highways, carrying only one-way traffic, terminate, each speech direction on an array of its own. The same holds for the outgoing highways connected to the right hand side.

If the two paths (one per speech direction) in each array are chosen identically, it is sufficient to provide control memories only for one array; the other one can be controlled by these memories, too.

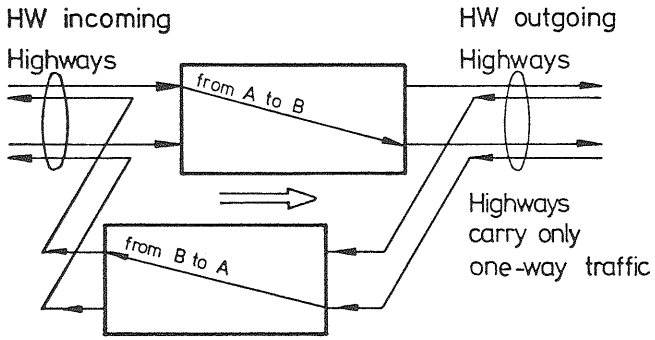


Fig. 1: The Separated Switching Mode

2.1.2. Combined Switching

Combined Switching (CSw) means that connections between all highways, connected to one array can be established. The highways may carry two-way traffic as well as one-way traffic.
The incoming speech directions of all highways terminate on the left hand side of the array; the outgoing speech directions on the right hand side, see Fig.2. For each speech connection one has therefore to establish two paths through the same "Combined" switching array.

The manner how these two paths are allocated within the array has a remarkable influence on the costs as the number of necessary control memory bits is influenced by it. Suitable path allocation principles will be presented in chapter 6.
Combined Switching and Separated Switching are treated within the CHARTS together on one sheet.

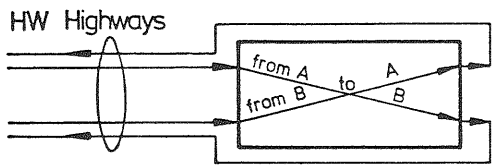


Fig. 2: The Combined Switching Mode

It is important to point out that the two arrays cooperating in case of the Separated Switching mode serve twice as many highways than one array of the same size operating in the Combined Switching mode. Consequently, the maximum number of simultaneous speech connections for SSw is twice as much as for CSw. Furthermore, the probability of the Point-to-Point loss for a fixed carried traffic per TS is the same for one array operating in the Combined Switching mode having HW highways as for the two arrays operating together in the Separated Switching mode with 2·HW highways.

2.2. On the Choice of the Highway Numbers

The highway numbers for the different array types being presented have been chosen such that comparisons between the various array types are easily possible. Therefore the arrays TST, STS, TSST, TSSST and SSTSS are calculated for highway numbers according to a quadratic progression, However, arrays having space matrices with more than 64 incoming MLs are not regarded.
The six stage arrays are designed according to a cubic progression of the highway numbers.
The size of all presented arrays yields minimum costs per TS and is regarded as a final size. Smaller intermediate sizes or extensions beyond the final size result in an increase of the relative costs per TS see chapter 4.

2.3. Examples for the Use of the PCM CHARTS

Five typical examples are given for the use of the PCM CHARTS.

2.3.1. Design of a TSST Switching Array

Be prescribed:

- 196 highways with M = 30/32 TS each
- Combined Switching
- carried traffic per TS Y/TS = 0.8 Erlang
- probability of the Point-to-Point loss B_{pp} = 0.1% (Definition of B_{pp} see chapter 5).

The diagram on the left hand side of CHART 20 shows the expansion factor β of the array versus the carried traffic per TS; the probability of loss B_{pp} is the curve parameter. For the above prescribed parameters one obtains β = 1.6. This value β, together with the matrix size h_2 = 14 defines the array structure, see Fig.3.

The additional "horizontal" MLs are necessary as Combined Switching is prescribed (c.f. chapter 4.3.).

The expansion is performed by increasing the number of internal time-slots from 30 to 48 (increase of clock frequency).

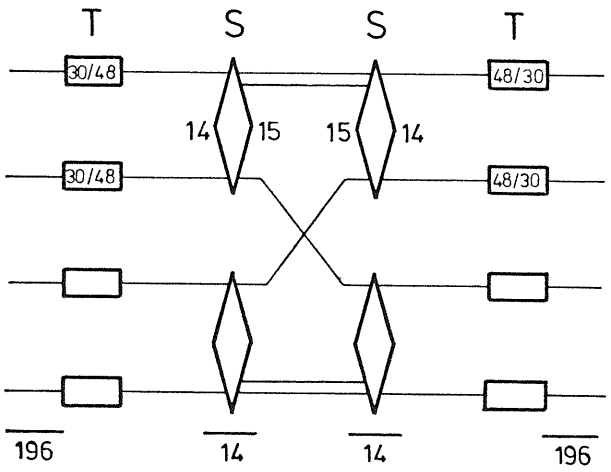


Fig. 3: Design Example of a TSST Array
HW = 196 ML, M = 30 TS, Y/TS = 0.8 Erl, B_{pp} = 0.1%

The right diagram in CHART 20 shows the resulting relative costs/TS for a given expansion β. Parameter for the curves is the cost ratio. The bold lines hold for Combined Switching and the dashed lines for Separated Switching.

The resulting relative costs/TS for e.g. CR = 5 and CSw are about 35 bits/TS.

The same CHART 20 allows the design of a TSST array operating in the Separated Switching mode and having 2·196 highways. For the same values of Y/TS and B_{pp} one obtains the same design parameters. For the same CR one gets (dashed line) slightly smaller costs, 34.5 bits/TS, as the above mentioned additional "horizontal" MLs are no longer required.

2.3.2. Comparison of the Costs Between Different Array Types

Be calculated the costs of the different array types for a prescribed constant grade of service, B_{pp} = 0.1% for Y/TS = 0.8 Erl, and for various highway numbers, each highway having M = 30 TS. Combined Switching is assumed as well as a cost ratio of CR = 5.

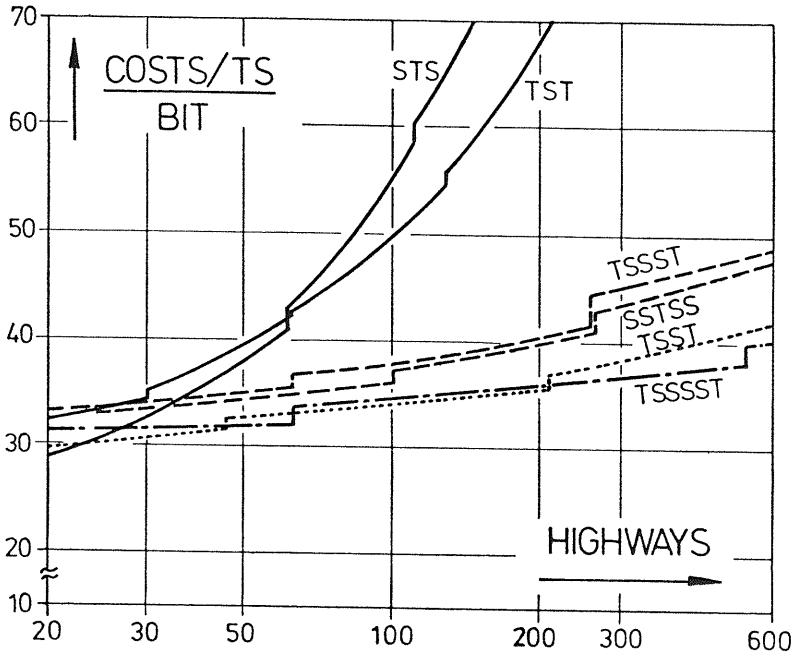


Fig. 4: Comparison of the Costs
M = 30 TS, Y/TS = 0.8 Erl, B_{pp} = 0.1%,
Combined Switching, CR = 5,

The resulting relative costs are drawn in Fig.4; the different costs for the different highway numbers and the desired grade of service have been looked up in the PCM CHARTS.
The curves show that the three-stage arrays become rather expensive for greater highway numbers whereas the four- and six-stage arrays are the cheapest over the whole range (TST and STS arrays with more than 64 highways are not included in the CHARTS).

2.3.3. Comparison Between Combined Switching and Separated Switching

Be designed a switching array for about 70 highways with M = 30 TS each, a grade of service B_{pp} = 0.1% for Y/TS = 0.8 Erl and a cost ratio CR = 5.
The type of the array and the switching mode are to be chosen such that the cheapest realization is possible.
Regarding the highway numbers being presented within the CHARTS, it is possible to design an array for Combined Switching with 64 highways and for Separated Switching with 2·36 highways.

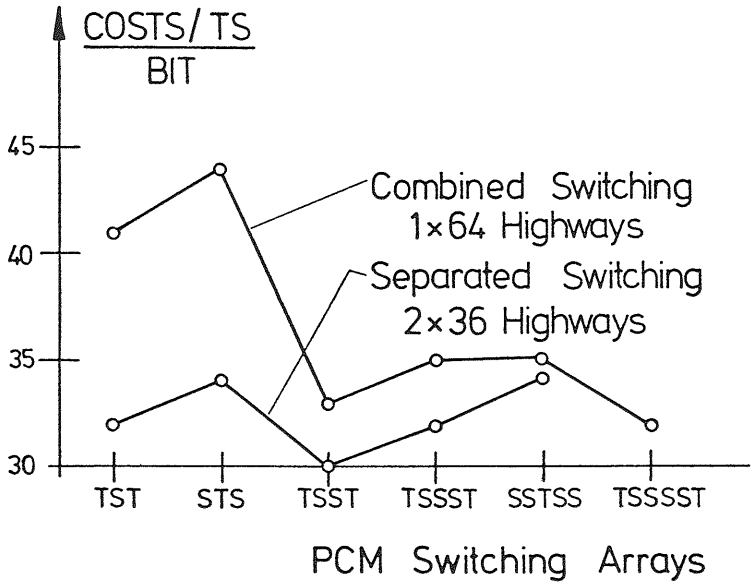


Fig. 5: Comparison Between Combined and Separated Switching
M = 30 TS, Y/TS = 0.8 Erl, B_{pp} = 0.1% CR = 5

The costs for the different array types have been looked up in the CHARTS, the result is shown in Fig. 5.
As one can see Separated Switching is in any case cheaper than Combined Switching. The example shows that for the given parameters the TSST array, operating in the Separated Switching mode, is the cheapest in this case.

2.3.4. The Influence of the Number of Time-Slots per Multiplex-Line on the Costs

Be designed a PCM switching array for n = 1920 trunks with B_{pp} = 0.1% for Y/TS = 0.8 Erl and Combined Switching.
The number of time-slots per highway (30 or 120 TS,resp.) is to be chosen such that minimum costs are achieved.

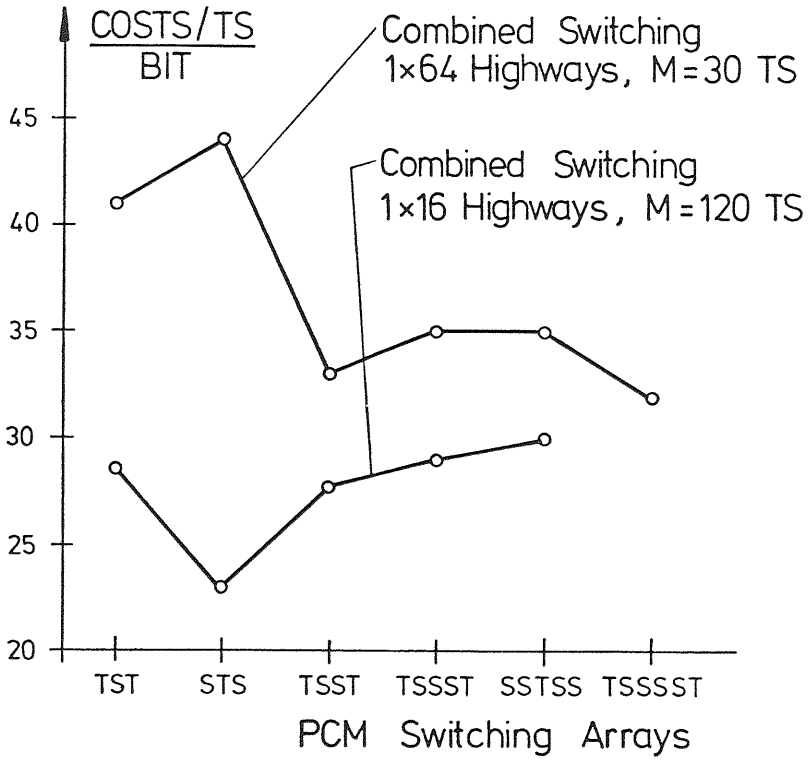


Fig. 6: Influence of the Number of Time-Slots on the Costs
n = 1920, Y/TS = 0.8 Erl, B_{pp} = 0.1%,
Combined Switching, CR = 5

The relative costs per TS for M = 30 and M = 120 can be looked up in the CHARTS. Switching with M = 120 TS/ML is in all cases cheaper as the number of gates is reduced if the number of TS/ML is increased. In this case the STS array (M = 120) has the least costs (see Fig.6).

2.3.5. The Influence of the Cost Ratio CR

Fig. 7 demonstrates the increase of the relative costs per TS for an increasing cost ratio CR. The regarded arrays have 144 highways with M = 30 TS/ML each, a grade of service with B_{pp} = 0.1% for Y/TS = 0.8 Erl and operate in the Combined Switching mode.
The strongest increase suffer the three-stage arrays, the smallest increase holds for the T..T arrays.

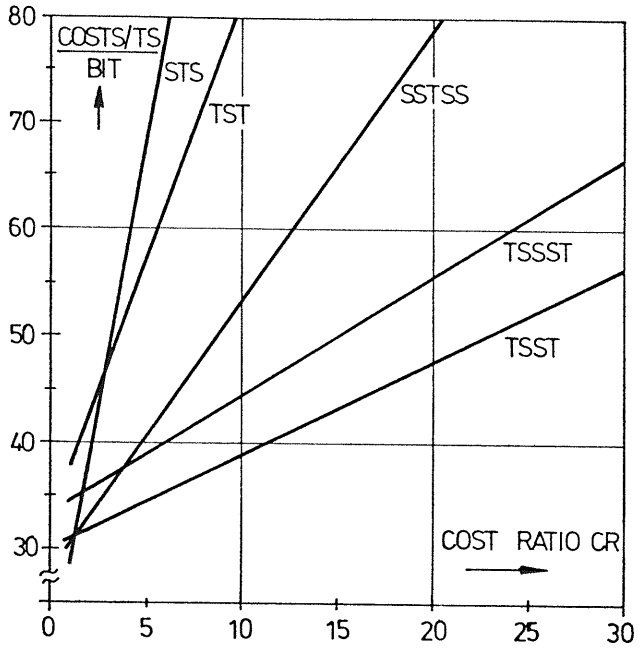


Fig. 7: Influence of the Cost Ratio CR on the Costs
HW = 144 ML, M = 30 TS, Y/TS = 0.8 Erl, B_{pp} = 0.1%
Combined Switching

Up to now the use of the CHARTS has been explained in order to enable their application. The following chapters outline in more detail the investigations leading to these PCM CHARTS.

3. ELEMENTS OF A PCM SWITCHING ARRAY

3.1. The Space Stage

PCM switching arrays are composed of two different types of stages, namely the space stage and the time stage.
The space stage consists of space switches (SS) as shown in Fig. 8, which form switching matrices for time- multiplex-lines.
Each switching matrix has h incoming and j outgoing MLs, having M time-slots each. The number of outgoing MLs may be equal, greater or less than the number of incoming ones.
A space switch only allows the coincident switching of time-slots from each incoming ML to each outgoing ML. Switching is performed by logical gates, forming the crosspoints of the matrices. They are controlled by control memories. The cheapest realization is achieved if a control memory controls the gates of an incoming ML, if h < j .

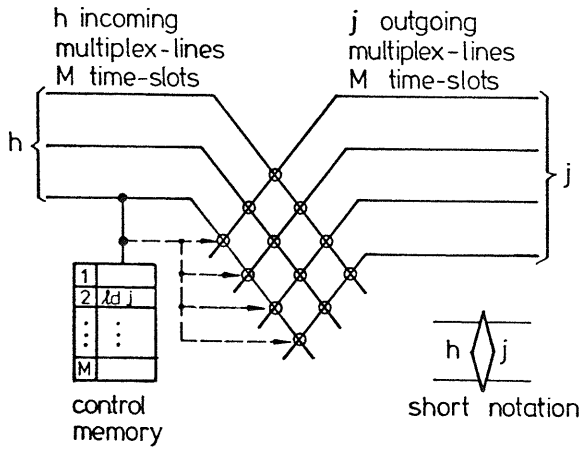


Fig. 8: The Space Switch

A control memory has as many storage places as there are time-slots on the multiplex-line; each storage place needs ld j bits, eventually to be rounded up to the next greater integer value.
To simplify the figures, a short notation for the space switch is introduced as shown in Fig. 8 below.

3.2. The Time Stage

The time stage is composed of a number of time-slot interchanges (TSI) as shown in Fig. 9, consisting of a speech memory and a control memory. A time-slot interchange allows the switching of each of the M time-slots of the incoming ML to each of the M* time-slots of the outgoing ML.
M* may be equal or greater than M.
Time-slot interchanging is performed by the aid of the speech memory and the respective control memory. The control memory controls either writing into the speech memory or reading out from it.
This function of random addressing is depicted in Fig. 9 by a double arrow.
Reading or writing on the opposite side of the speech memory is done cyclically according to a time-slot counter.
The cheaper realization is achieved if the control memory controls that side of the speech memory where the number of time-slots is greater. To simplify the figures a short notation for the TSI is introduced as shown in Fig. 9 below.

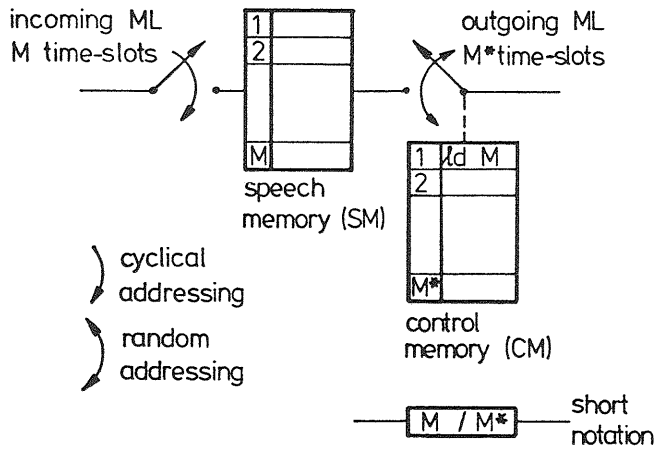


Fig. 9: The Time-Slot Interchange

4. THE PRESENTED PCM SWITCHING ARRAYS

4.1. General Remarks

With the space switch and the time-slot interchange a great variety of PCM switching arrays, consisting of T-stages and S-stages can be designed.
The presented PCM CHARTS deal with six types of symmetrical arrays, having as many incoming MLs as outgoing ones. Only such symmetrically structured arrays allow savings in control memories, provided that a suitable path allocation principle is implemented in case of CSw.
An expansion, if necessary, is always performed in the first stage and the corresponding concentration in the last stage. All intermediate stages switch 1:1. All space switches of these stages have the same size.
Arrays consisting only of space stages are not regarded, as they have a very poor grade of service.
The presented six array types in the PCM CHARTS fulfill the prerequisites which lead to economic solutions depending on the size, CR and the desired traffic parameters.

4.2. Three Stage PCM Arrays and Mapping Rules

4.2.1. The TST Array

Fig. 10a shows the TST array. It has h_2 incoming and $j_2 = h_2$ outgoing MLs with M time-slots each. Fig. 10b shows the mapped equivalent SDM array.
In order to calculate the probability of loss of a PCM switching array it is advantageous to map this array into an equivalent SDM array and to calculate the probability of loss of this SDM array. There are certain mapping rules which will be discussed in the following.

The mapping rules are as follows:

One time-slot interchange with M time-slots on the incoming ML and M* time-slots on the outgoing ML becomes one multiple of the size M|M*.

The space switch with h_2 incoming MLs and j_2 outgoing MLs, each having M* time-slots, becomes a column of M* multiples with h_2 inlets and j_2 outlets, each.

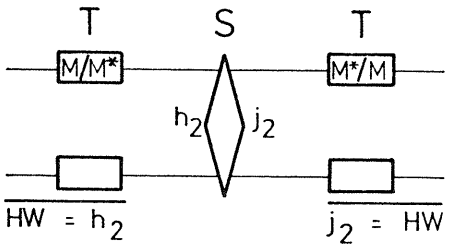


Fig. 10a: The TST Array

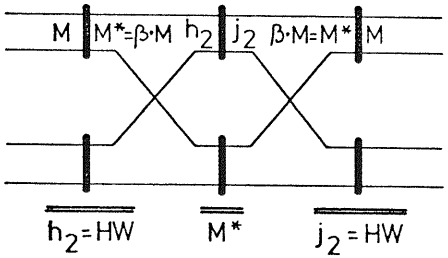


Fig. 10b: The Mapped TST Array

The value $\beta = M^*/M$ depends on the carried traffic per TS and the prescribed probability of loss, see chapter 5.
As the MLs terminate on a time-slot interchange each,the mapped M time-slots per ML terminate all in the same multiple. It is obvious that only Point-to-Point selection with one marking attempt is possible, provided that the considered outgoing trunk group consists of one highway, only.
It is possible to make this array type strictly nonblocking if M^* is chosen to

$$M^* = 2 \cdot M - 1 \qquad /6/.$$

4.2.2 The STS Array

Fig. 11a shows the STS array and Fig. 11b its mapped equivalent SDM array.
The mapping rules are the same as above. Different is the mapping of the incoming and outgoing MLs terminating now on space switches.
The mapped M TS of these MLs lead now to M different multiples of the first and the last stage, resp.

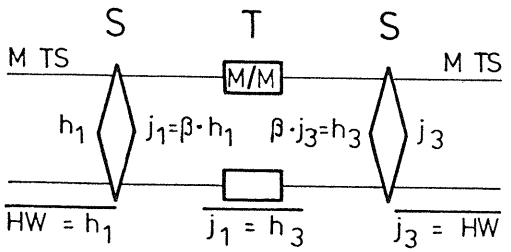


Fig. 11a: The STS Array

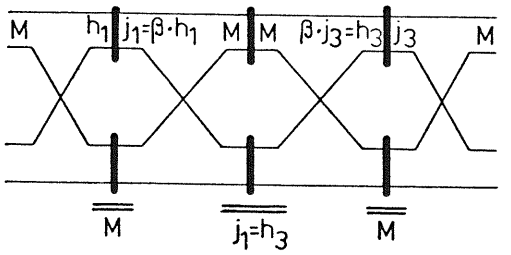


Fig. 11b: The Mapped STS Array

From this it follows that different selection modes can be applied.
- Point-to-Point selection (PPL calculation /11/)
- Point-to-Point selection with multiple marking attempts (PPLM calculation /15/)
- Point-to-Group selection (CLIGS calculation /1/)

It is well known that Point-to-Group selection leads to the lowest probability of loss, but requires the maximum amount for path searching.

Mapping of the PCM arrays does not depend on the switching mode.
For Combined Switching the one and only array has to be mapped; if Separated Switching is applied, only one array of the two identical arrays has to be regarded.
From this it follows that the loss calculation can be performed, considering only one equivalent SDM array.
It is possible to make also this array type strictly nonblocking, if j_1 is chosen to

$$j_1 = 2 \cdot h_1 - 1 \qquad /6/.$$

4.3. The Four Stage Switching Array TSST

The four stage TSST array, see Fig. 12a,is the first to allow forming of blocks; Fig. 12b shows the mapped SDM array. The same mapping rules hold as above.
The blocks which are formed between stages 1 and 2 as well as 3 and 4 of the PCM array appear also as blocks within the mapped array. The incoming and outgoing multiplex-lines, having M TS, terminate at one TSI each. From this it follows that the equivalent M trunks terminate in the mapped array also at one SDM multiple only. Therefore, only Point-to-Point selection with one marking attempt is possible as one outgoing ML can only be reached via one multiple of the last stage.

Additional multiplex-lines (i.e. the dashed lines between stages 2 and 3) have to be provided if Combined Switching is applied. This is necessary for this switching mode only, as thus the maximum number of possible connections remains constant between all blocks on the left and right hand side, including likewise numbered blocks.(for CSw one connection requires two paths).

The design formula follows from the prerequisite that all intermediate stages switch 1:1 and the number of incoming and outgoing MLs is the same, namely HW.

This four stage array can easily be extended from a smaller initial size to the planned final size, if the principle of constant block size is applied / 11/. In this case the space switches have a priori the final size. For intermediate sizes of the four stage array with less blocks, more than one ML leads from a block on the left hand side to a block on the right hand side.

4.4. Five Stage Switching Arrays

4.4.1. The TSSST Array

Fig. 13a shows the PCM array and Fig. 13b the mapped equivalent SDM array. Blocks are formed between stages 1 and 2 as well as between stages 4 and 5. These blocks also appear in the mapped array. The presentation of the middle stage in the SDM array is such that multiples, representing the same time-slot number, are adjacent.

Design Formula:

$h_2 = (j_2 = h_3) = j_3 = \sqrt{HW}$

$M^* = \beta \cdot M$

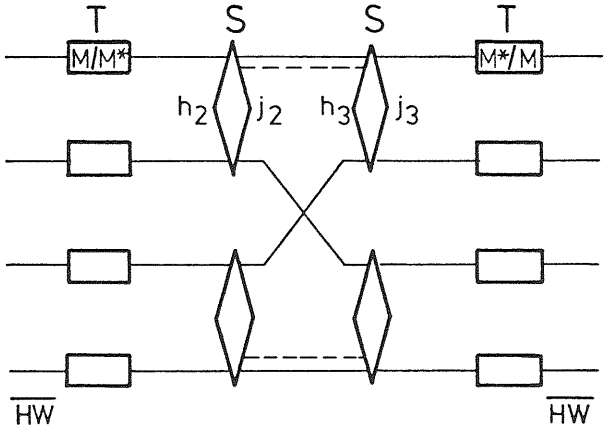


Fig. 12a: The TSST Array

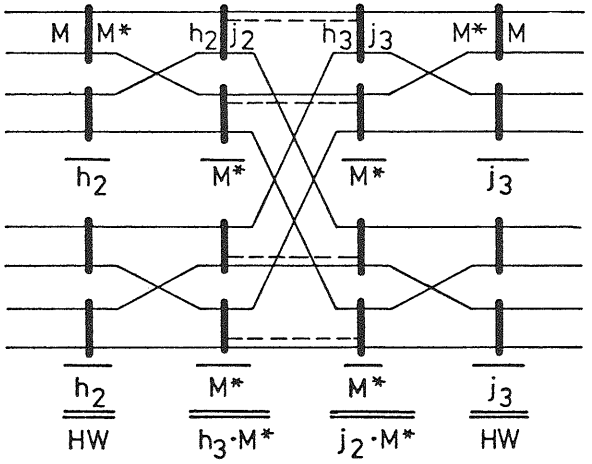


Fig. 12b: The Mapped TSST Array

The TSSST array can be extended blockwise like the four stage array if the space switches are designed a priori for the final size.

Design Formula:

$$h_2 = j_2 = h_3 = j_3 = h_4 = j_4 = \sqrt{HW}$$

$$M^* = \beta \cdot M$$

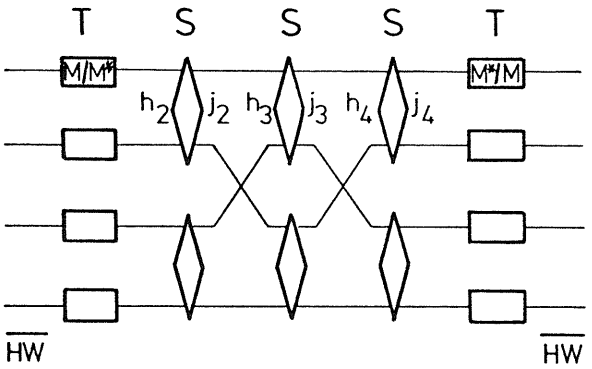


Fig. 13a:

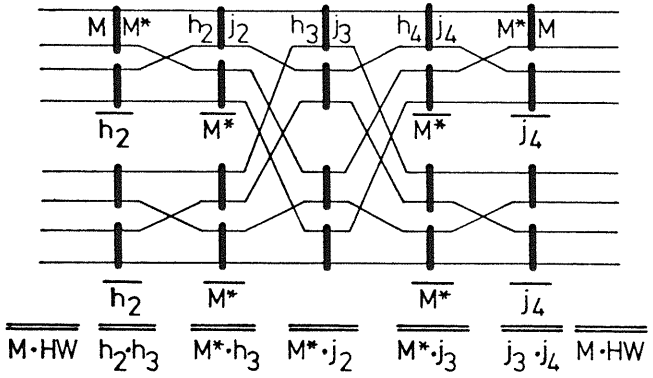


Fig. 13b: The Mapped TSSST Array

4.4.2. The SSTSS Array

This PCM array allows forming of blocks between stage 2,3 and 4, see Fig. 14a. Expansion in the first stage is done by increasing the number of multiplex-lines $j_1 = \beta \cdot h_1$

Design Formula:

$$h_1 = j_2 = h_2 = j_4 = h_4 = j_5 = \sqrt{HW}$$

$$j_1 = h_5 = \beta \cdot h_1$$

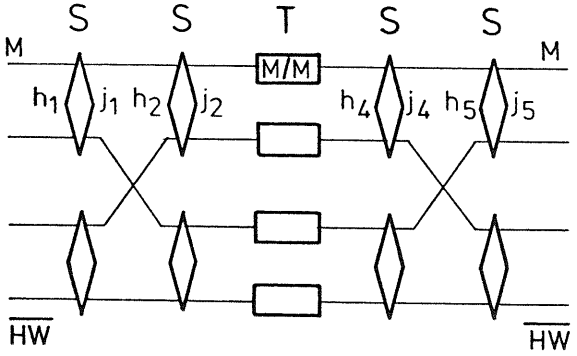


Fig. 14a: The SSTSS Array

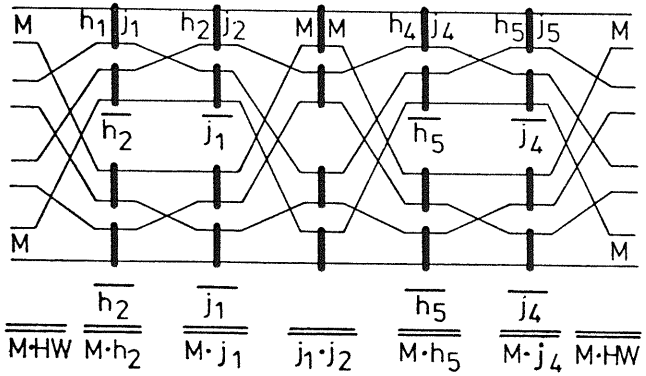


Fig. 14b: The Mapped SSTSS Array

The array allows very good extension strategies if the blocks in the middle stages and the space switches are designed for the final size.
Fig. 14a shows the PCM array and Fig. 14b the mapped equivalent SDM array.
If in contradiction to the prerequisites also the second stage is expanded, the array can become strictly nonblocking (the values are $j_1 = 2h_1-1$, $j_2 = 2h_2-1$, /6/).

4.5. The Six Stage Switching Array TSSSST

There are different possibilities for the structure of this array type. The presented array has the minimum amount of costs and can easily be extended if the blocks and space switches are designed for the final size.
Similar to the TSST array additional "horizontal" MLs between stages 3 and 4 in case of Combined Switching could be provided; the influence on the probability of loss as well as on the costs is not remarkable.
Fig. 15 shows the design formula, the PCM array and the mapped SDM array.

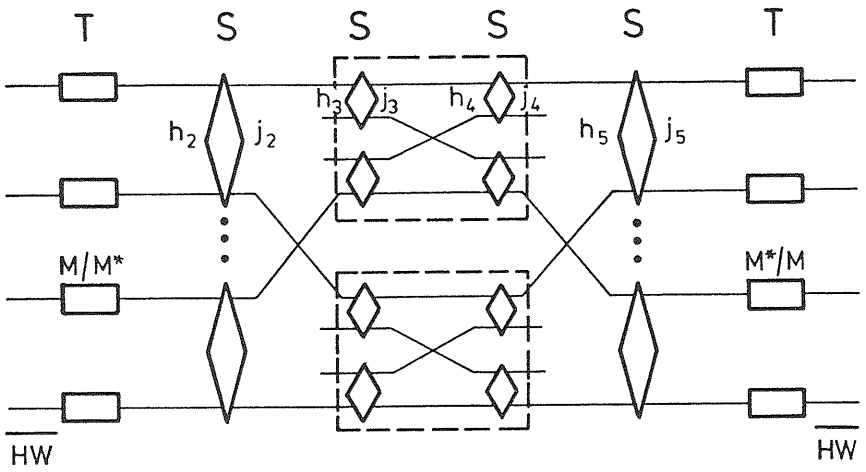


Fig. 15a: The TSSSST Array

Design Formula:

$$h_2 = j_2 = h_3 = j_3 = h_4 = j_4 = h_5 = j_5 = \sqrt[3]{HW}$$

$$M^* = \beta \cdot M$$

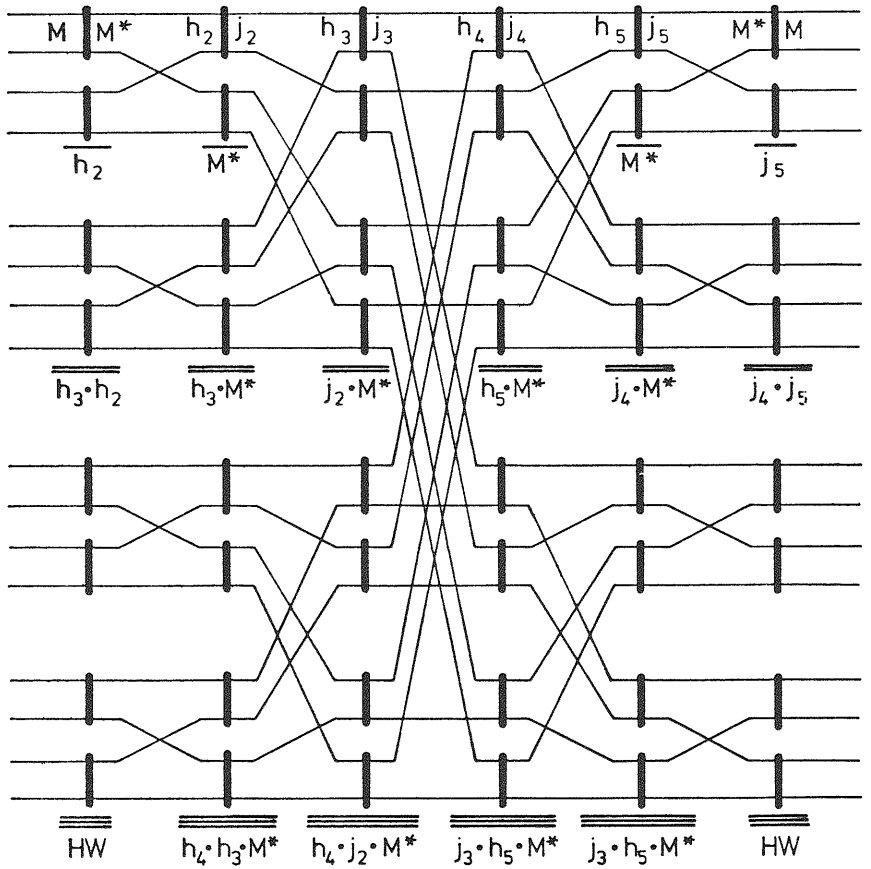


Fig. 15b: The Mapped TSSSST Array

5. CALCULATION OF THE PROBABILITY OF LOSS

5.1. Calculation Methods

Within the presented PCM CHARTS all curves for the probability of loss are calculated for the Point-to-Point loss in case of one marking attempt, as this represents the worst case. Many simulations show the good accordance between calculation and simulation for Combined Switching as well as for Separated Switching /11/.
The Point-to-Point loss is defined as follows:

Upon arrival at an idle inlet, a call suffers a Point-to-Point loss, if no chain of idle links through the link system can be found to the a priori determined idle outlet of the desired trunk group. Only those calls contribute to the arrival rate that find one inlet as well as at least one outlet of the desired outgoing trunk group idle. According to this definition the Point-to-Point loss is defined as

$$B_{pp} = \text{lost calls/ offered calls.}$$

The Point-to-Point loss has been calculated under the assumption of PCT 1 traffic (Pure Chance Traffic of Type 1).
PCT 1 is defined as an offered Poisson traffic having a constant call rate λ, negative exponentially distributed interarrival times and negative ex - ponentially distributed holding times with mean value h_m; thus the offered traffic is $A = \lambda \cdot h_m$

For T..T arrays a Point-to-Point selection with more than one marking attempt is only then possible if the considered outgoing trunk group consists of more than one highway.

For S..S arrays Point-to-Point selection with one or multiple marking attempts as well as Point-to-Group selection can be performed.

The probability of loss for
- Point-to-Point selection with one marking attempt is calculated with the PPL method /11/.
- Point-to-Point selection with multiple marking attempts is calculated with the PPLM method /15/
- Point-to-Group selection is calculated according to the CLIGS method /1/.

The mapped SDM structures of 5- and 6-stage PCM arrays do not have the usual interleaved wiring. Therefore the PPL method was suitably adapted /16/.

5.2. Expansion in Stage One

It is known from SDM arrays that the probability of loss is reduced by an expansion in the first stage and a corresponding concentration in the last stage; all multiples in the intermediate stages switch 1:1. This expansion leads to different realizations of PCM switching arrays depending on the type of the first and the last stage (T or S).
If both are T stages, expansion can be done by increasing the number of time-slots within the PCM switching array, i.e. $M^* > M$. This is, however, only possible up to a maximum clock frequency, depending on the technological standard at the time being. If a further increase is not possible, the change from serial to parallel switching reduces the clock frequency by the factor 8. As this expansion mode, namely the increase of the number of internal TS is the cheapest, it is applied within the PCM CHARTS.

If the first and the last stage is a S-stage, the expansion is performed by increasing the number of MLs leaving the first stage compared with the number of incoming MLs.
For the expansion factor β it holds:

$$M^* = \beta \cdot M \qquad \text{or} \qquad j_1 = \beta \cdot h_1$$

It should be noted that not all values of β can be realized, as the number of TS or the number of MLs leaving stage 1,resp., has to be an integer value.

Fig. 16 shows a typical example for the calculated loss curves. Here the necessary expansion factor β in stage No.1 is drawn versus Y/TS in Erlangs for a given Point-to-Point loss as parameter.
This example of an 5-stage array with n = 3000 terminations for CSw or n = 2·3000 terminations for SSw, needs for a carried traffic of 0.8 Erl/TS and a prescribed probability of loss of 0.1% an expansion factor β of 1.75.

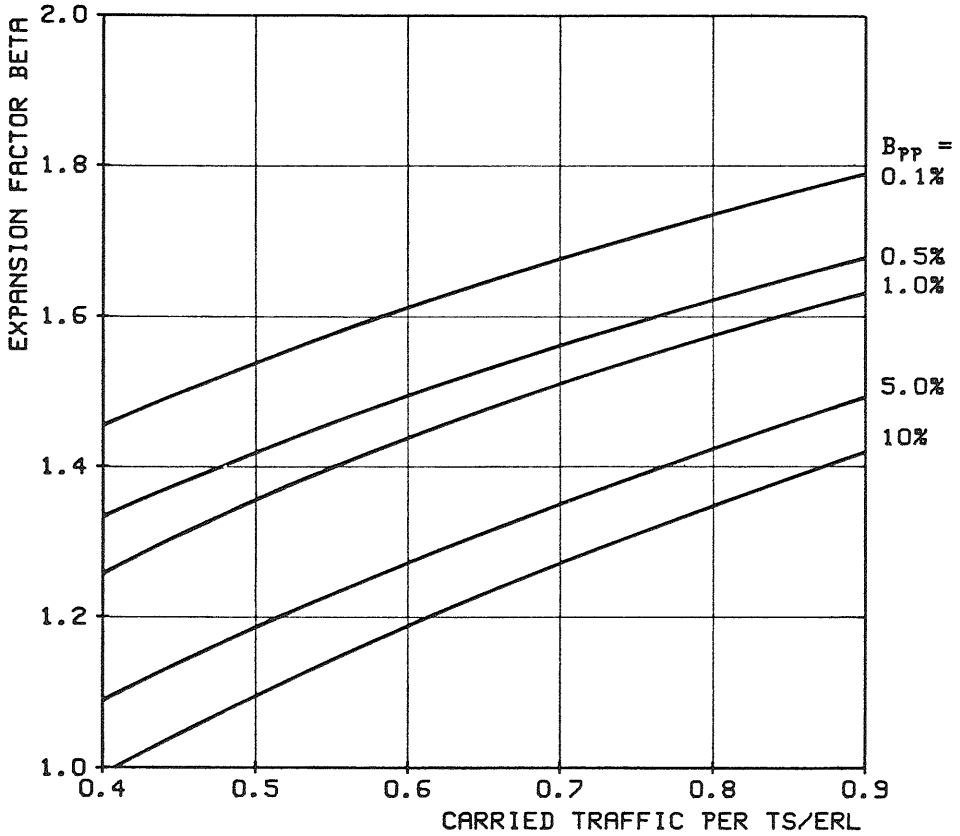


Fig. 16: Probability of Loss for a SSTSS Array
HW = 25 MLs, M = 120 TS

6. PATH ALLOCATION FOR COMBINED SWITCHING

The recommended path allocation principles require symmetrically structured PCM switching arrays, i.e. the types and number of stages have to be identical on both sides of the median vertical line. This prerequisite holds for all investigations and switching arrays discussed in the following.
Path allocation between both speech directions of one connection is applied in order to save control memories for the gates and the speech memories.

An appropriate path allocation allows the elements on the right hand side of the median vertical line to be controlled by the control memories on the left hand side. Two different path allocation principles will be considered:

- the symmetrical path allocation
- the quasisymmetrical path allocation

6.1. Path Allocation Within T..T Arrays

6.1.1. The Symmetrical Path Allocation

Symmetrical path allocation means that the two speech directions of one connection lead through the Combined Switching array on paths which are symmetrical to the median vertical line. Furthermore, these two paths use likewise numbered time-slots between the first and the last stage.
This allows the TSIs of the last stage to be controlled by the control memories for the TSIs of the first stage. The same holds for the space switches for the intermediate stages, supposed there is more than one S-stage.
It is important to notice that path searching is simplified by this allocation principle , as it is sufficient to search only for one idle path, e.g. the speech direction from A to B, the corresponding path from B to A, i.e. the other speech direction,is its symmetrical counterpart and a priori idle, too.
The principle of symmetrical path allocation is shown in Fig.17.

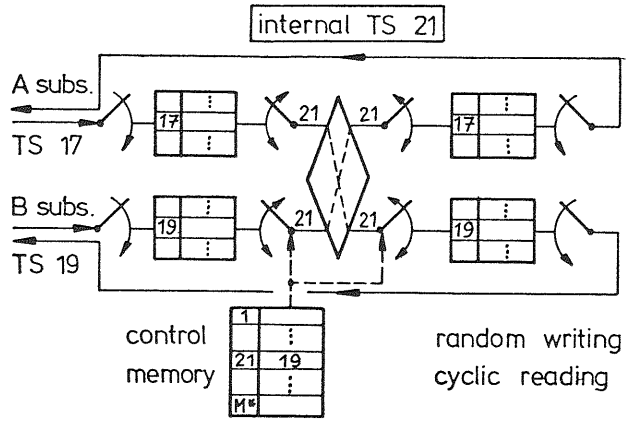


Fig. 17: Symmetrical Path Allocation Within T..T Arrays

A connection has to be established from the incoming ML of the A subscriber to the outgoing ML of the B subscriber and vice versa. The A subscriber uses TS No.17 on both MLs of its highway, the B subscriber TS No.19.
Be chosen by the path search algorithm TS No.21 for both speech directions as internal time-slot.
The depicted control memory on the lower left hand side controls time slot interchanging from external time-slot No.19 to internal TS No.21, and at the right hand side interchanging from internal TS No.21 to external TS No.19.

An important restriction of symmetrical path allocation is the fact that it is impossible to switch a call which originates in a certain highway back to a destination via the same highway; the internal TS No.21 would be necessary twice on the one intermediate multiplex-line.

For T..T arrays with 4 and more stages a further restriction arises:
It is not possible to switch an arriving call on the left hand side to a destination via the likewise numbered block on the right hand side.

This restriction can be overcome by doubling the "horizontal" MLs between likewise numbered blocks (c.f. TSST array).

6.1.2. The Quasisymmetrical Path Allocation

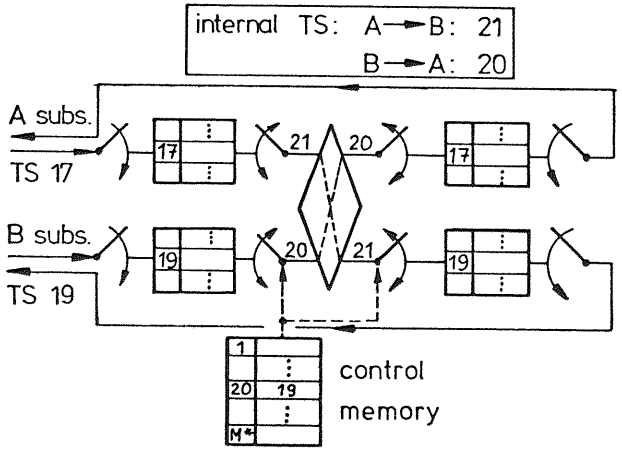


Fig. 18: Quasisymmetrical Path Allocation Within T..T Arrays

The two paths for the two speech directions now use an even/odd time-slot relation as shown in Fig. 18.
Even /odd relation means:
If the speech direction from A to B uses an even time slot number, the speech direction from B to A uses the time-slot even + 1.
If the speech direction from A to B uses an odd time-slot number, the speech direction from B to A uses the time-slot odd-1.

It is obvious that both paths again have to lead via MLs being symmetrical to the median vertical line.
The quasisymmetrical path allocation overcomes the restriction of not being able to switch into the same highway or block, resp.
The example as shown in Fig.18 uses for the speech direction A to B the internal TS No.21 and for speech direction B to A the internal TS No.20.
The logical function is such that during internal time-slot No.20 the storage place 19 of the lower left speech memory has to be read. During internal TS No.21 the storage place 19 of the lower right speech memory has to be written.
From this it follows that it is sufficient to store control information "19" only once; it can control the left and right TSI during the corresponding time-slots.
For path searching holds that only one path has to be searched for, the corresponding path for the other speech direction is its quasisymmetrical counterpart.

The only condition for quasisymmetrical path allocation is that the number of time-slots within one frame has to be even.

6.2. Path Allocation Within S..S Arrays

6.2.1. The Symmetrical Path Allocation

Here symmetrical path allocation means that both speech directions of one connection lead via symmetrical paths through the array; in the middle T-stage the same TSI has to be used.
This again allows the space switches right of the median vertical line to be controlled by the control memories of the left hand side.
It should be noted that no connections can be established using likewise TS numbers on the highways from A and to B. The influence of this restriction can be neglected if path searching is intelligent enough to avoid this time-slot combination.

6.2.2. The Quasisymmetrical Path Allocation

The difference to the symmetrical path allocation appears in the middle T-stage. Both speech directions now lead via two related TSIs, instead of via the same one. However, these two related TSIs can be controlled by the same control memory. This also cuts down the number of the control memories of the middle stage to one half.
The control memory as shown in Fig.19 controls reading from the upper TSI and writing into the lower TSI; the stored control information is used twice. It is necessary for this allocation principle that the number of TSIs in the middle stage be even.
In case of five stage SSTSS arrays the number of TSIs has to be even within each block formed by stages 2,3 and 4 (see also example in 7.2.5).

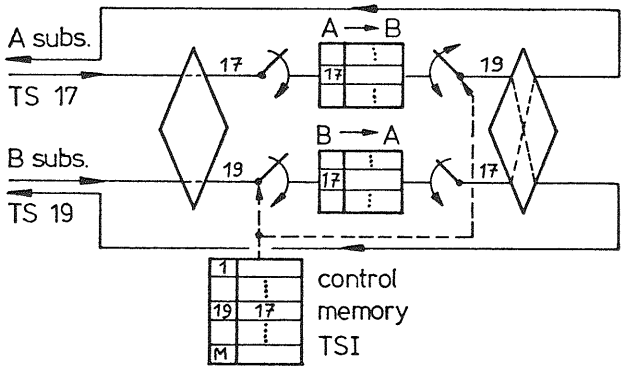


Fig. 19: Quasisymmetrical Path Allocation Within S..S Arrays

Quasisymmetrical path allocation is provided for all T..T and S..S arrays being presented in the PCM CHARTS.

7. CALCULATION OF THE COSTS OF A PCM SWITCHING ARRAY

7.1. Cost Formulae

The costs for a PCM array are the sum of the costs for all logical gates in the crosspoints of the space switches, the costs for the control memories of the SS, the costs for the TSIs, i.e. costs for the speech memories and the respective control memories. The costs for the control memories depend on whether a path allocation principle is applied or not. The formulae for the calculation are given in Table 1. The equations have a general form in order to allow their application also if e.g. additional multiplex-lines have to be provided.
The prerequisite of symmetrically structured arrays is already implemented. For all formulae it is assumed that quasisymmetrical path allocation for Combined Switching is applied.

Abbreviations and prerequisites:

G	: number of gates	
CMG	: number of control memory bits for the gates	
SM	: number of speech memory bits	
CMSM	: number of control memory bits for the SMs	
M	: number of time-slots per ML	
E,Q	: Separated Switching	E = 2, Q = 1,
	Combined Switching	E = 1, Q = 0.5,
P	: switching in serial	P = 1,
	switching in parallel	P = 8,
β	: expansion factor	
ld a	: logarithmus dualis $\log_2 a$	

whenever ld a is used, it has to be checked whether the result is an integer value; if not, the next greater integer value has to be applied for the calculation of the necessary number of memory bits.

- the number of incoming and outgoing MLs is identical
- switching arrays are structured symmetrically
- forming of blocks is as discussed in chapter 4.

Table 1:

TST:

$G = h_2^2 \cdot E \cdot P$

$CMG = h_2 \cdot \beta \cdot M \cdot \mathrm{ld}\, h_2$

$SM = h_2 \cdot M \cdot 2 \cdot 8 \cdot E$

$CMSM = h_2 \cdot \beta \cdot M \cdot E \cdot \mathrm{ld}\, M$

STS:

$G = h_1 \cdot j_1 \cdot 2 \cdot E \cdot P$

$CMG = h_1 \cdot M \cdot E \cdot \mathrm{ld}\, j_1$

$SM = j_1 \cdot M \cdot 8 \cdot E$

$CMSM = j_1 \cdot M \cdot Q \cdot \mathrm{ld}\, M$

TSST:

$G = HW \cdot j_2 \cdot 2 \cdot E \cdot P$

$CMG = HW \cdot \beta \cdot M \cdot E \cdot \mathrm{ld}\, j_2$

$SM = HW \cdot M \cdot 2 \cdot 8 \cdot E$

$CMSM = HW \cdot \beta \cdot M \cdot E \cdot \mathrm{ld}\, M$

TSSST:

$G = (HW \cdot j_2 \cdot 2 + h_3 \cdot j_3 \cdot j_2) \cdot E \cdot P$

$CMG = HW \cdot \beta \cdot M \cdot E \cdot \mathrm{ld}\, j_2 + j_2 \cdot h_3 \cdot \beta \cdot M \cdot \mathrm{ld}\, h_3$

$SM = HW \cdot M \cdot 2 \cdot 8 \cdot E$

$CMSM = HW \cdot \beta \cdot M \cdot E \cdot \mathrm{ld}\, M$

SSTSS:

$G = (HW \cdot j_1 \cdot 2 + h_2 \cdot j_2 \cdot j_1 \cdot 2) \cdot E \cdot P$

$CMG = (\mathrm{ld}\, j_1 + \beta \cdot \mathrm{ld}\, j_2) \cdot HW \cdot M \cdot E$

$SM = j_1 \cdot j_2 \cdot M \cdot 8 \cdot E$

$CMSM = j_1 \cdot j_2 \cdot M \cdot Q \cdot \mathrm{ld}\, M$

TSSSST:

$G = (HW \cdot j_2 \cdot 2 + 2 \cdot h_3^2 \cdot j_3 \cdot j_2) \cdot E \cdot P$

$CMG = (HW \cdot \beta \cdot M \cdot \mathrm{ld}\, j_2 + j_2 \cdot h_3 \cdot \beta \cdot M \cdot \mathrm{ld}\, j_3) \cdot E$

$SM = HW \cdot M \cdot 2 \cdot 8 \cdot E$

$CMSM = HW \cdot \beta \cdot M \cdot E \cdot \mathrm{ld}\, M$

The formulae include a factor E. This factor E holds for a multiplication by two if Separated Switching is applied, due to the necessary second switching array.
As the number of MLs is also multiplied by two for Separated Switching there is generally no influence on the calculated costs per time-slot concerning the gates and the speech memories.
However, the amount for the control memories for SSw is not in any case twice as much as for CSw, it is sometimes smaller. This will be discussed in detail in chapter 7.2.

In order to allow comparisons between the different arrays, a cost ratio CR was defined which is the ratio between the costs for a gate and the costs for a storage bit.

For the total costs it holds:

COSTS = CR· number of gates +
speech memory bits +
control memory bits for gates and speech memories

$$\boxed{COSTS = CR \cdot G + SM + CMG + CMSM}$$

THE UNITY OF THE COSTS BE ONE MEMORY BIT.

Within the CHARTS these costs are standardized with respect to the number of connected highways and the number of time-slots, i.e. the total number of terminations.
Therefrom result the COSTS/TS/BIT.

7.2. Typical Examples for the Calculated Costs

As already outlined in chapter 5 the curves for the Point-to-Point loss hold for Combined Switching as well as for Separated Switching, as the mapping of both arrays yields the same SDM array. This is the reason why PCM switching arrays, operating in the two different switching modes and therefore having two different sizes, can be treated together within one PCM CHART.
The difference between both switching modes concerning the relative costs, COSTS/TS, will be outlined by means of the following examples.

7.2.1. The TST Array

CHART 5 shows on the right hand side the costs of a TST array (Fig.10) having HW = 36 ML with M = 30 TS each.
Depending on the switching mode the number of connected highways differs:

72 highways are connected for Separated Switching (two identical arrays)
36 highways are connected for Combined Switching (one array of the same type)

The relative costs per TS differ for one array operating in the Combined Switching mode (bold line) and for two arrays operating together in the Separated Switching mode (dashed line) only because of the middle S-stage. The path allocation principles do not allow to save control memories for this middle stage. Therefore, the relative costs increase as this middle stage requires a complete control memory in any case.

7.2.2. The STS Array

CHART 10 shows the costs of the STS array with 25 highways (CSw) or 50 highways (SSw), resp.(Fig.11).
Here the quasisymmetrical path allocation principle leads to identical relative costs for CSw and SSw, resp., as half of the control memories of the middle stage for CSw can be saved.
The discontinuities in the curves at the value of the expansion factor $\beta = 1.28$ result from the increase of the expansion in stage No. 1 from 25|32 to 25|33. For $\beta > 1.28$ a further (6th) memory bit is necessary for addressing the space switches in dual coded form.

7.2.3. The TSST Array

CHART 20 shows the relative costs for a TSST array (Fig. 12) with 196/392 highways. Here the difference of the costs between Combined Switching and Separated Switching is due to the additional "horizontal" links which are necessary for Combined Switching, c.f. chapter 4.5.

7.2.4. The TSSST Array

CHART 43 shows the relative costs for the TSSST array (Fig.13) with 4096/8192 highways, resp. The decrease of the costs for SSw result only from the savings of control memories in the middle stage (c.f. 7.2.1.).

7.2.5. The SSTSS Array

The quasisymmetrical path allocation requires an even number of TSIs in each block formed by the three middle stages.
Depending whether the block size h_2 is even or odd, the costs for CSw and SSw are different.
If the block size h_2 is even (see Fig.20 and 21) the relative costs for CSw and SSw are the same.
However, if the block size h_2 is odd (see Fig. 22 and 23) and therewith the number j_2 of TSIs per block, too, one has to increase the TSIs per block by 1 in order to obtain an even value. This requires $j_2 = h_2 + 1$ and $h_4 = j_4 + 1$ intermediate MLs per block. Consequently Combined Switching becomes more expensive, see also CHART 45 and CHART 46.

7.2.6. The TSSSST Array

CHART 65 shows the relative costs for the TSSSST array (Fig.15) with 1000/2000 highways, resp. Combined and Separated Switching have exactly the same relative costs because of the even number of stages.

8. DERIVATION OF THE DESIGN FORMULAE

8.1. General Remarks

When a symmetrical structure and the number of highways to be connected to has been chosen, the number of MLs terminating in one space switch (ML matrix) or block is the only variable remaining free. This variable, however, is responsible for the number of blocks and has a significant influence on the costs of the whole PCM array.
There are different boundary conditions that can be applied in order to find that block size which guarantees minimal costs for the switching array.

The basic idea is either to minimize the number of gates, as the gates appear as the most expensive elements, or to minimize the costs of the array as a whole.

Two gate minimization modes will be discussed first.
It should be noticed that all presented optimization modes are only valid for PCM arrays having more than 4 stages.

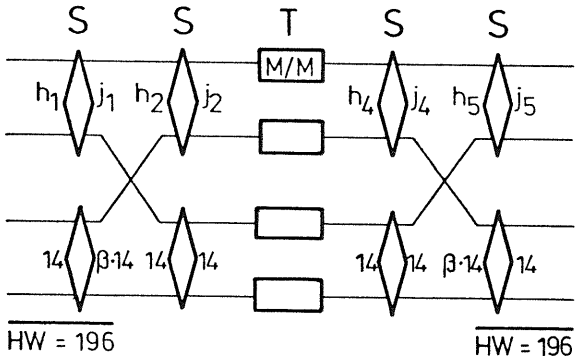


Fig. 20: Design Example of a SSTSS Array, Even Value of the Block Size HW = 196, M = 30

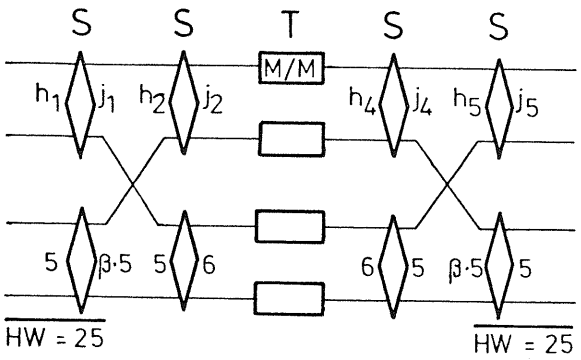


Fig. 22: Design Example of a SSTSS Array, Odd Value of the Block Size HW = 25, M = 30,

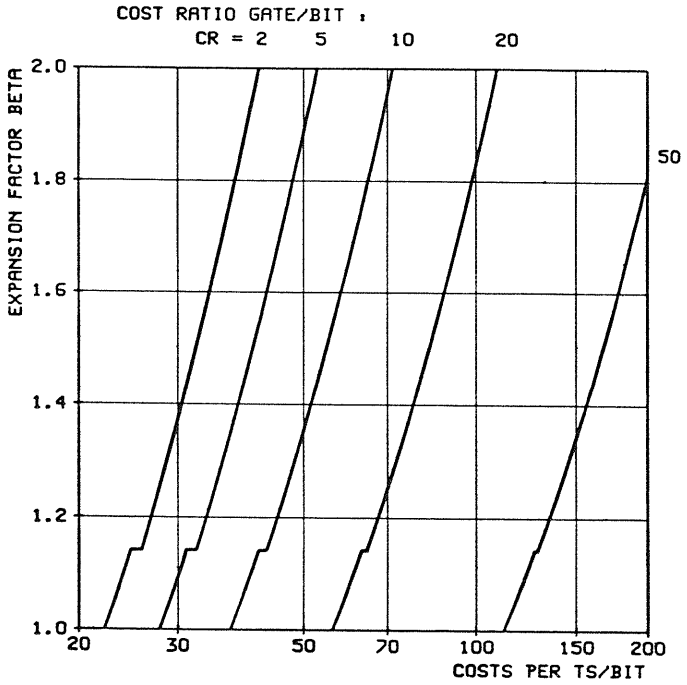


Fig. 21: Costs of a SSTSS Array, HW = 196, M = 30

——— { *Combined Switching*
Separated Switching

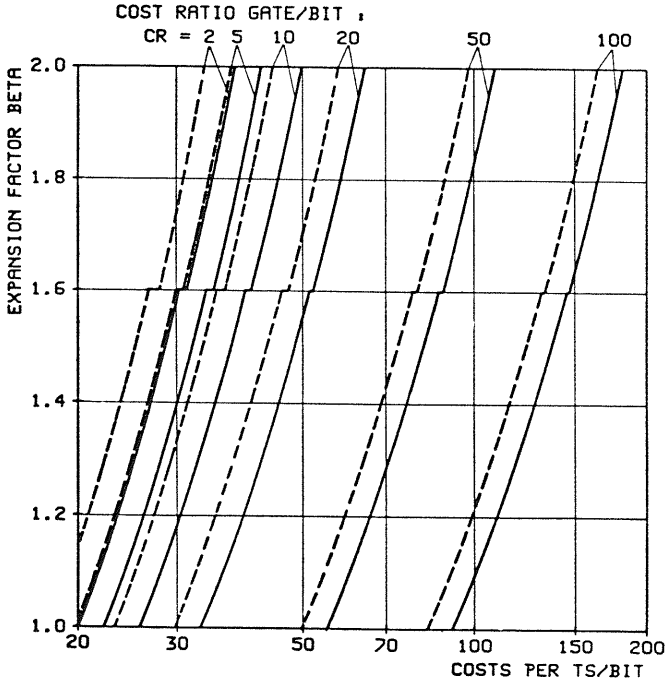


Fig. 23: Costs of a SSTSS Array, HW = 25, M = 30

——— *Combined Switching*
– – – *Separated Switching*

The design of PCM arrays having 4 or less stages is already fixed by the prerequisite of symmetrical arrays.
The TSSST array may serve as an example for the derivation of the formulae, see Fig. 24.

As prerequisites for both design modes hold:

- the arrays are symmetrically structured (I)
- expansion and the corresponding concentration are performed in the first and the last stage (II)
- the intermediate stages switch 1:1 (III)
- only switching arrays with "single linkage" (SL) wiring are considered (IV)

Here SL wiring means that exactly one multiplex-line leads from a space switch or block to a consecutive space switch or block in the following stage.
It can be defined as follows, e.g. for the TSSST array (Fig.24):

$$j_2 = g_3 = h_4$$
$$g_2 = h_3 \ , \ j_3 = g_4$$

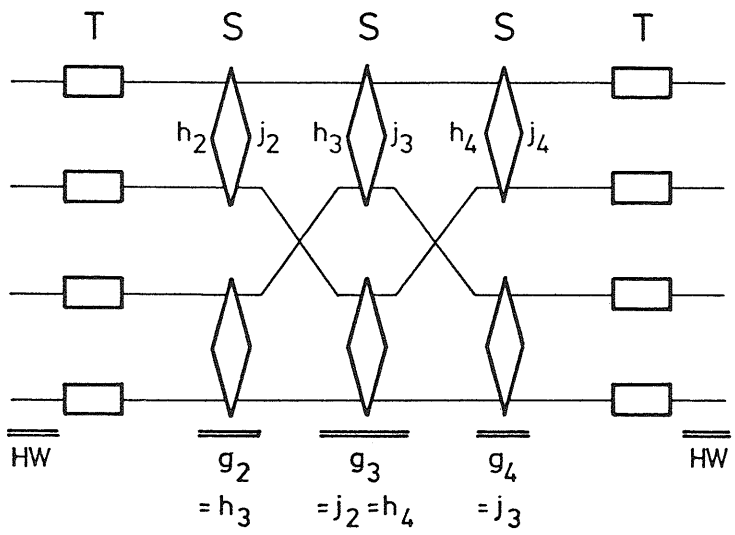


Fig. 24: The TSSST Array

If SL wiring is applied the following formula holds for the number of MLs being connected on each side of the PCM array.

$$HW = \prod_{j=1}^{[S/2+1]} h_j \qquad (1)$$

Note: Only the space stages must be counted by the variable j.

[ ] means the next lower integer value.

For the TSSST array it holds for the number HW of MLs on each side :

$$HW = h_2 \cdot h_3$$

8.2. Gate Minimization Mode PCM 1

The mode PCM 1 starts by calculating the number of gates per incoming external multiplex-line (GPM).

$$GPM = j_1 + \beta(j_2 + j_3 + j_i + .. + j_s) \qquad (2)$$

Note: Only these stages must be included in the sum, which are space stages. The expansion factor $\beta = j_1/h_1$ has only to be regarded if the first and the last stage are space stages, elsewhere $\beta = 1$.

Now a grade of access from the incoming to the outgoing external multiplex-lines via the intermediate space stages be defined
It depends on the product:

$$P^* = \prod_{i=1}^{S} j_i \qquad (3)$$

Note: Only these subscripts i must be regarded which stand for space stages.

Be considered a constant value P^* which must be achieved with a minimum number of GPM.
The partial derivation of equations (2) and (3) with respect to the outlets j yields (together with prerequisite III) to a uniform matrix size

$$j_i = h_i \qquad (4)$$

This result together with the demand for SL wiring (1) yields the required value for the matrix size:

$$h_i = \sqrt[[S/2+1]]{HW} \qquad (5)$$

As an example, this derivation is shown for a TSSST array:

$$GPM = 1\cdot(j_2 + j_3 + j_4) \qquad (2a)$$

$$P^* = j_2 \cdot j_3 \cdot j_4 \qquad (3a)$$

from (3a)

$$j_2 = \frac{P^*}{j_3 \cdot j_4}$$

$$\frac{\partial GPM}{\partial j_3} = \frac{-P^*}{j_3^2 \cdot j_4} + 1 = 0 \Longrightarrow j_3 = \frac{P^*}{j_3 \cdot j_4}$$

$$\frac{\partial GPM}{\partial j_4} = \frac{-P^*}{j_3 \cdot j_4^2} + 1 = 0 \Longrightarrow j_4 = \frac{P^*}{j_3 \cdot j_4}$$

and therefore:

$$j_2 = j_3 = j_4$$

Observing the prerequisites I and III one gets:

$$h_2 = j_2 = h_3 = j_3 = h_4 = j_4 \qquad (4a)$$

with (5) one obtains:

$$h_2 = h_3 = h_4 = \sqrt[2]{HW} \qquad (5a)$$

8.3. Gate Minimization Mode PCM 2

Also the minimization mode PCM 2 starts with the number of gates per incoming external ML (GPM):

$$GPM = j_1 + \beta(j_2 + j_i + .. + j_S) \qquad (2)$$

Note: Only these subscripts i must be regarded which stand for space stages.

The condition of SL wiring is taken into account right now,

$$HW = \prod_{j=1}^{[S/2+1]} h_j \ , \qquad (1)$$

without prescribing the product P*.

Partial derivation of equ.(2) and (3) with respect to the outlets j leads together with the symmetry condition I to different matrix sizes.
This will be outlined in detail for the TSSST array:

$$GPM = j_2 + j_3 + j_4 \qquad (2b)$$

$$HW = j_2 \cdot j_3 \qquad (1b)$$

Partial derivation of (2b) together with (1b) yields

$$\frac{\partial GPM}{\partial j_3} = -2 \cdot \frac{HW}{j_3^2} + 1 = 0 \Longrightarrow j_3 = \sqrt[2]{2 \cdot HW}$$

and with (1b)

$$j_2 = \frac{HW}{j_3} = \frac{HW}{\sqrt[2]{2 \cdot HW}} = \sqrt[2]{HW/2}$$

The final matrix sizes follow from I and III

$$h_3 = j_3 = 2h_2 = 2j_2 = 2h_4 = 2j_4 \qquad (4b)$$

The resulting design formulae of these two minimization modes PCM 1 and PCM 2 for the presented array types are shown in Table 2.

8.4. Examples for the Use of Design Mode PCM 1 and PCM 2

Five Stage TSSST Array

Fig. 25 shows a 5-stage PCM switching array of the type TSSST with about 1500 incoming as well as outgoing speech directions. The array is designed according to the modes PCM 1 and PCM 2 (the values in paranthesis hold for the design according to mode PCM 2).
The mode PCM 1 yields, for 49 MLs per side of the array, uniform matrices with $h_2=j_2=h_3=j_3=h_4=j_4= 7$.
The mode PCM 2 yields two different matrix sizes, namely $h_2=j_2=h_4=j_4=5$ and $h_3=j_3=10$. Therewith 50 MLs are connected to the TSIs of the T-stages on each side .
It should be focused upon the fact that an expansion between inlets and outlets of the first stage is performed in both cases only by increasing the number of internal time-slots per ML. The number of MLs and the size of the matrices remains constant.

Table 2:

PCM 1	PCM 2
S = 3: TST $h_2=j_2=HW$ $M^*=\beta\cdot M$	S = 3: TST, STS S = 4: TSST like PCM 1
S = 3: STS $h_1=j_3=HW$ $j_1=h_3=\beta\cdot h_1$	S = 5: TSSST $h_2=j_2=h_4=j_4=\sqrt[2]{HW/2}$ $h_3=j_3=2\cdot h_2$ $M^*=\beta\cdot M$
S = 4: TSST $h_2=j_2=h_3=j_3=\sqrt[2]{HW}$ $M^*=\beta\cdot M$	S = 5: SSTSS like PCM 1 (only 2 space stages contribute to the HW-access)
S = 5: TSSST $h_2=j_2=h_3=j_3=h_4=j_4=\sqrt[2]{HW}$ $M^*=\beta\cdot M$	
S = 5: SSTSS $h_1=h_2=j_2=h_4=j_4=j_5=\sqrt[2]{HW}$ $j_1=h_5=\beta\cdot h_1$	S = 6: TSSSST $h_2=j_2=h_5=j_5=\sqrt[3]{\frac{HW}{4}}$ $h_3=j_3=h_4=j_4=2\cdot h_2$ $M^*=\beta\cdot M$
S = 6: TSSSST $h_2=j_2=h_3=j_3=h_4=j_4=h_5=j_5=\sqrt[3]{HW}$ $M^*=\beta\cdot M$	

Fig. 26 shows diagrams for these two TSSST arrays. In the diagram on the left hand side, the Point-to-Point loss B_{pp} is prescribed with 0.1% or 1.0%. The curves show the necessary expansion β in the first stage versus the carried traffic per time-slot.

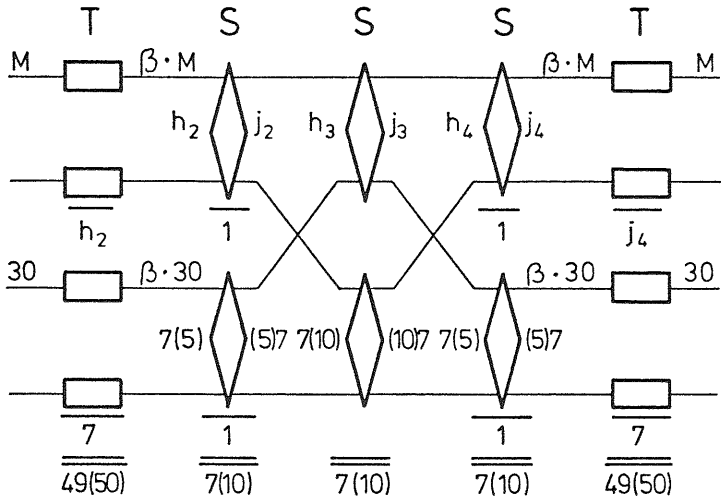


Fig. 25: Five Stage Array Designed According to Mode PCM 1 and PCM 2

As one can see the expansion β for the mode PCM 2 is for a constant loss probability somewhat greater for all values Y/TS. This compensates the fact that the design mode PCM 2 minimizes the gate requirement without regarding the "transparency" condition P* according to equ.(3).

The right hand diagram yields the corresponding relative costs per TS for each triple (Y/TS, β, B_{pp}).
The marked example gives for Y/TS = 0.8 Erl and for B_{pp} = 0.1% the relative costs for both arrays. In this example, the array according to PCM 1 is slightly cheaper than that one, designed with mode PCM 2. The difference decreases as the cost ratio increases.
Also PCM arrays can be found where mode PCM 2 is slightly cheaper than mode PCM 1.

Regarding the small difference of costs, as well as the advantage of uniform matrices in all space stages, all switching arrays, being presented in the PCM CHARTS, are designed according to mode PCM 1.

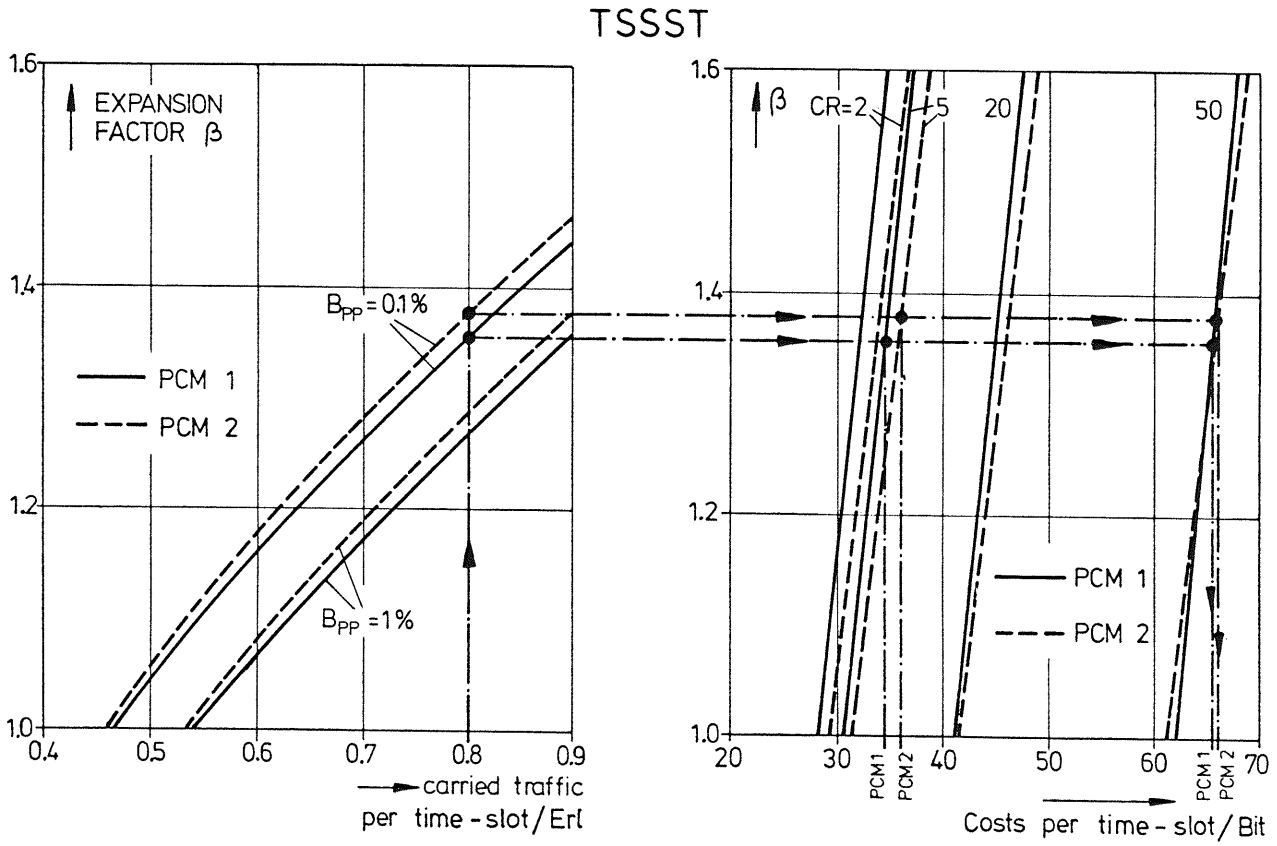


Fig. 26: Comparison of the Relative Costs for the TSSST Array as shown in Fig. 25, Designed According to Mode PCM 1 and PCM 2, resp.

8.5. Overall Cost Minimization of PCM Switching Arrays

The third method for designing cost minimum PCM switching arrays is to minimize the costs of gates and speech memories and the respective control memories as a whole. This can be done by differentiating the overall cost formula of a PCM switching array,as shown in chapter 7, with respect to the inlets and outlets of the space switches. Also this principle is only applicable for PCM arrays having 5 and more stages. The design for arrays with less than 5 stages is already determined by the demand of a symmetrical structure.
This overall cost minimization was applied to all PCM arrays having more than two space stages. Here, the minimum costs depend on the size of the space switches and their respective control memories; the number of the time-slot interchanges of the T-stages has no influence.
The result is, that the difference of the costs between only gate minimal arrays and overall least-cost arrays is negligible.

There are two reasons:

First:Strictly optimal values for the size of the space switches and the control memories can normally not be observed, because only integer values of inlets and outlets can be realized. The same holds for the memory bits per storage place.

Second: Overall cost minimization generally yields smaller space switches in the first and the last S-stage than even the gate minimal solution (mode PCM 2). As a rule the expansion factor β therefore has to be remarkably increased in order to achieve a prescribed grade of service. Consequently, the costs increase and the desired savings may again be compensated.

Overall cost minimization has been checked for many PCM arrays.
The result was always as described above.Therefore, this third cost minimization principle will not be applied.

Acknowledgement:

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9. References

/ 1/ BAZLEN, D., KAMPE, G., LOTZE, A.: On the Influence of Hunting Mode and Link Wiring on the Loss of Link Systems
a) 7th ITC, Stockholm 1973, Proc. pp 232/1-12.
b) Information Express "Information Transmission", Moscow, Sept. 1973, No. 35, pp. 11-39 (in Russian).

/ 2/ BAZLEN, D., KAMPE, G., LOTZE, A.: Design Parameters and Loss Calculation of Link Systems.
IEEE-COM 22 (1974) 12, pp. 1908-1920.

/ 3/ BIESZCZAD, E.S., KOWALIK, R.F., KRYLOW, K.E., MACRANDER, M.S:
No. 3 EAX Network and Master Clock.
GTE Automatic Electric Journal, July 1977.

/ 4/ CIESLAK, T.J., HICKSON, P.J.: Analysis and Simulation of No. 4 ESS Network Performance
IEEE Trans. Comm., No. 1, Jan. 1979

/ 5/ COUDREUSE, J.P., GRALL, P., RAPHALEN, C.: Système E10 centres de transit temporels.
Commutation et Electronique, No. 43, Oct. 1973.

/ 6/ CLOS, C.: A Study of nonblocking Switching Networks.
BSTJ, Vol. 32 (1953), pp. 406-424.

/ 7/ HOLM, R.K.: No. 3 EAX Description.
GTE Automatic Electric Journal, July 1977

/ 8/ HUBER, M.: On the Congestion in TDM Systems.
4th ITC, London 1964, Doc. 104.

/ 9/ KOBYLAR, A.W.: Methodology for Isolating a Set of Near Optimum PCM Digital Network Configurations.
ICC Minneapolis 1974, Proc. pp. 34E1-5.

/10/ LOTZE, A.: Optimum Link Systems.
a) 5th ITC, New York 1967, Pre-book pp. 242-251.
b) Field Engineering Methods for Economic Network Planning, Proc.XX, Int. Meeting, The Institut of Management Science, Tel Aviv, Vol.I, pp. 159-167.

/11/ LOTZE, A., RÖDER, A., THIERER, G.: PPL - A Reliable Method for the Calculation of Point-to-Point Loss.
a) 8th ITC, Melbourne 1976, Proc. pp. 547/1-14.
b) ICC 77, Chicago, Proc. Vol.I, pp. 213-226.

/12/ LOTZE, A., RÖDER, A., THIERER, G.: Investigations on Folded and Reversed Link Systems.
a) 8th ITC, Melbourne 1976, Proc. pp. 544/1-5.
b) ICC 77, Chicago, Proc. Vol.I, pp. 232-236.

/13/ LOTZE, A., RÖDER, A., THIERER, G.: Point-to-Point Selection versus Point-to-Group Selection in Link Systems.
a) 8th ITC, Melbourne 1976, Proc. pp. 541/1-5.
b) ICC 77, Chicago, Proc. Vol.I, pp. 227-231.

/14/ LOTZE, A., RÖDER, A., THIERER, G.: Nik-Charts for the Design of Link Systems Operating in the Point-to-Point Selection Mode or Point-to-Group Selection Mode.
Supplement to the Congress Papers No. 541, 544, 547 distributed at the 8th ITC, Melbourne 1976.

/15/ LOTZE, A., RÖDER, A., THIERER, G.: Point-to-Point Loss in Case of Multiple Marking Attempts.
Supplement to the Congress Papers No. 541, 544, 547 distributed at the 8th ITC, Melbourne 1976.

/16/ LOTZE, A., RÖDER, A., THIERER, G.: On the Point-to-Point Loss in the Link Systems with Symmetrical or Interleaved Link Wiring.
(to be published)

/17/ LOTZE, A., ROTHMAIER, K., SCHELLER, R.: TDM versus SDM Switching Arrays - A Comparison.
9th ITC, Torremolinos 1979, Proc.

/18/ POSTOLLEC, J.: Le réseau de connexion du Système E10.
Commutation et Electronique, No.40, Janv. 1973.

/19/ ROTHMAIER, K., SCHELLER, R.: Design of Economic PCM-Arrays with a Prescribed Grade of Service.
9th ITC, Torremolinos 1979.

/20/ SAITO, T.: An Optimum Design Theory for PCM Toll Switching Networks.
NTC 77, Los Angeles, Proc. pp. 46:1-6.

/21/ SCHELLER, R., WIZGALL, M.: A Local PCM Switching System for Voice and Data.
ISS 76, Paris, Proc. pp. 419-426.

/22/ TANAKA, M.: Nonblocking Switching in Integrated PCM Networks.
6th ITC, München 1970, Proc. pp. 477-478.

/23/ THIERER, G.: Loss Calculation of Subscriber Link Systems.
9th ITC, Torremolinos 1979.

/24/ VAUGHAN, H.E.: An Introduction to No. 4 ESS.
ISS Cambridge 1972, Proc. pp. 19-25.

/25/ Voyer, P., Ballard, M., Ledieu, B.: Réseaux de connexion temporels a grande capacité.
Commutation et Electronique, No.43, Oct. 1973.

PCM SWITCHING ARRAY : TSI

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 4, 9, 16, 25, 36, 49, 64,

SEPARATED SWITCHING : HW = 8, 18, 32, 50, 72, 98, 128,

TIME-SLOTS (TS) PER HW : M = 30 TS

POINT-TO-POINT LOSS, PCT1 : B_{pp} = 0.1, 0.5, 1.0, 5.0, 10.0%

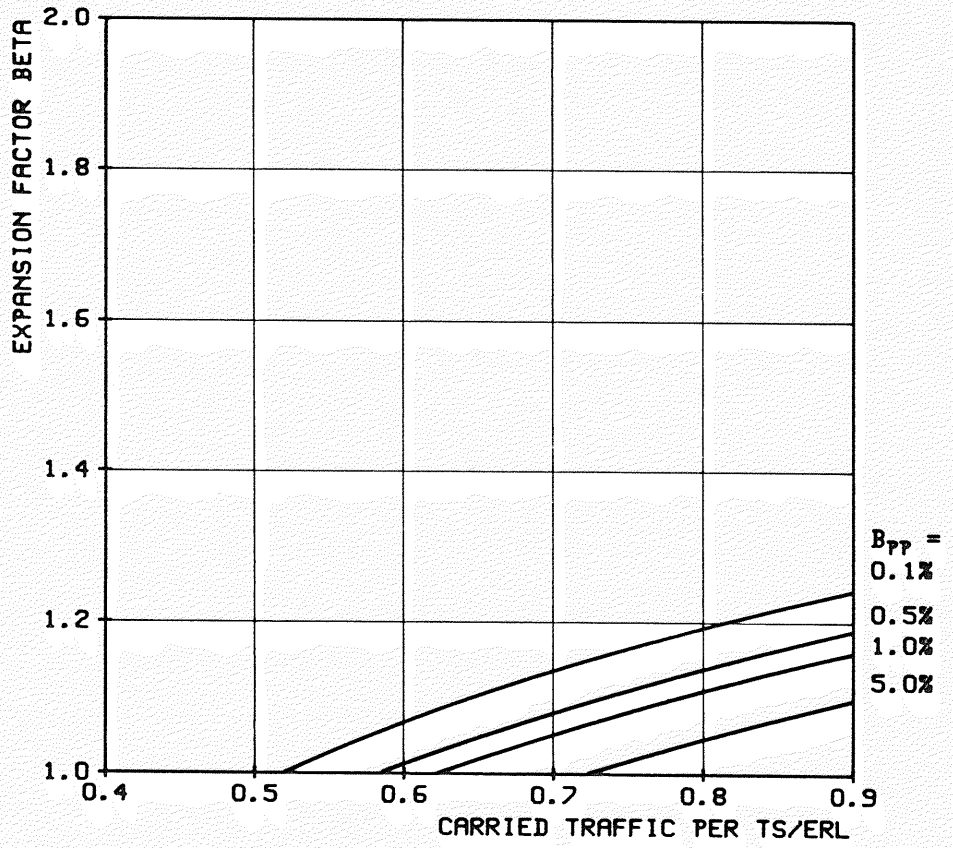
COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

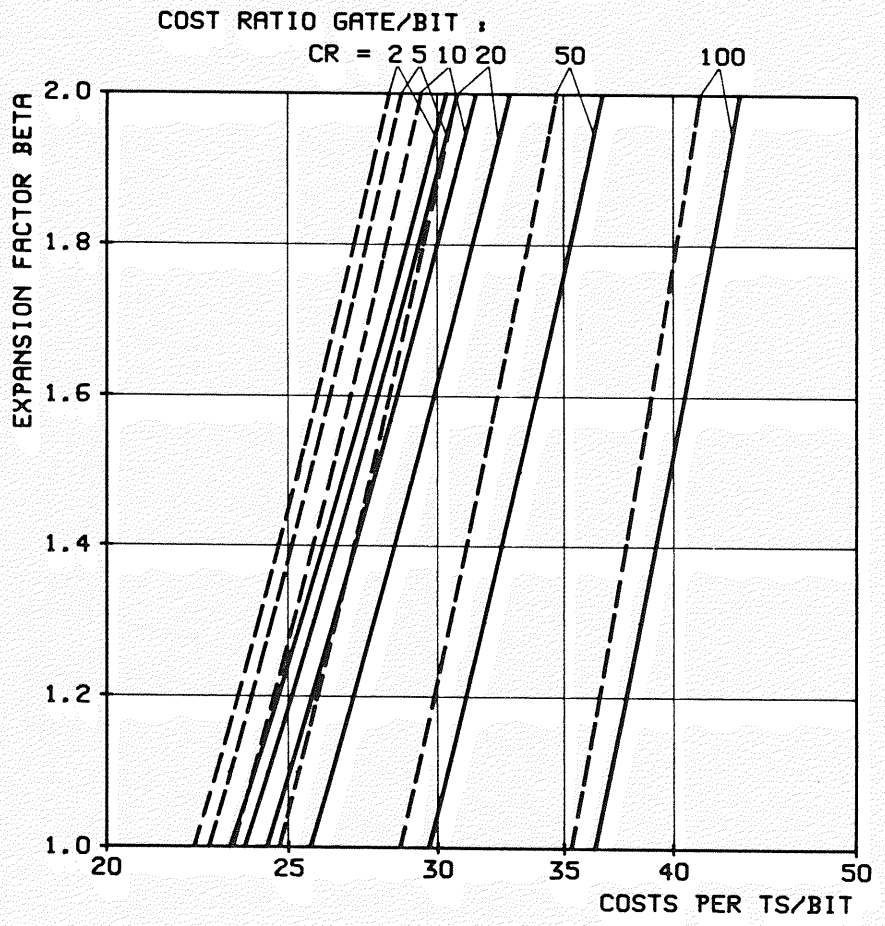
BLOCK SIZE

COMBINED SWITCHING : H_2 = HW

SEPARATED SWITCHING : H_2 = HW/2

TST





COMBINED SWITCHING 1 × 4 HW H_2 = 4

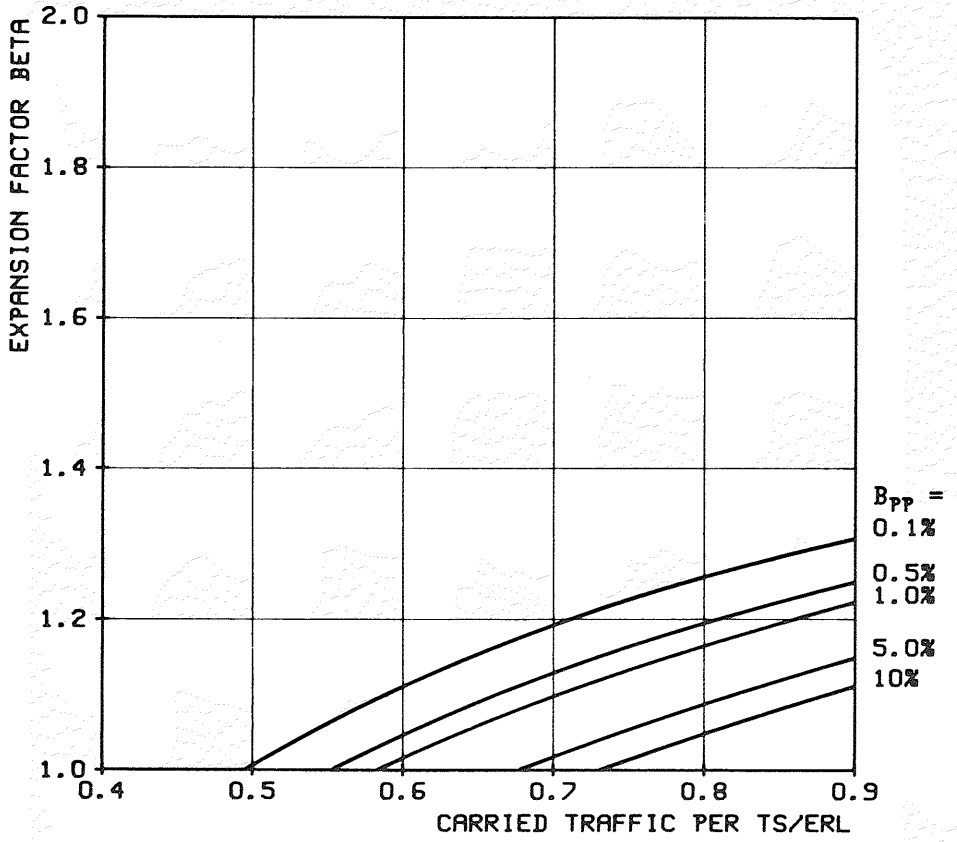
SEPARATED SWITCHING 2 × 4 HW M = 30

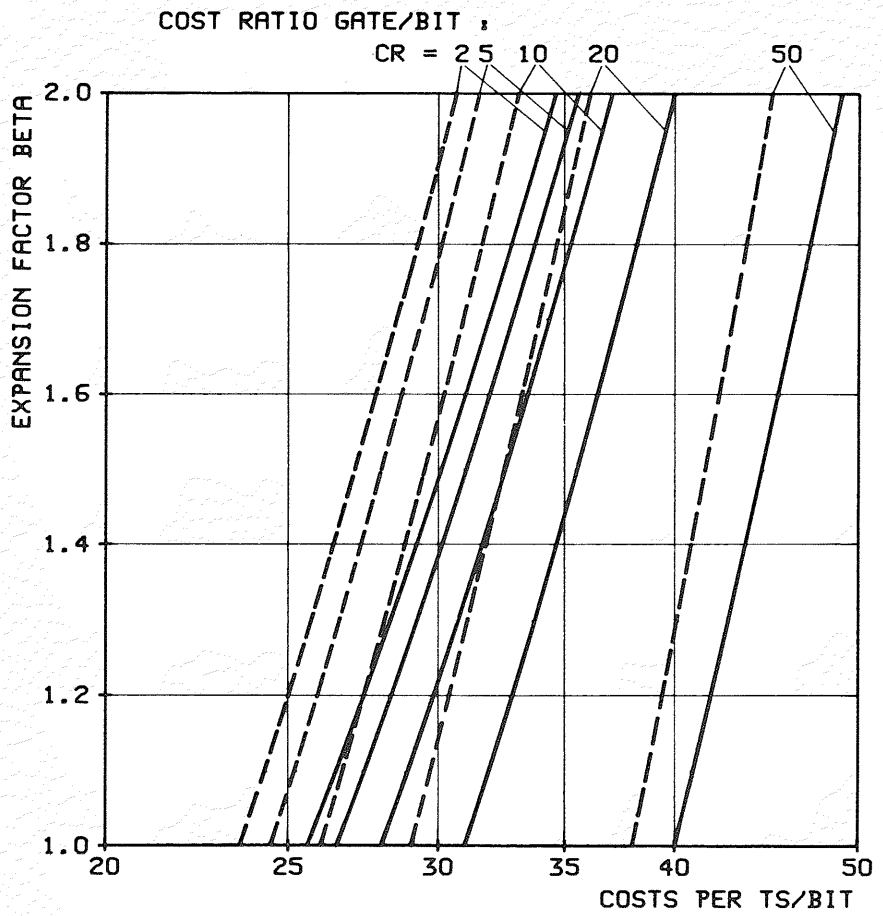
—— COMBINED SWITCHING

--- SEPARATED SWITCHING

-CHART 2-

TST

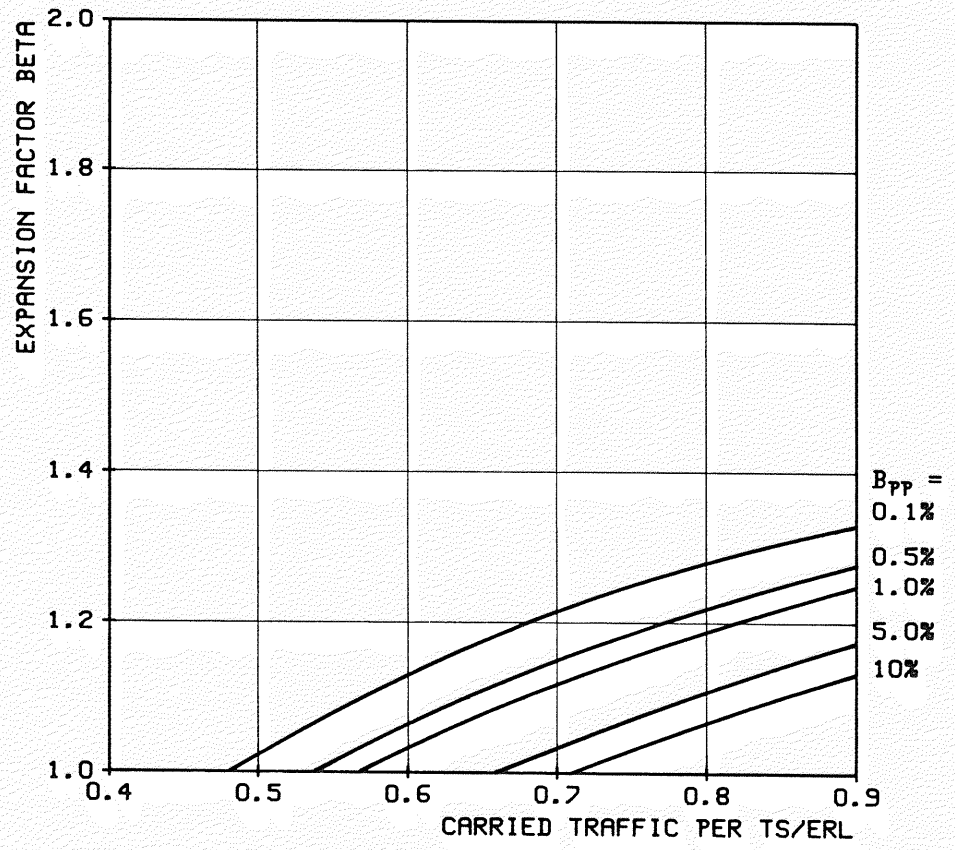


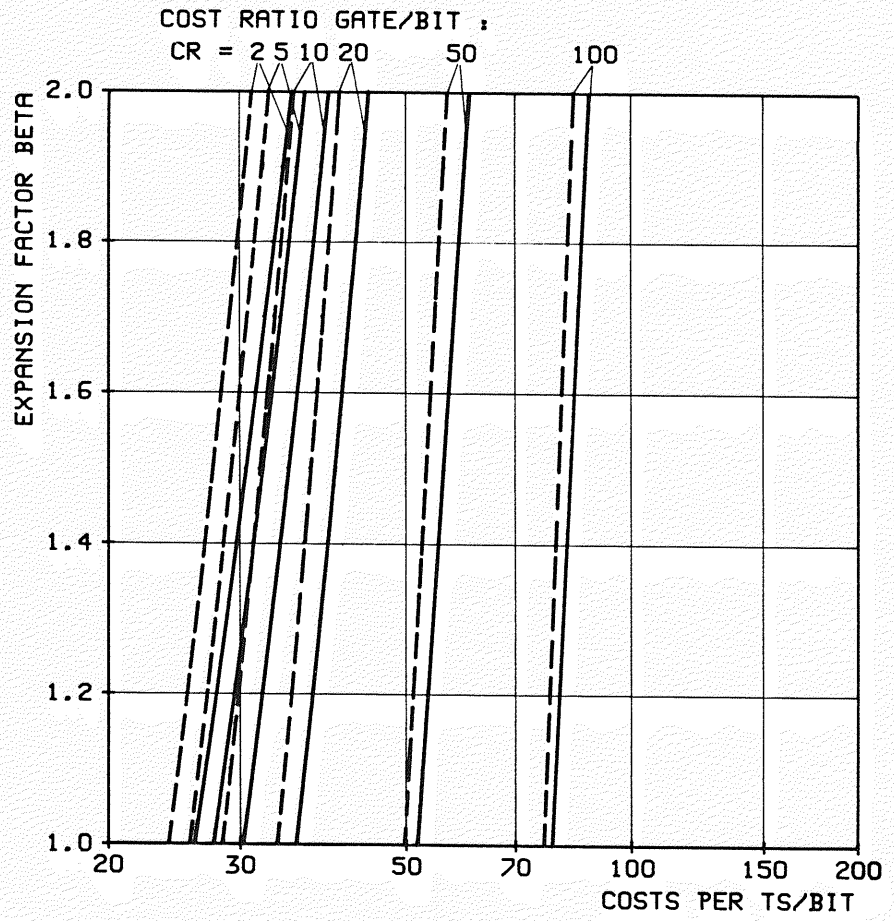


COMBINED SWITCHING 1 × 9 HW H_2 = 9
SEPARATED SWITCHING 2 × 9 HW M = 30

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

TST





COMBINED SWITCHING 1 × 16 HW H_2 = 16

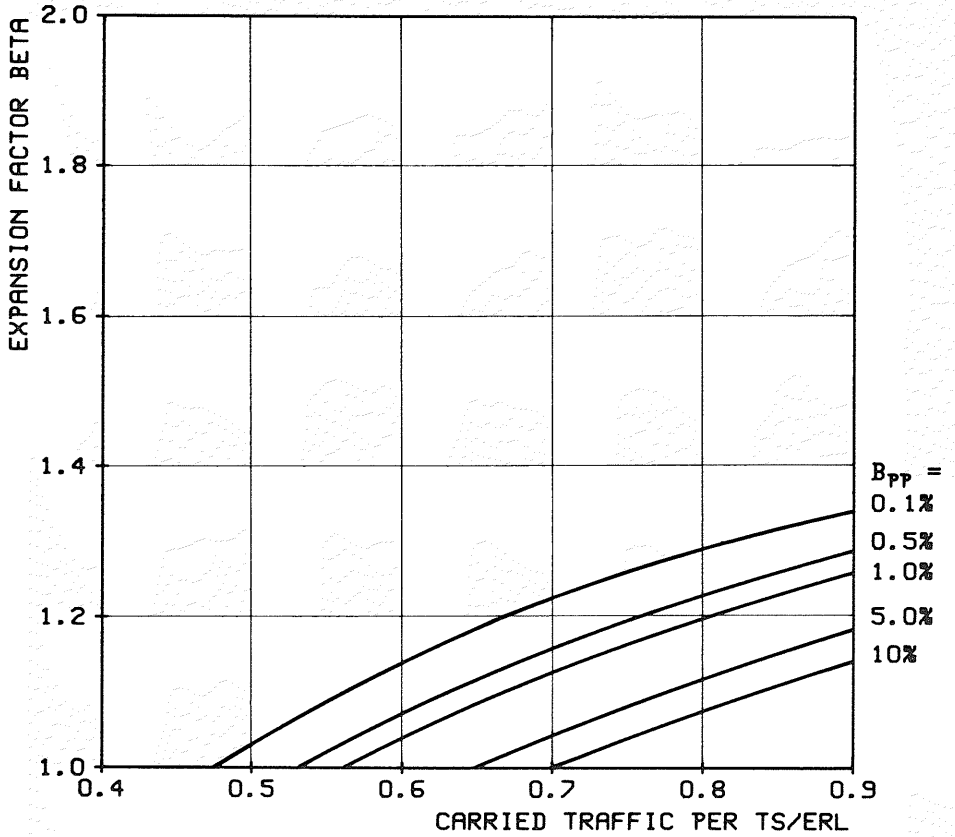
SEPARATED SWITCHING 2 × 16 HW M = 30

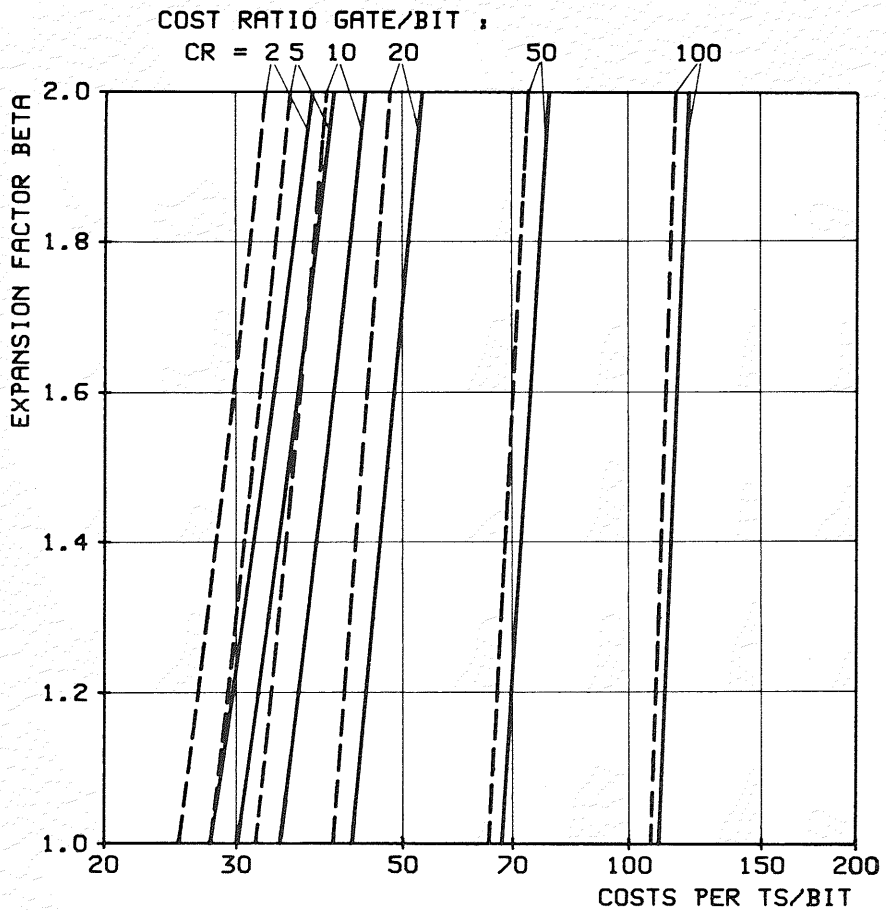
—— COMBINED SWITCHING

--- SEPARATED SWITCHING

-CHART 4-

TST





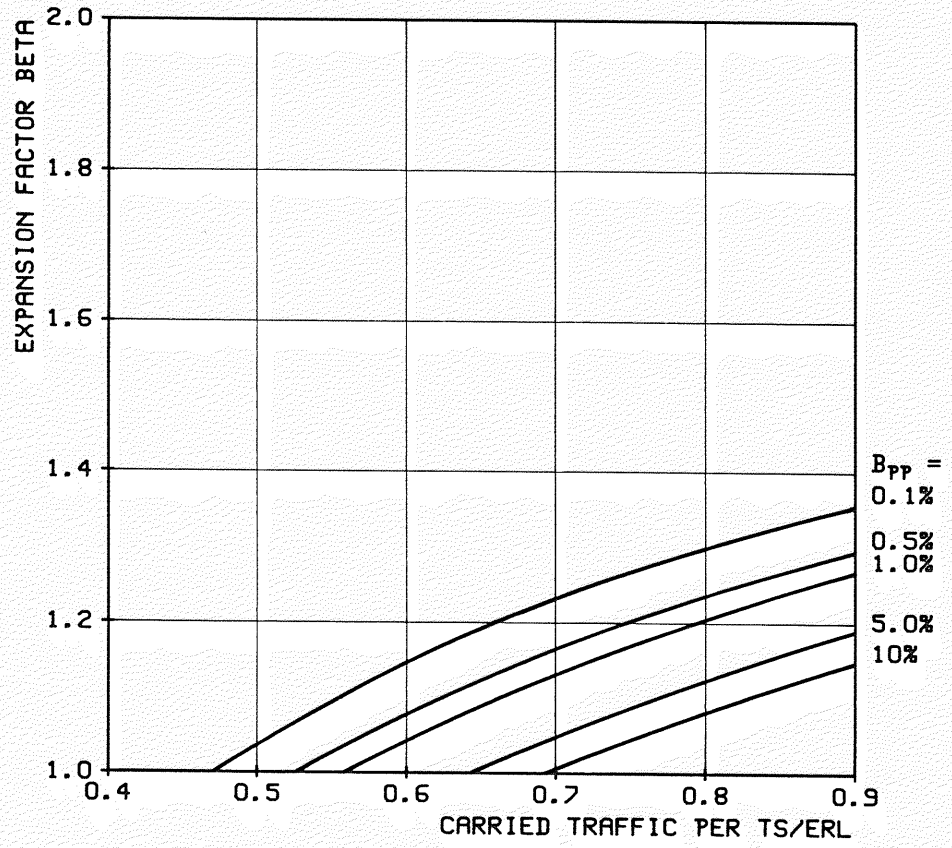
COMBINED SWITCHING 1 × 25 HW H_2 = 25

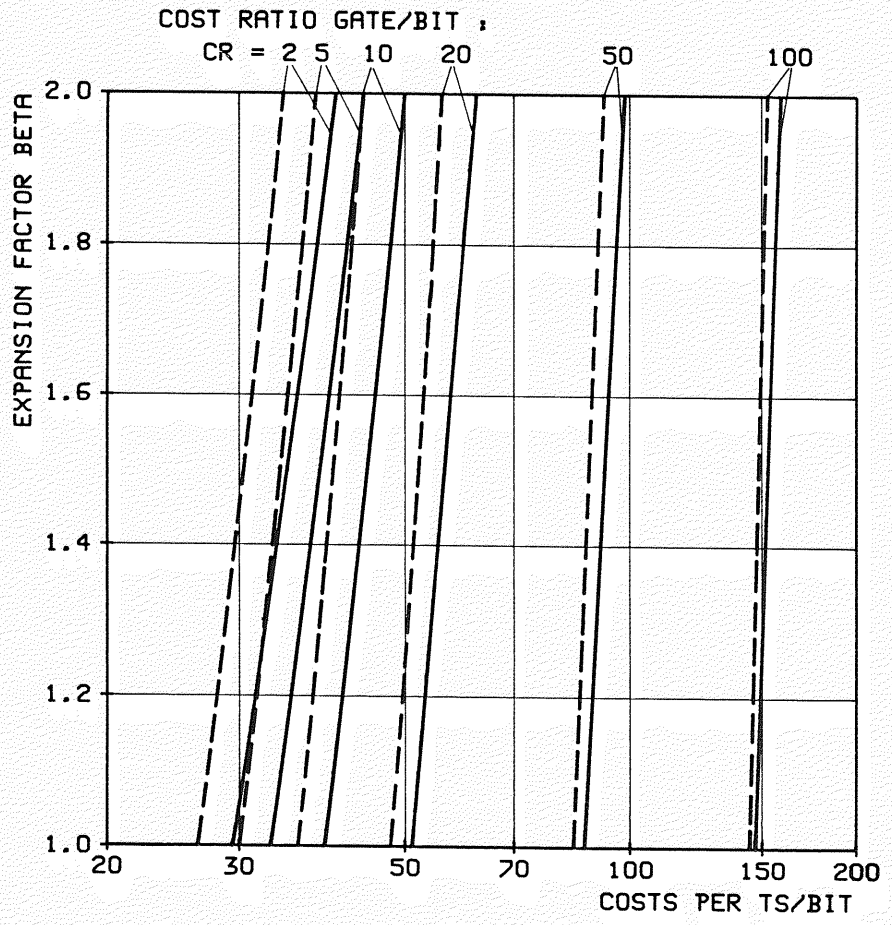
SEPARATED SWITCHING 2 × 25 HW M = 30

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

TST





COMBINED SWITCHING 1 × 36 HW H_2 = 36

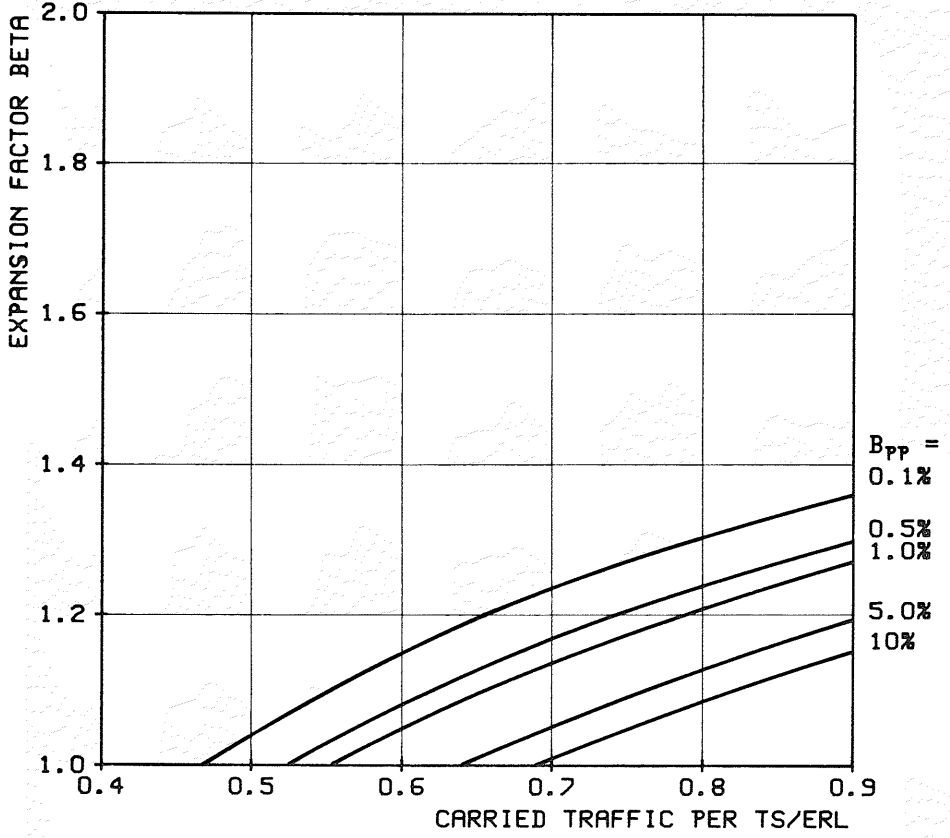
SEPARATED SWITCHING 2 × 36 HW M = 30

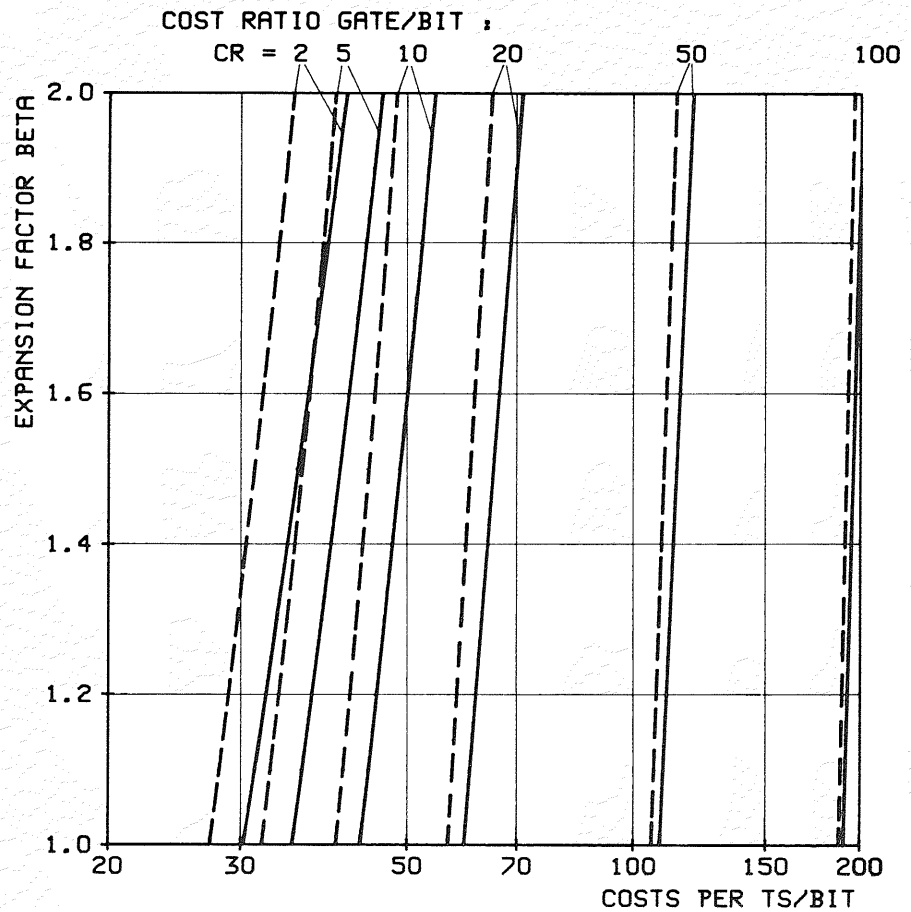
—— COMBINED SWITCHING

--- SEPARATED SWITCHING

-CHART 6-

TST





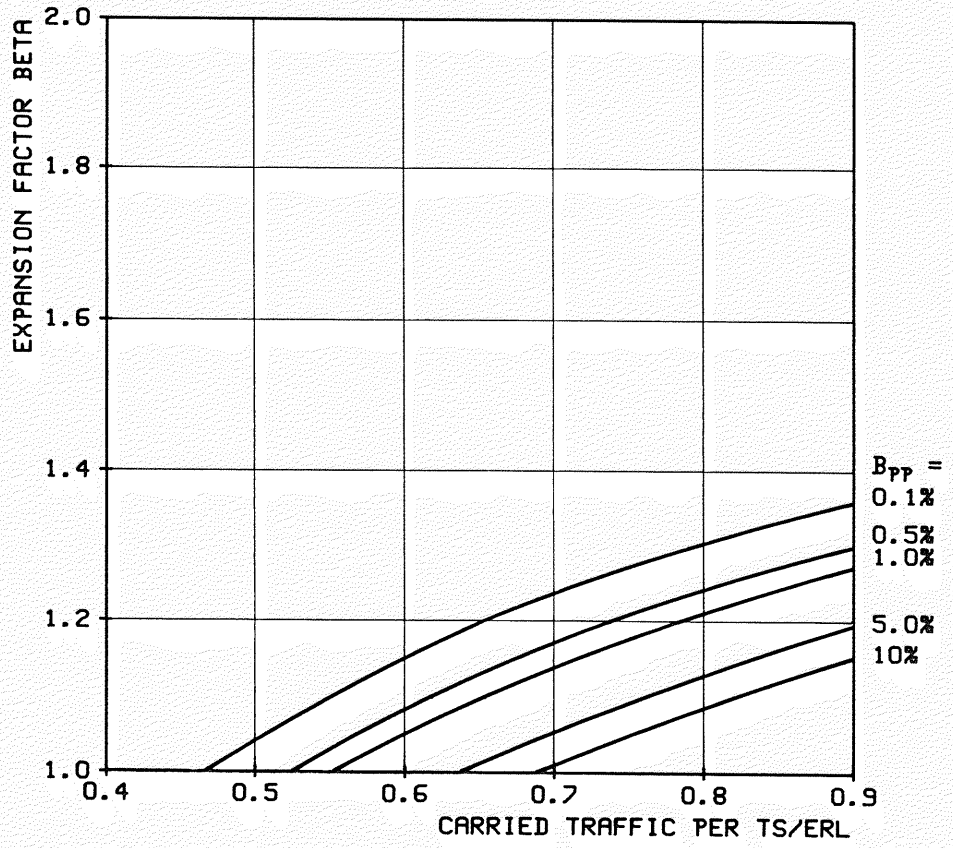
COMBINED SWITCHING 1 × 49 HW H_2 = 49

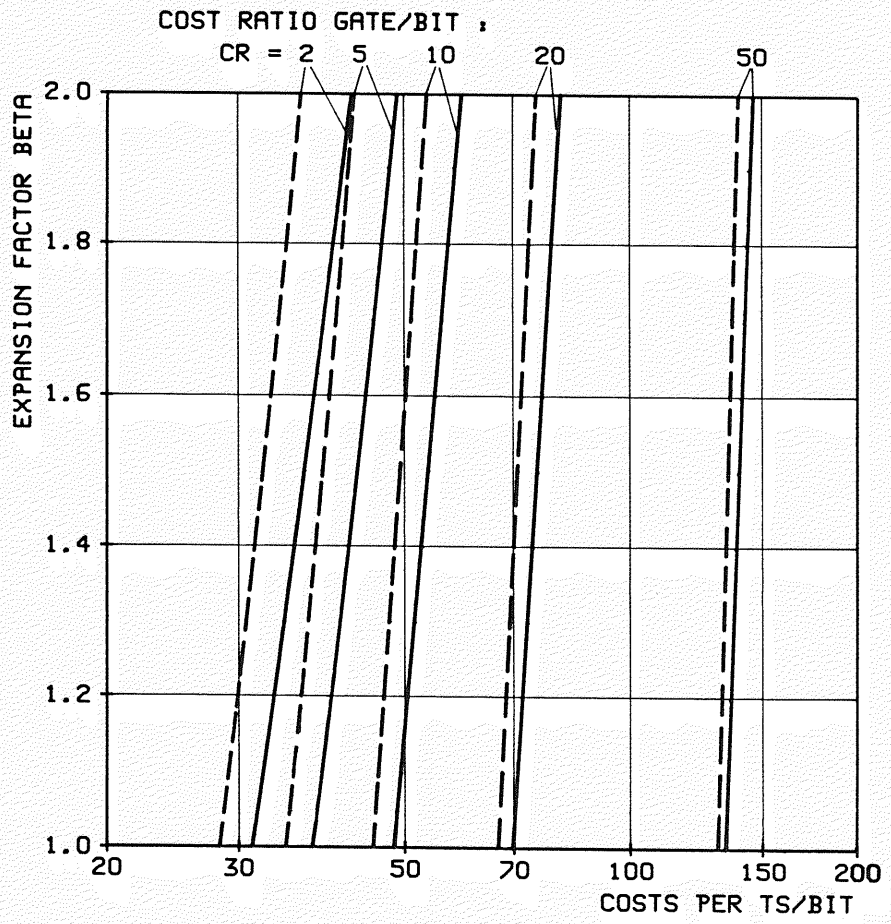
SEPARATED SWITCHING 2 × 49 HW M = 30

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

TST





COMBINED SWITCHING 1 × 64 HW H_2 = 64

SEPARATED SWITCHING 2 × 64 HW M = 30

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

PCM SWITCHING ARRAY : STS

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 9, 16, 25, 36, 49, 64,

SEPARATED SWITCHING : HW = 18, 32, 50, 72, 98, 128,

TIME-SLOTS (TS) PER HW : M = 30 TS

POINT-TO-POINT LOSS, PCT1 : B_{PP} = 0.1, 0.5, 1.0, 5.0, 10.0%

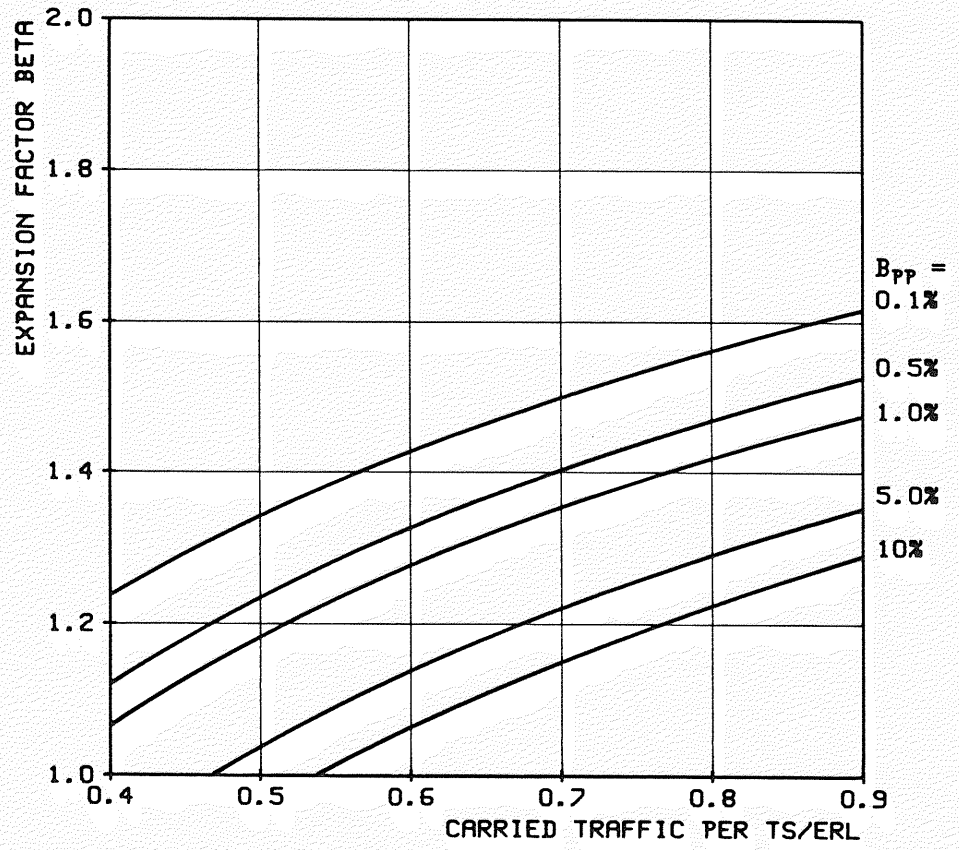
COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

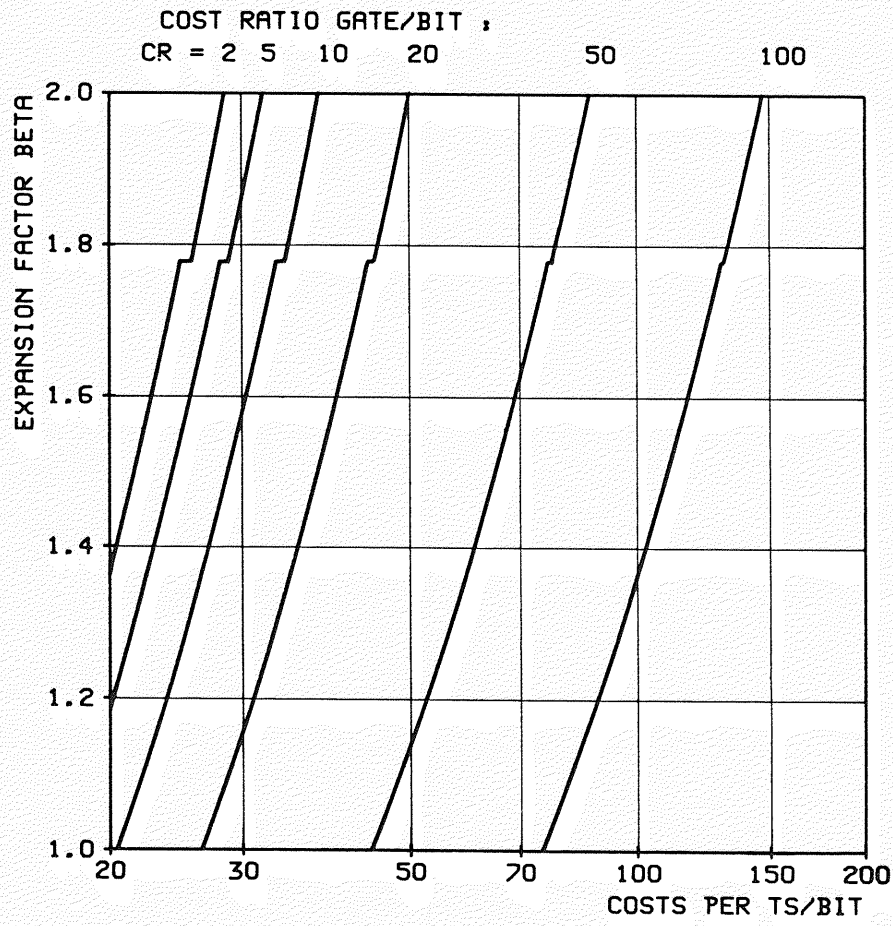
BLOCK SIZE

COMBINED SWITCHING : H_1 = HW

SEPARATED SWITCHING : H_1 = HW/2

STS

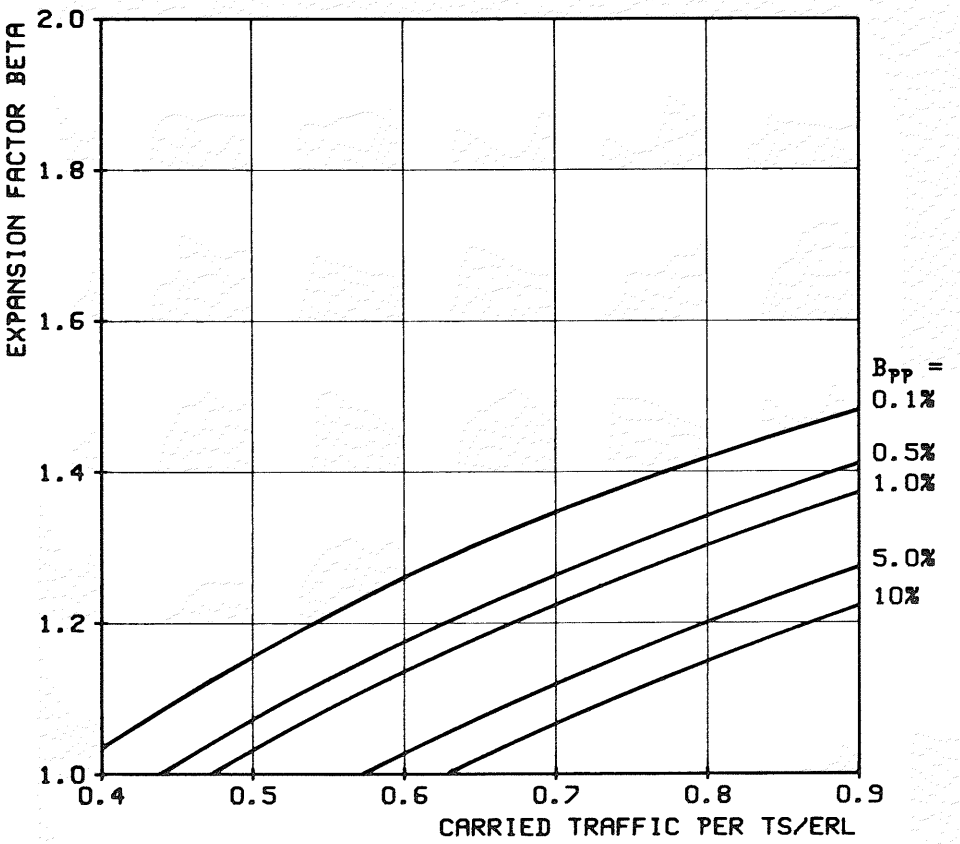


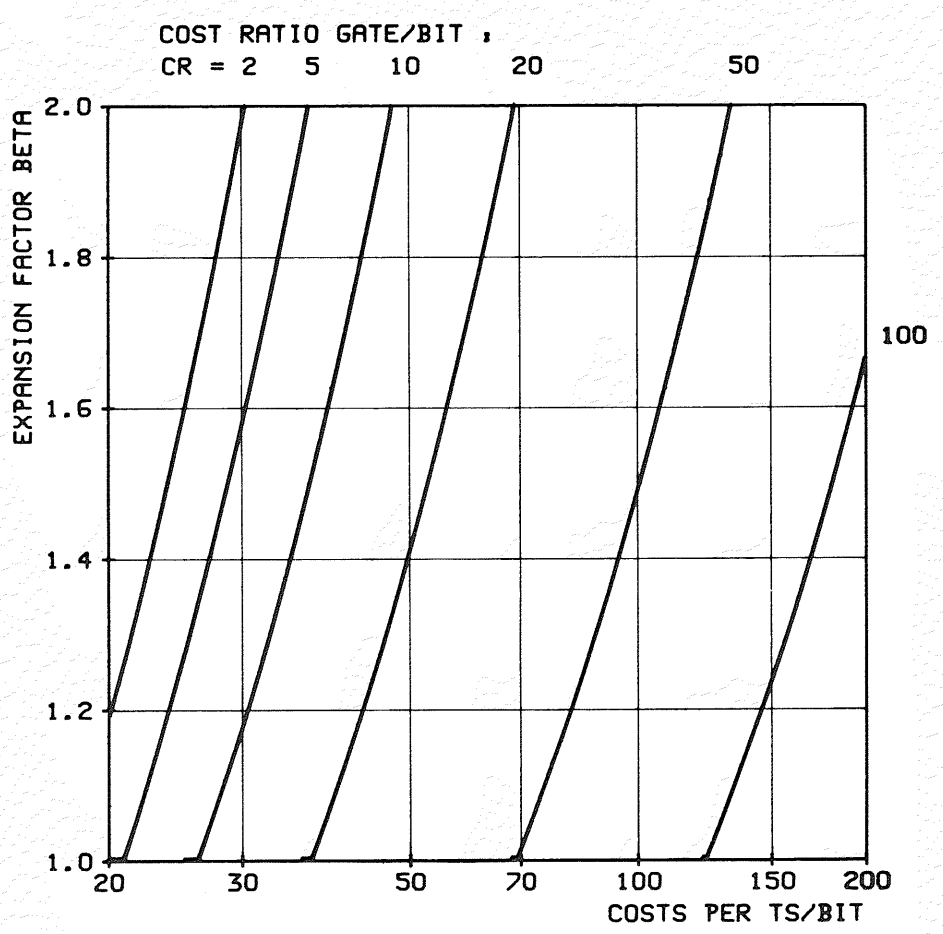


COMBINED SWITCHING	1 × 9 HW	H_1 = 9	—— { COMBINED SWITCHING
SEPARATED SWITCHING	2 × 9 HW	M = 30	{ SEPARATED SWITCHING

-CHART 9-

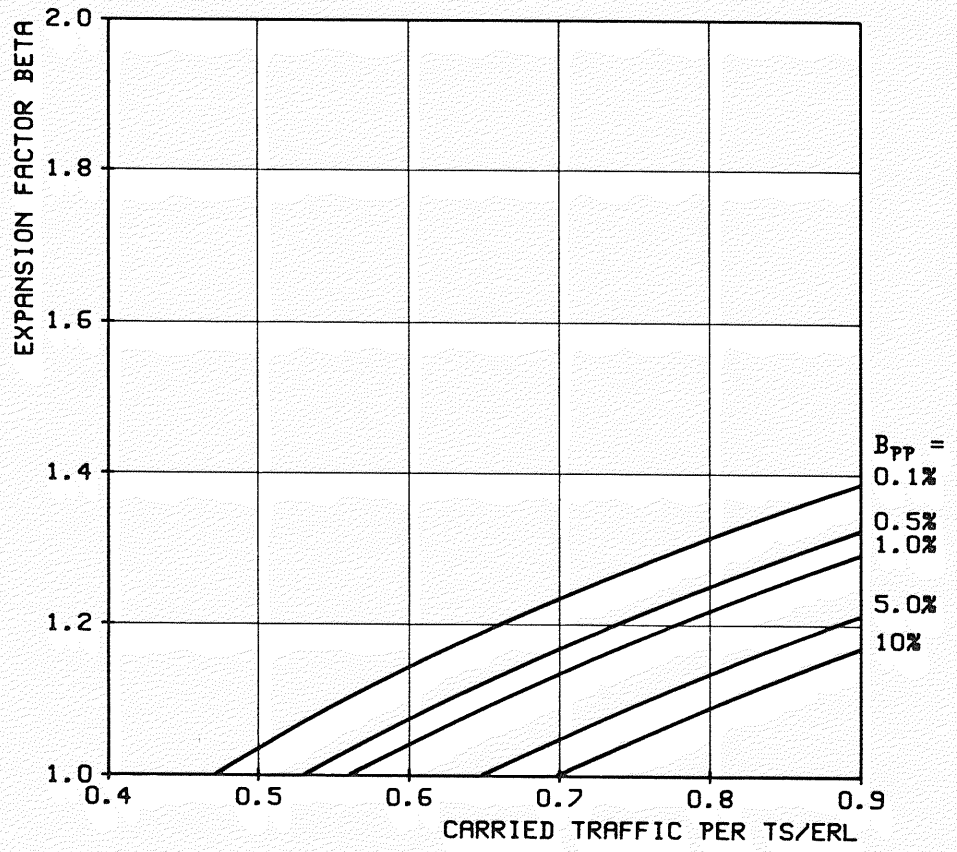
STS

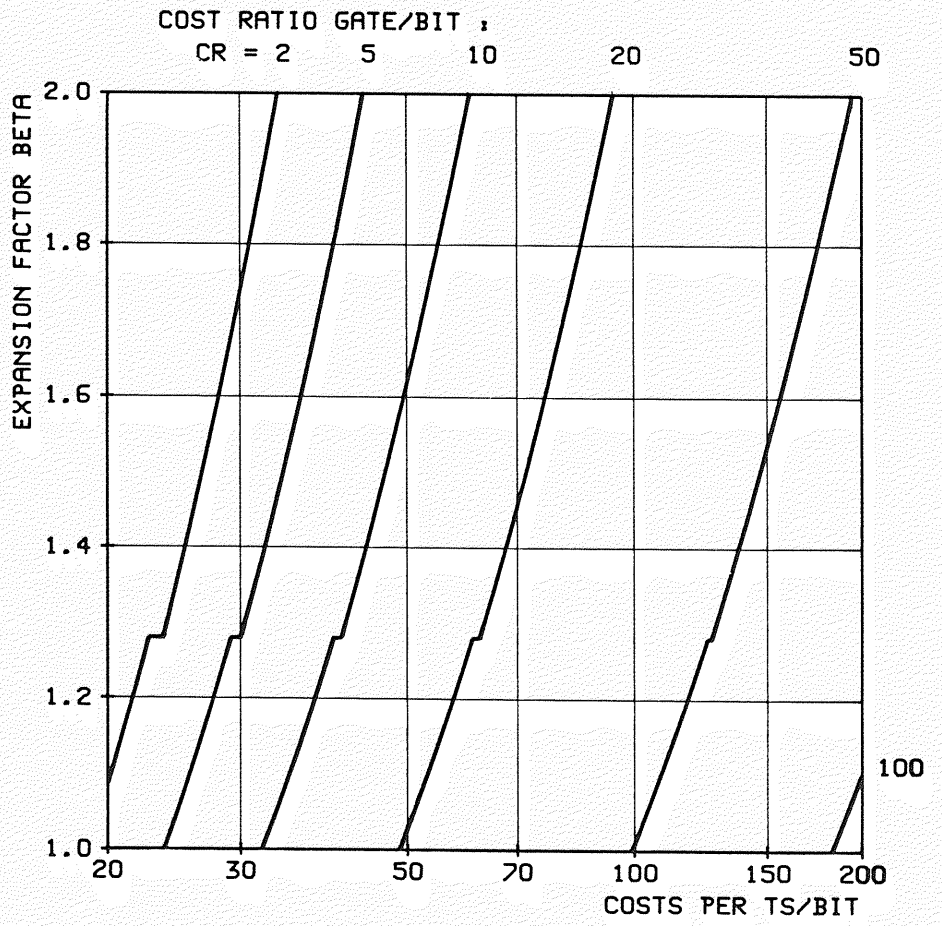




COMBINED SWITCHING	1 × 16 HW	H_1 = 16	—{ COMBINED SWITCHING
SEPARATED SWITCHING	2 × 16 HW	M = 30	{ SEPARATED SWITCHING

STS

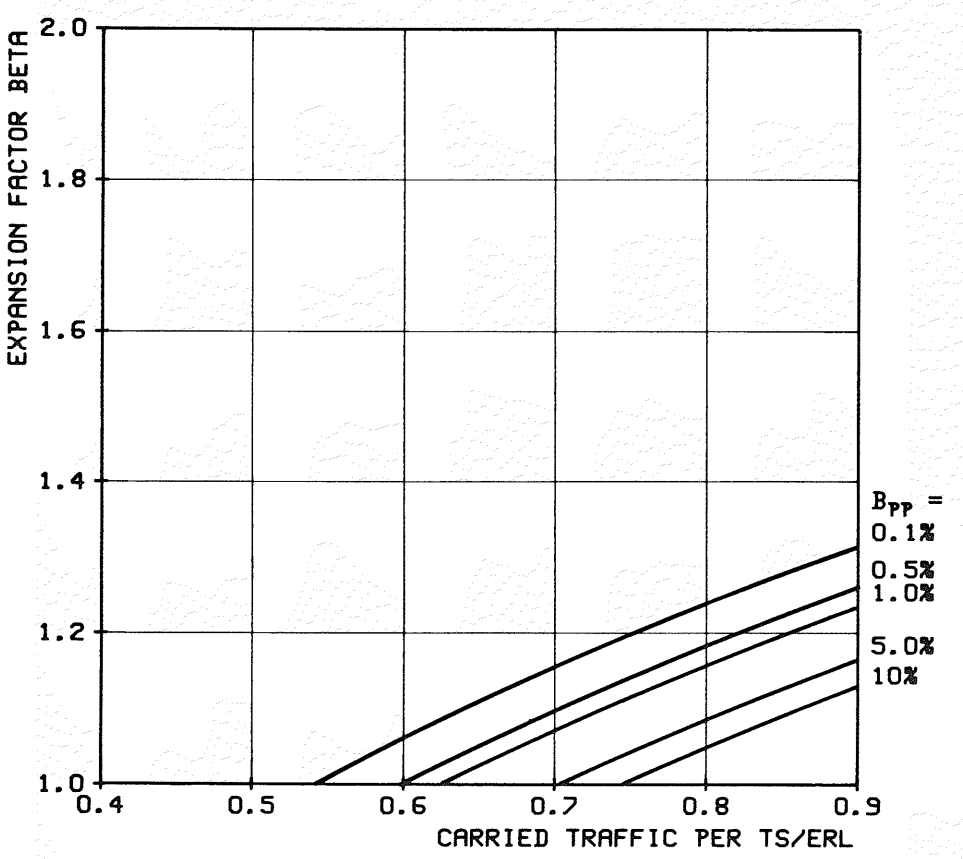


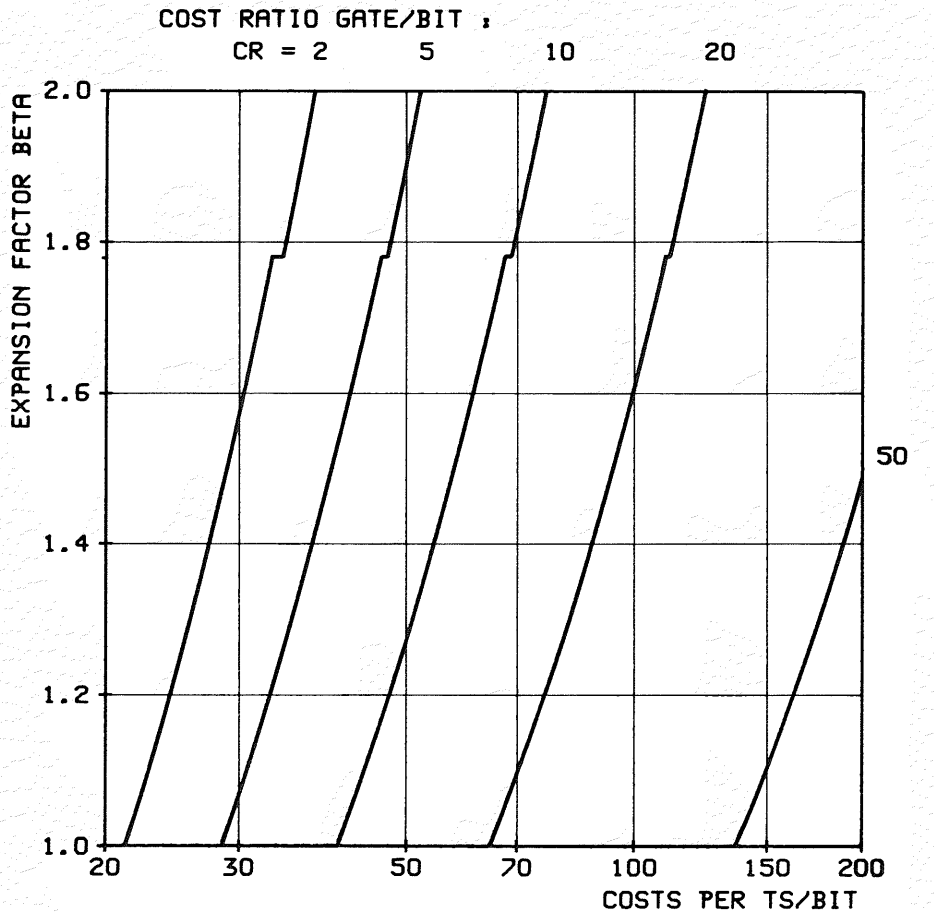


COMBINED SWITCHING	1 × 25 HW	H_1 = 25	—— { COMBINED SWITCHING
SEPARATED SWITCHING	2 × 25 HW	M = 30	{ SEPARATED SWITCHING

-CHART 11-

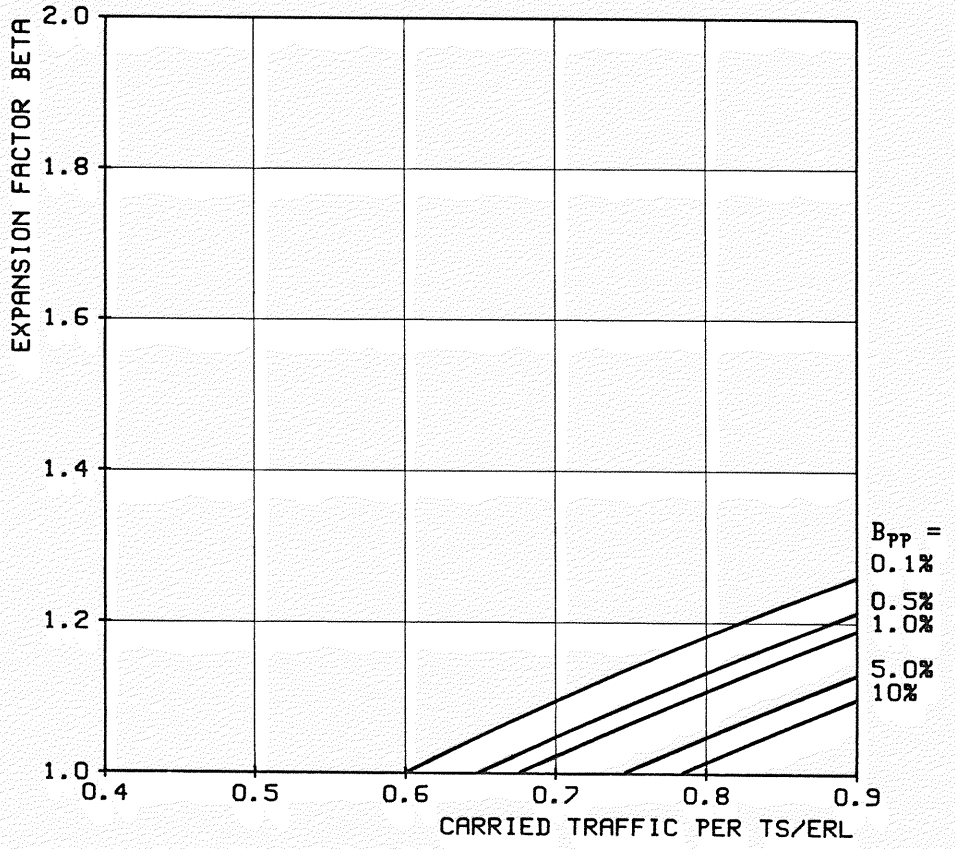
STS

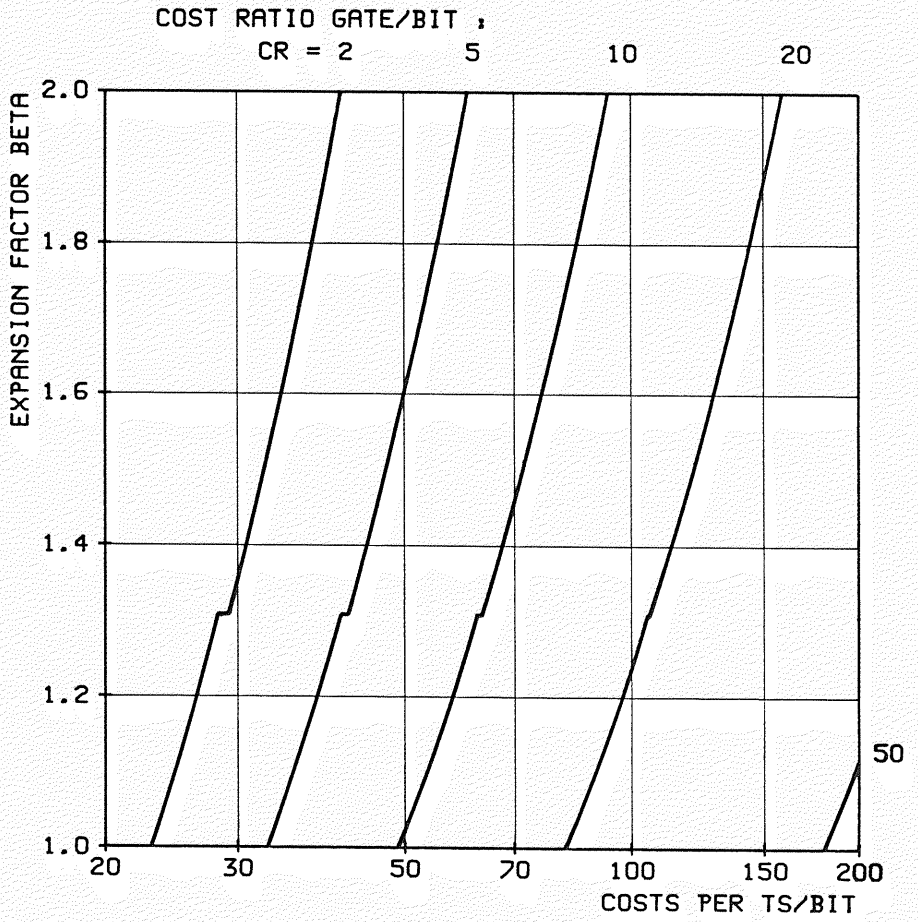




COMBINED SWITCHING	1 × 36 HW	H_1 = 36	——{ COMBINED SWITCHING
SEPARATED SWITCHING	2 × 36 HW	M = 30	{ SEPARATED SWITCHING

STS

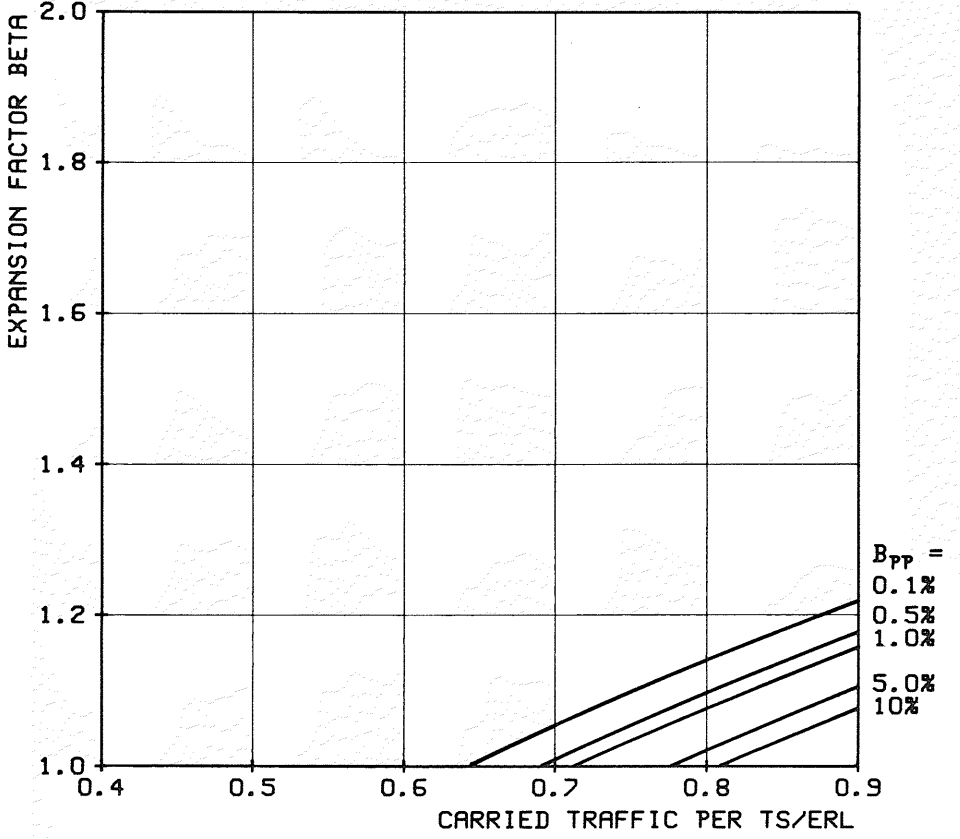


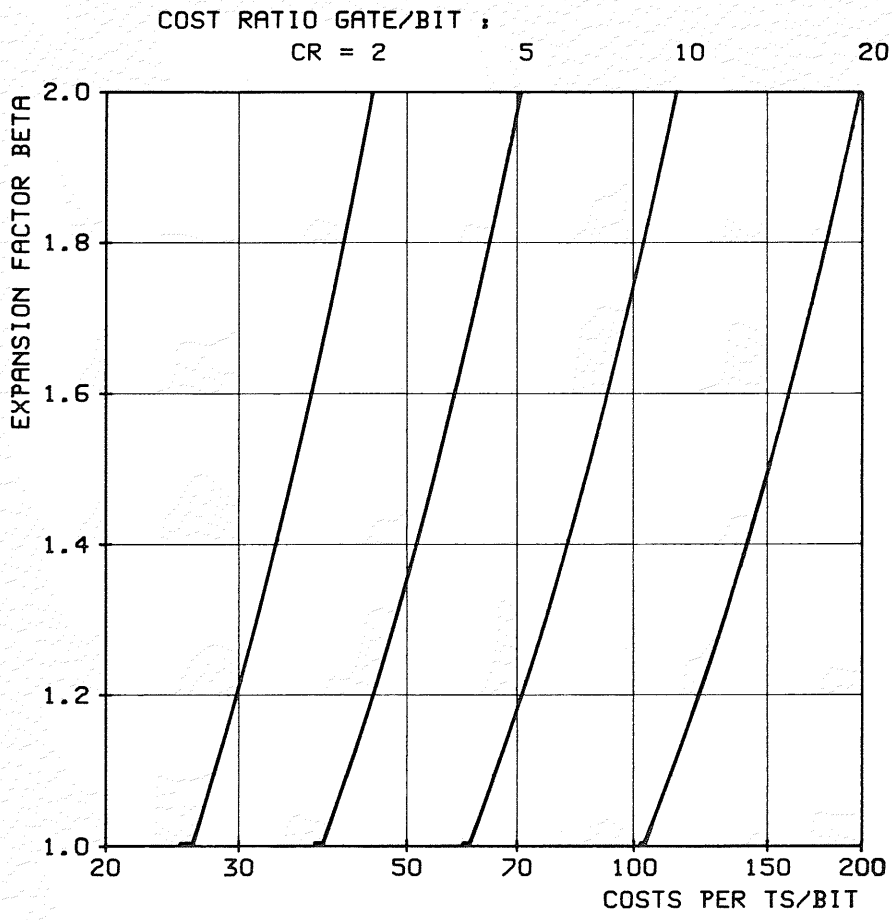


COMBINED SWITCHING	1 × 49 HW	H_1 = 49	COMBINED SWITCHING
SEPARATED SWITCHING	2 × 49 HW	M = 30	SEPARATED SWITCHING

-CHART 13-

STS





COMBINED SWITCHING 1 × 64 HW H_1 = 64

SEPARATED SWITCHING 2 × 64 HW M = 30

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

PCM SWITCHING ARRAY : TSST

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 16, 25, 36, 64, 100,
144, 196, 256, 324, 400,
625, 900, 1024, 2304, 4096,

SEPARATED SWITCHING : HW = 32, 50, 72, 128, 200,
288, 392, 512, 648, 800,
1250, 1800, 2048, 4608, 8192,

TIME-SLOTS (TS) PER HW : M = 30 TS

POINT-TO-POINT LOSS, PCT1 : B_{PP} = 0.1, 0.5, 1.0, 5.0, 10.0%

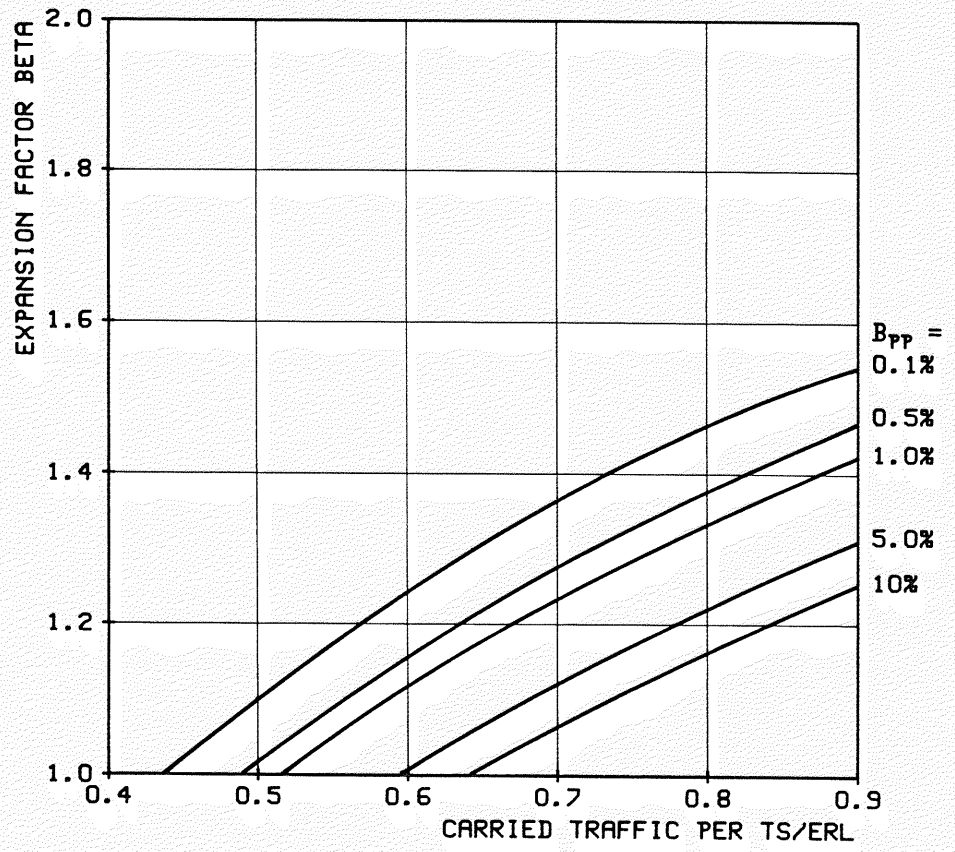
COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

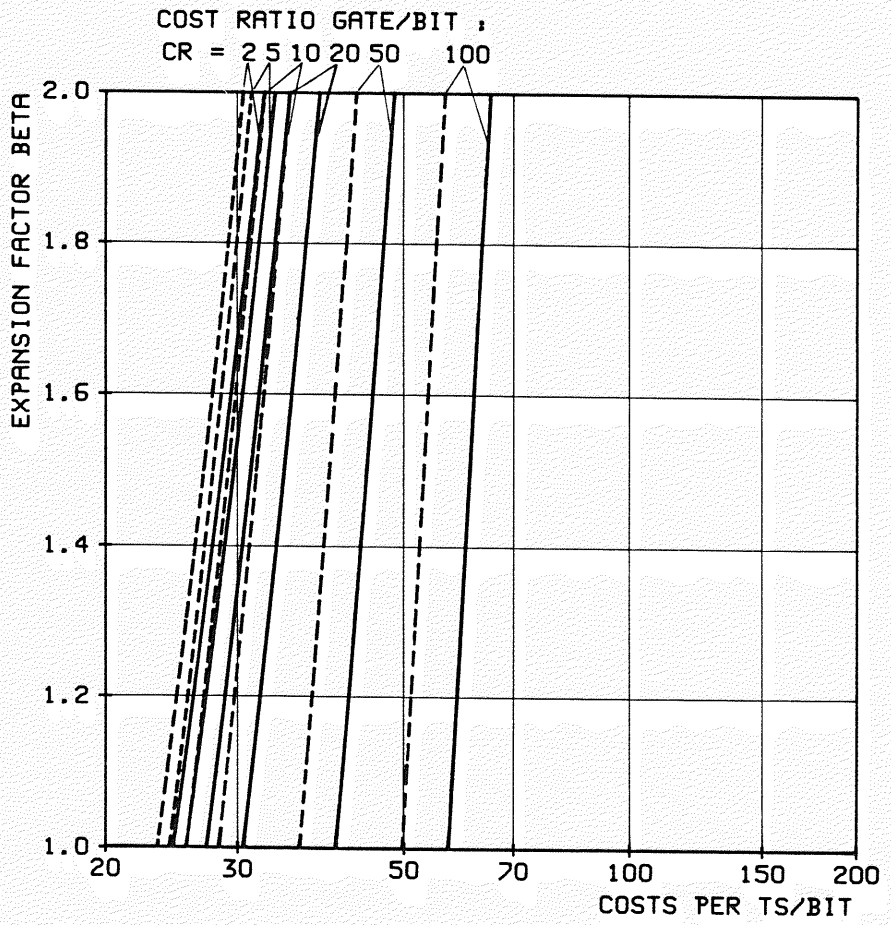
BLOCK SIZE

COMBINED SWITCHING : $H_2 = \sqrt{HW}$

SEPARATED SWITCHING : $H_2 = \sqrt{HW/2}$

TSST



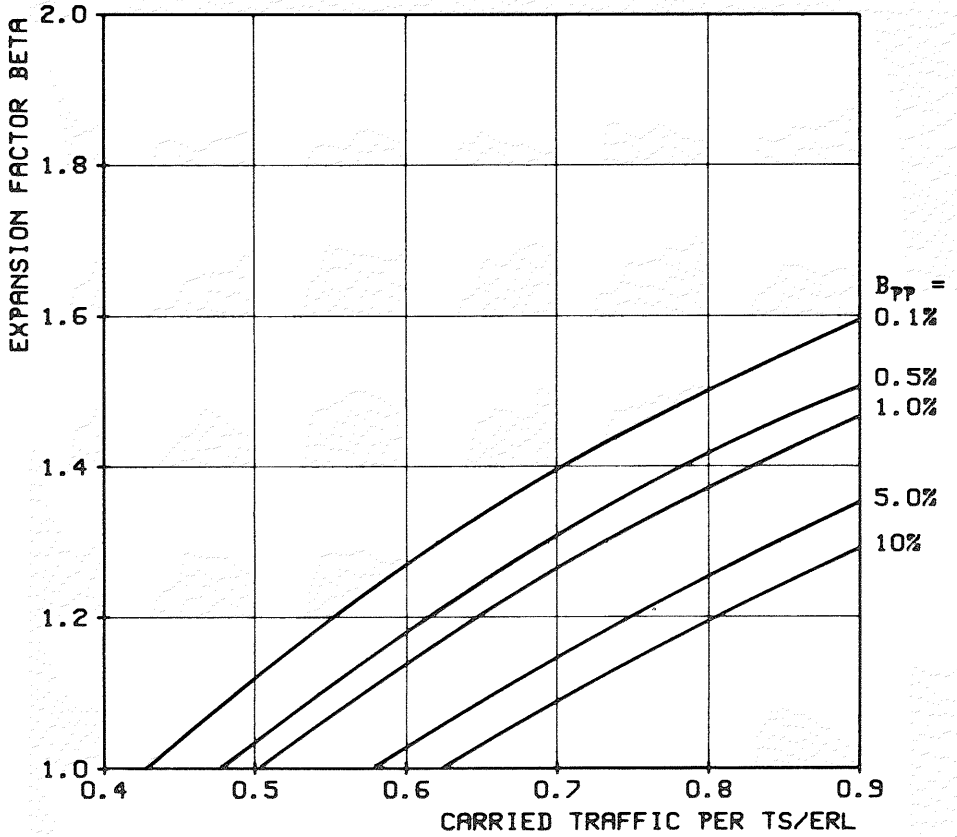


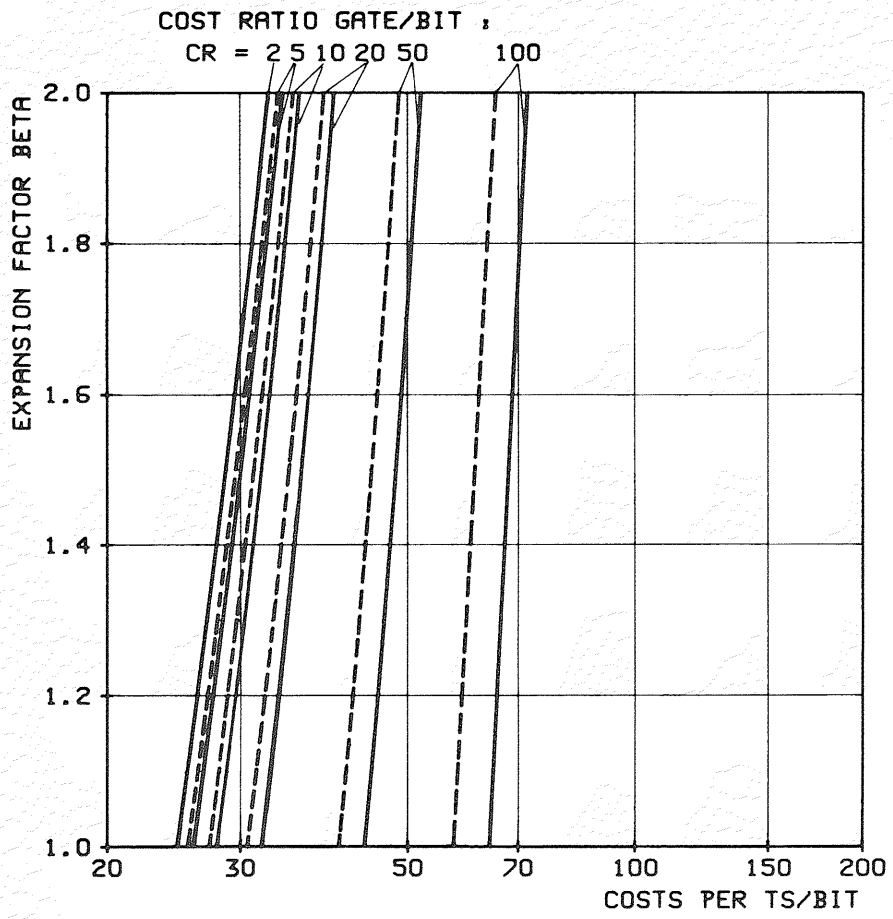
COMBINED SWITCHING 1 × 16 HW H_2 = 4
SEPARATED SWITCHING 2 × 16 HW M = 30

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

-CHART 15-

TSST





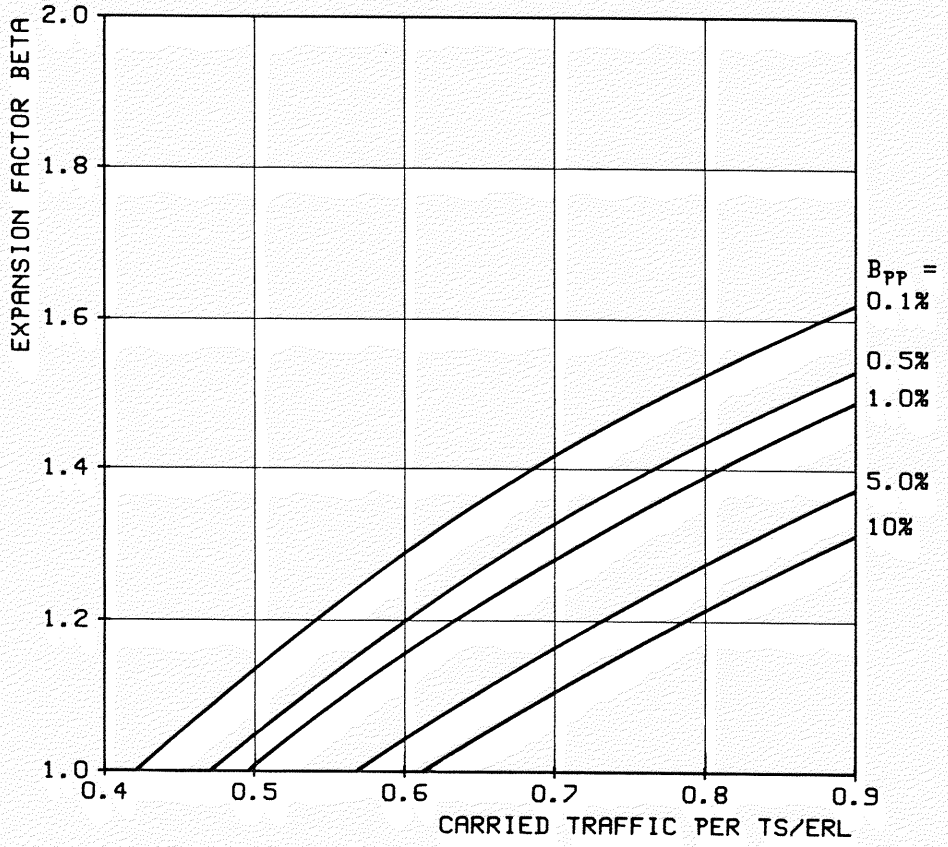
COMBINED SWITCHING 1 × 25 HW H_2 = 5

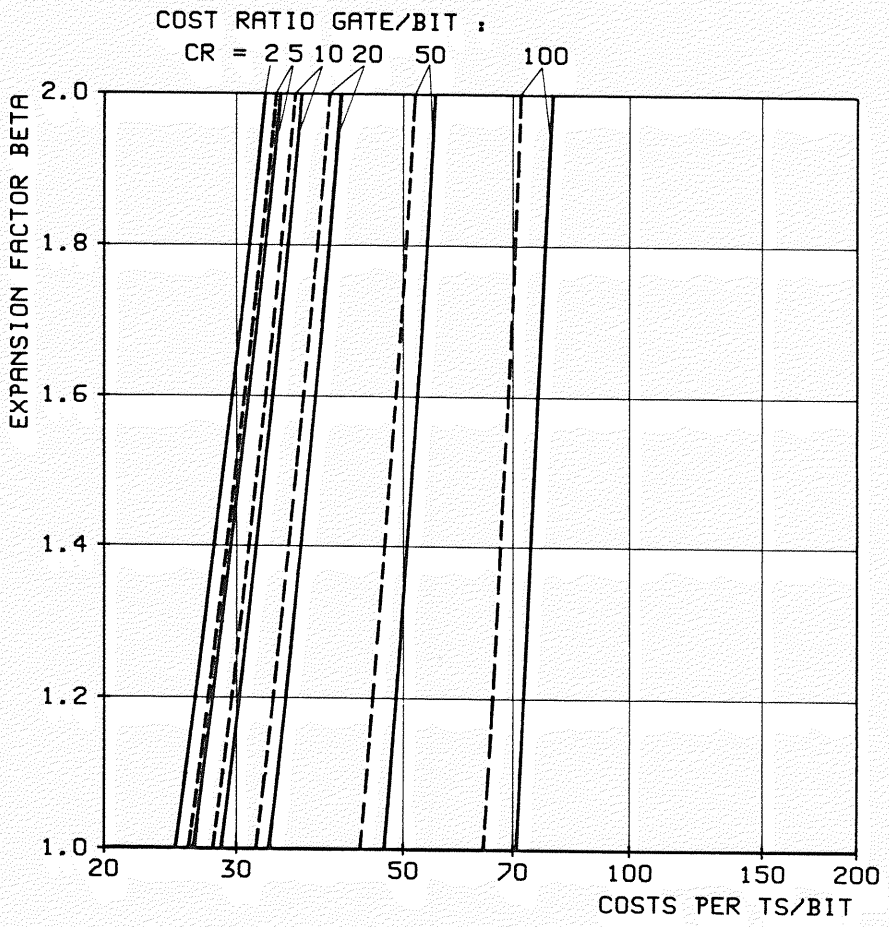
SEPARATED SWITCHING 2 × 25 HW M = 30

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

TSST



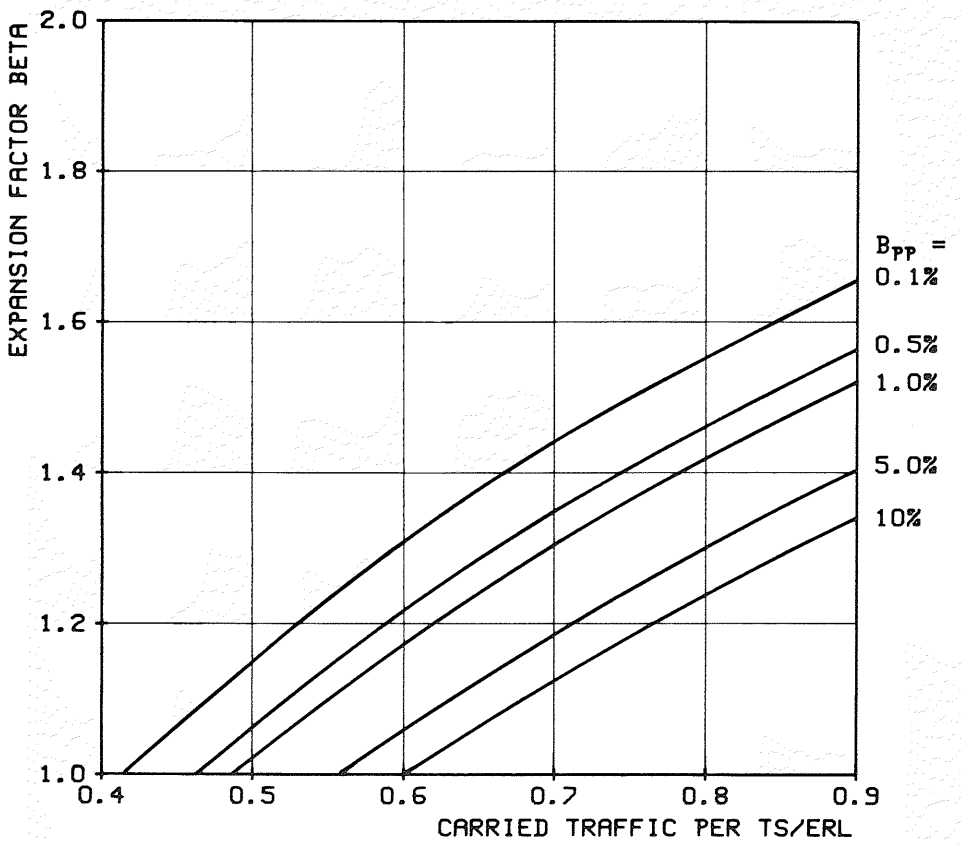


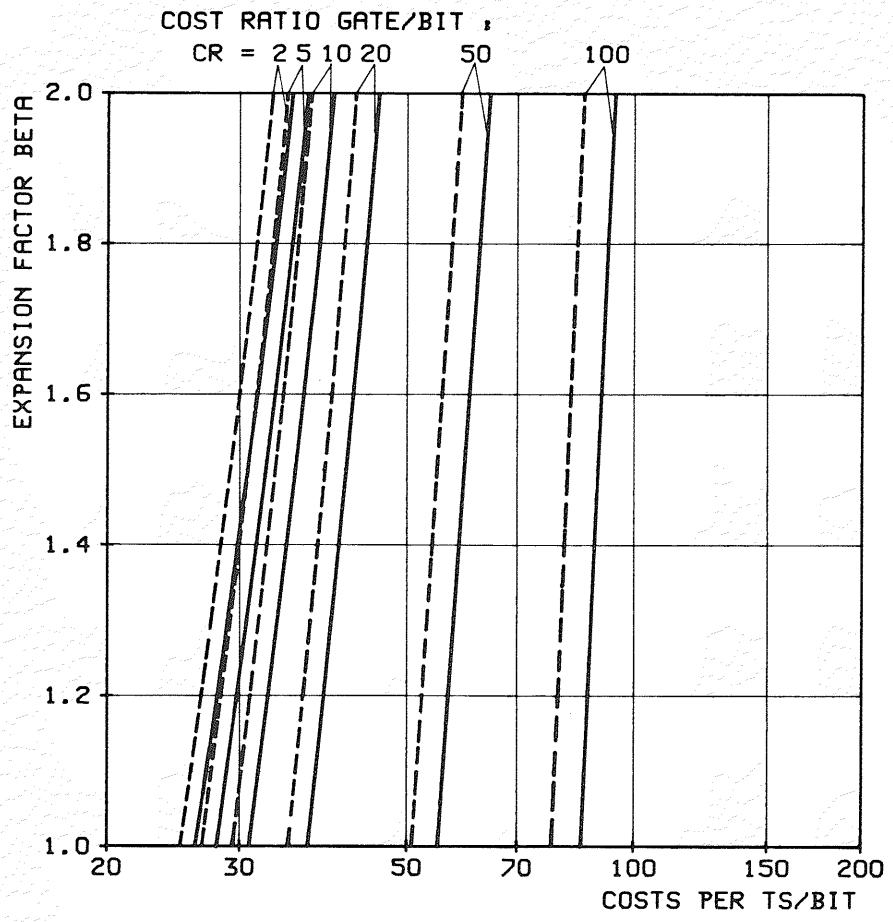
COMBINED SWITCHING 1 × 36 HW H_2 = 6
SEPARATED SWITCHING 2 × 36 HW M = 30

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

-CHART 17-

TSST

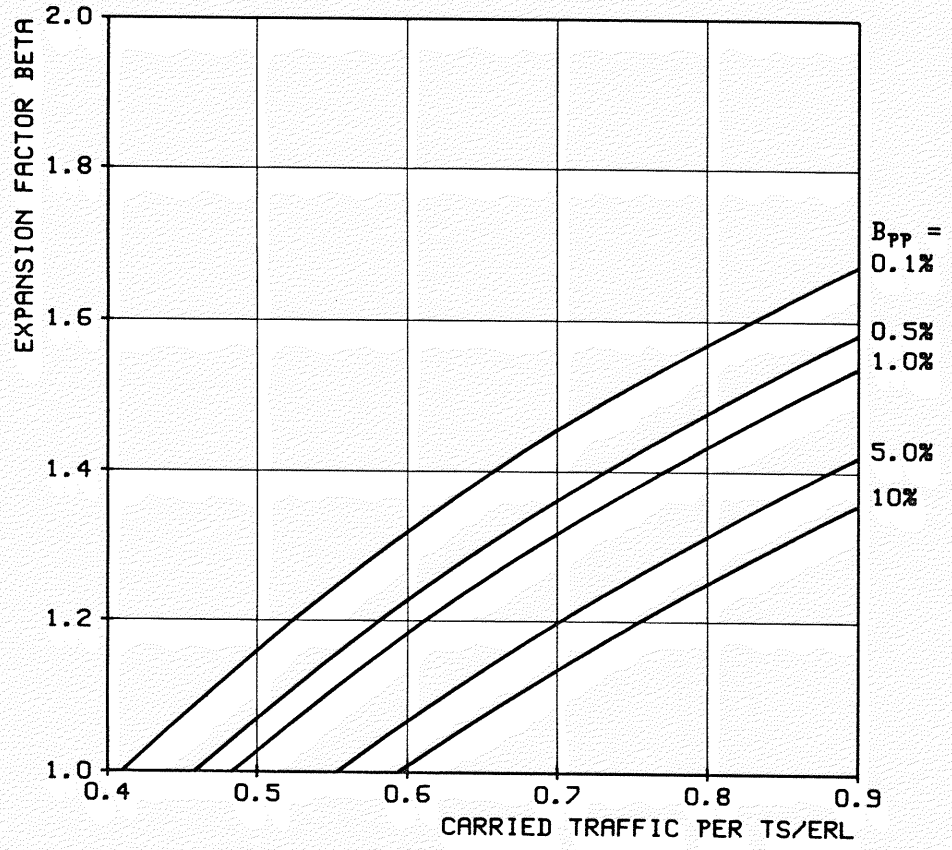


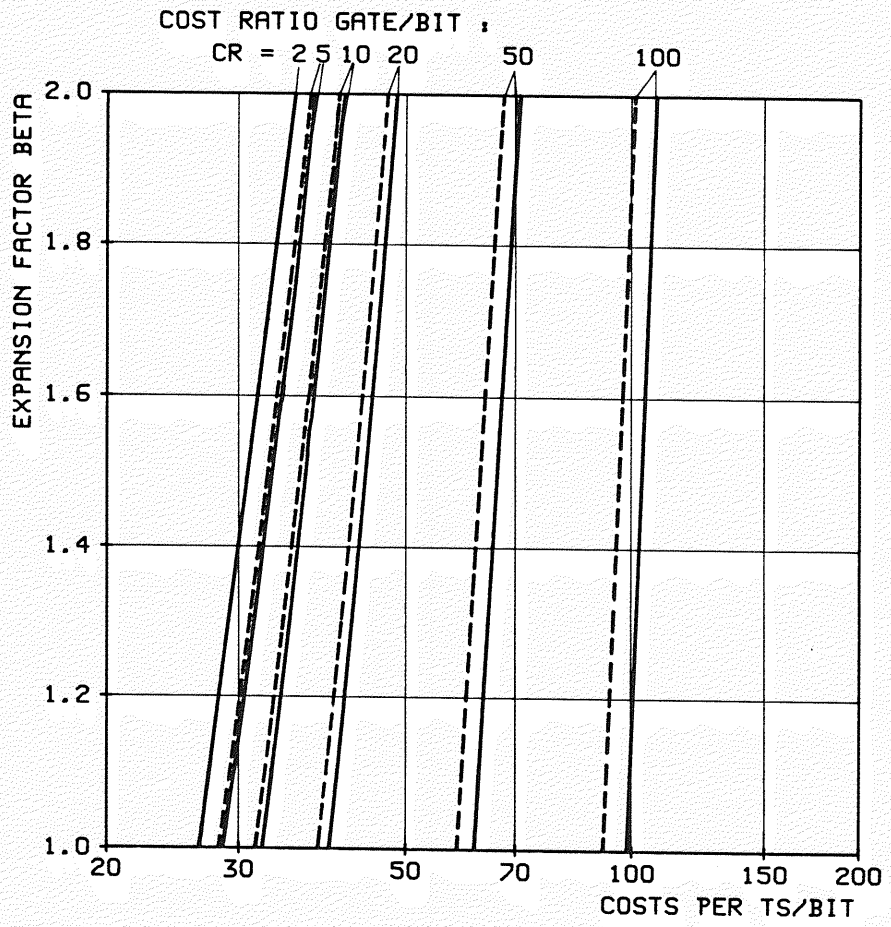


COMBINED SWITCHING 1 × 64 HW H_2 = 8 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 64 HW M = 30 --- SEPARATED SWITCHING

TSST



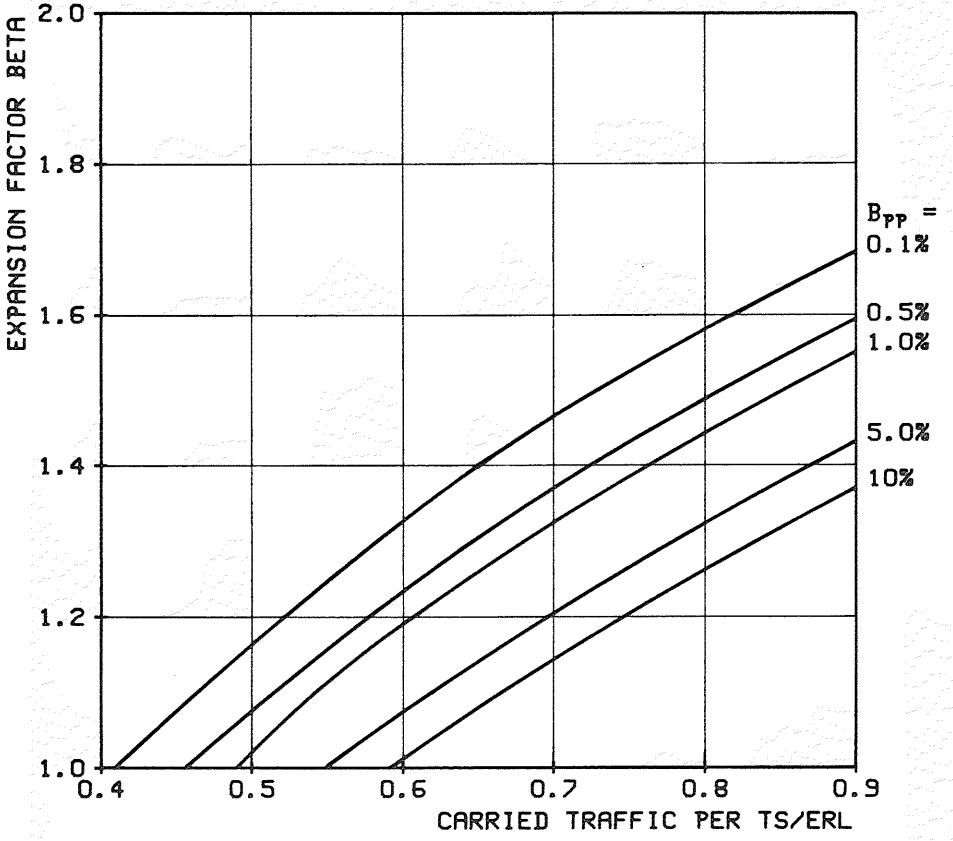


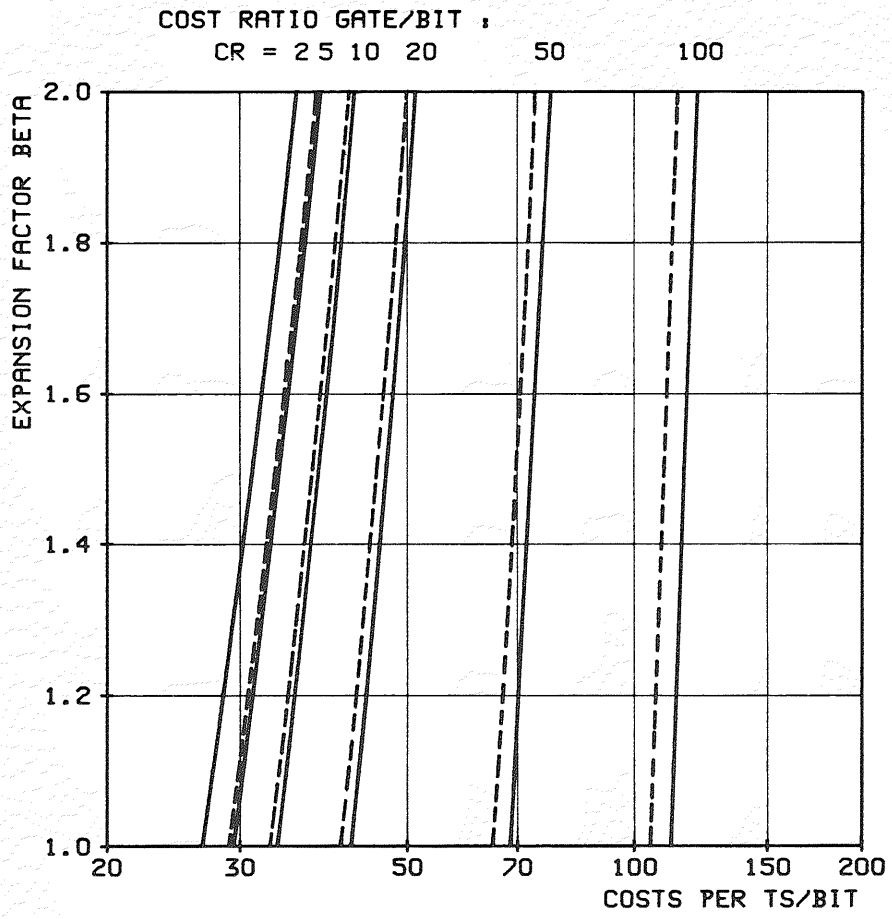
COMBINED SWITCHING 1 × 100 HW H_2 = 10
SEPARATED SWITCHING 2 × 100 HW M = 30

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

-CHART 19-

TSST

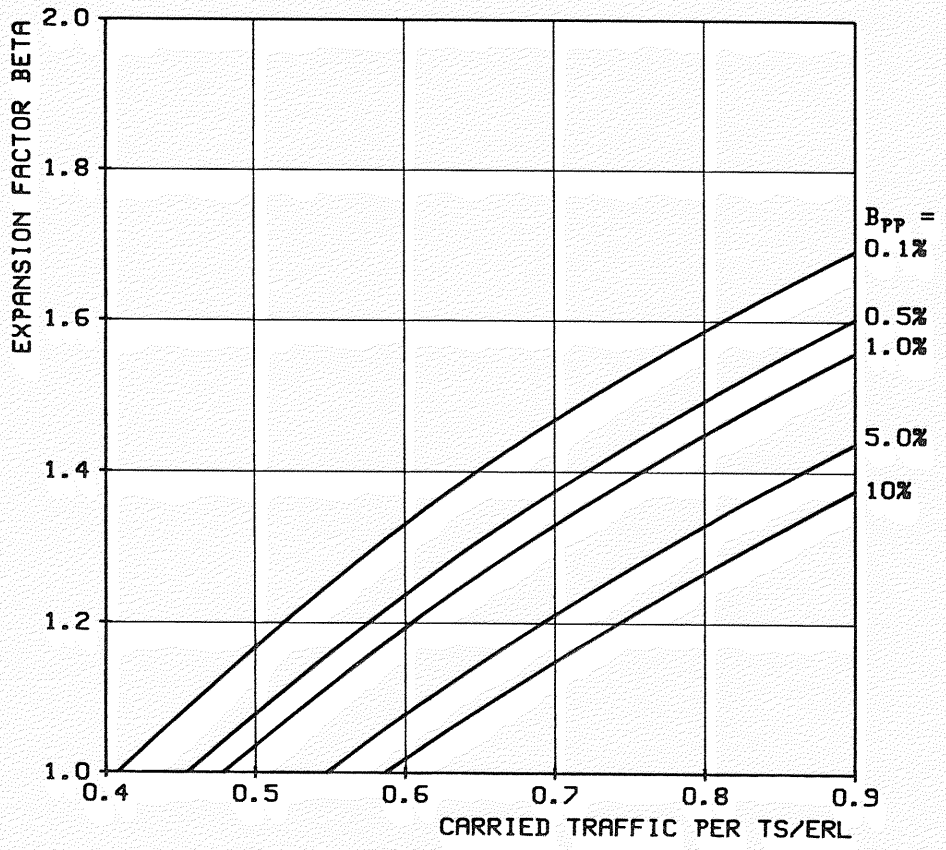


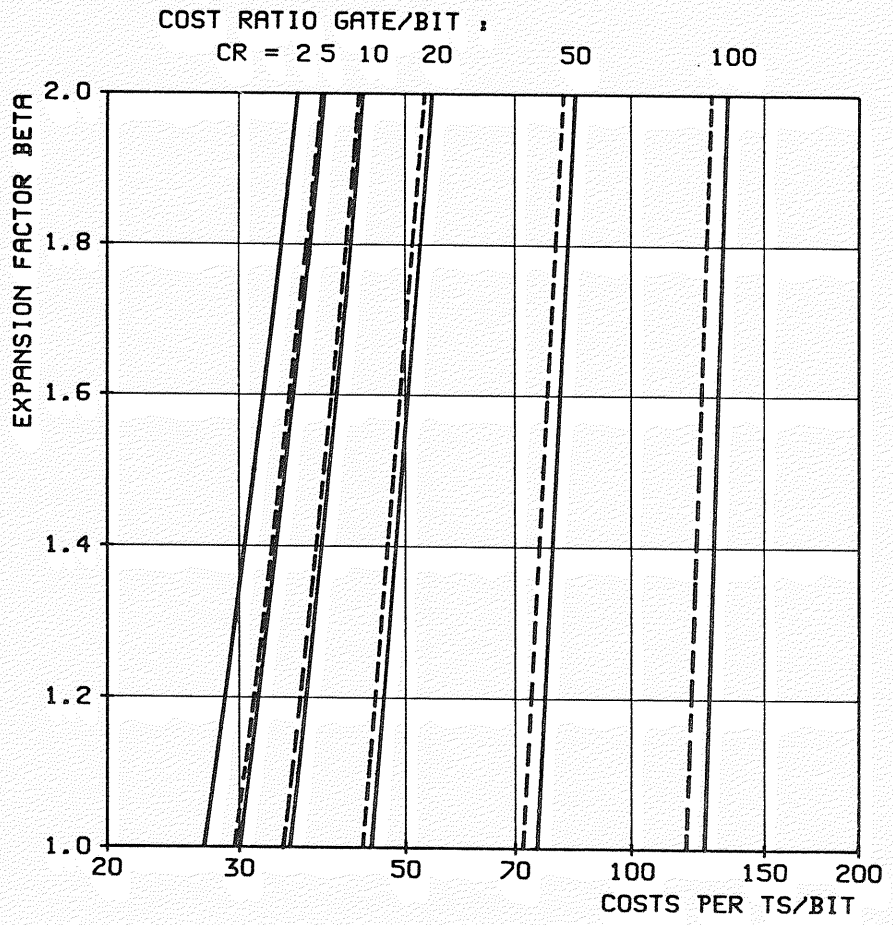


COMBINED SWITCHING 1 × 144 HW H_2 = 12
SEPARATED SWITCHING 2 × 144 HW M = 30

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

TSST



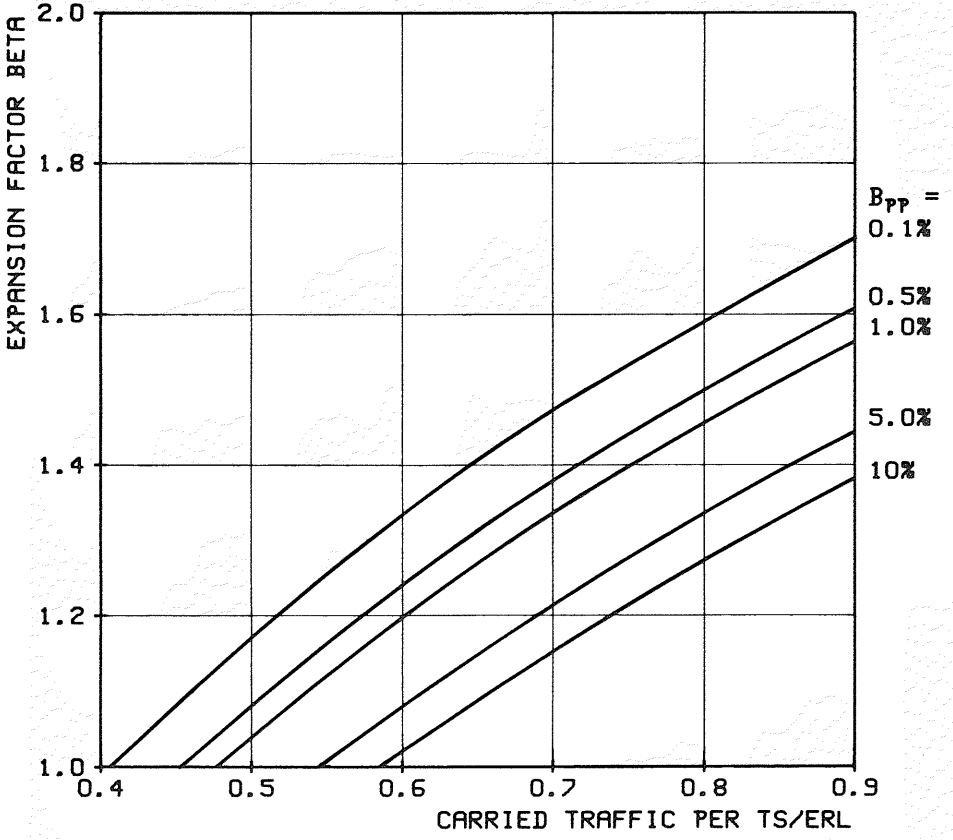


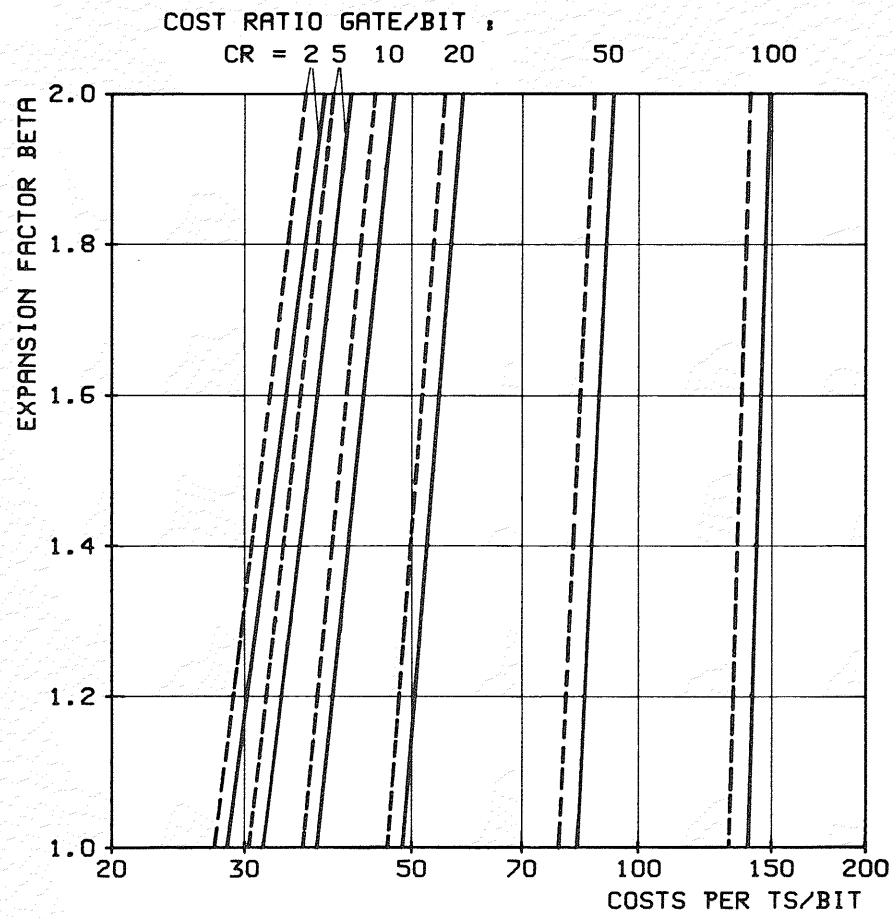
COMBINED SWITCHING 1 × 196 HW H_2 = 14
SEPARATED SWITCHING 2 × 196 HW M = 30

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

-CHART 21-

TSST

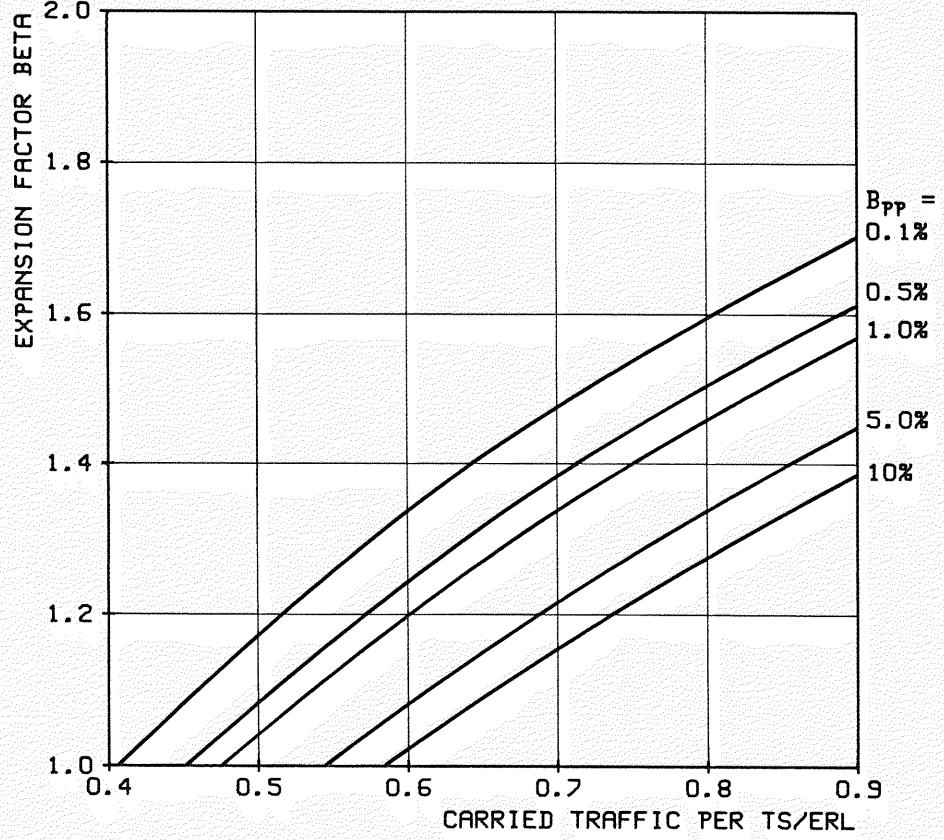


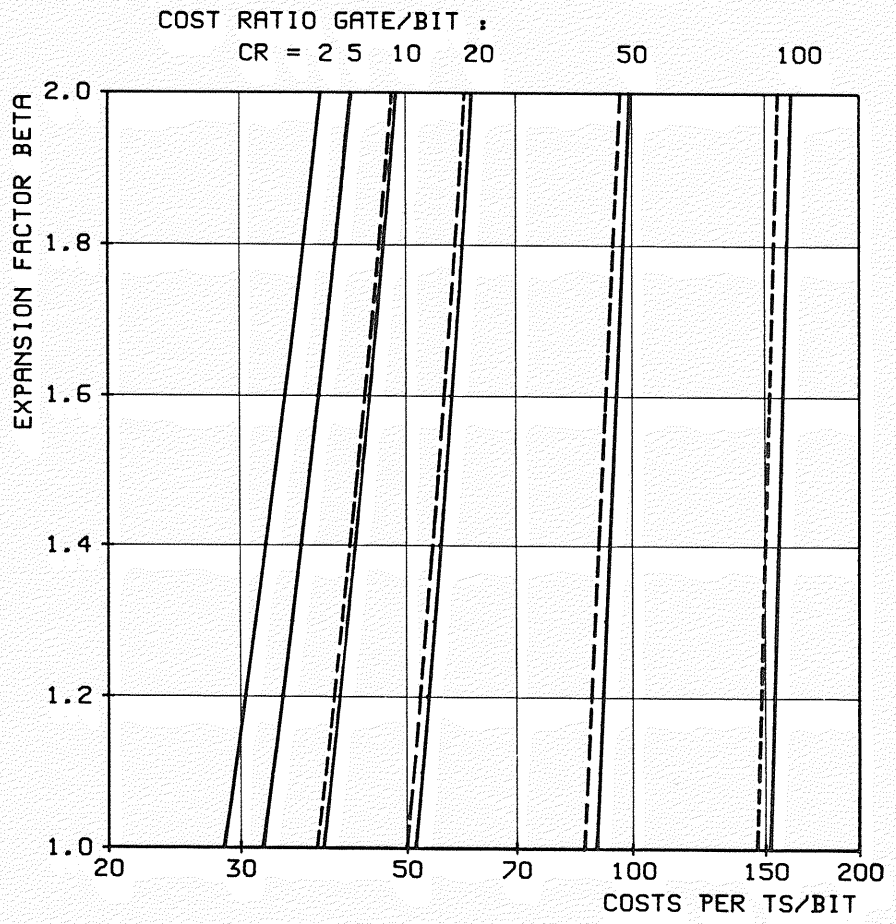


COMBINED SWITCHING 1 × 256 HW H_2 = 16 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 256 HW M = 30 --- SEPARATED SWITCHING

TSST



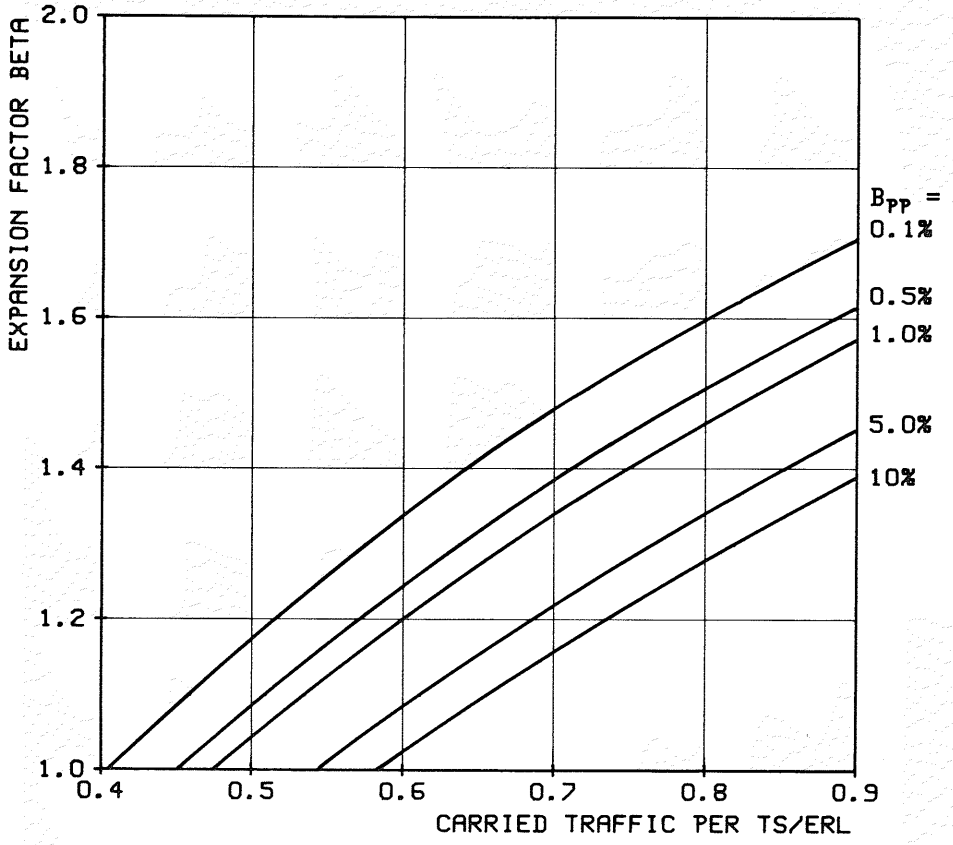


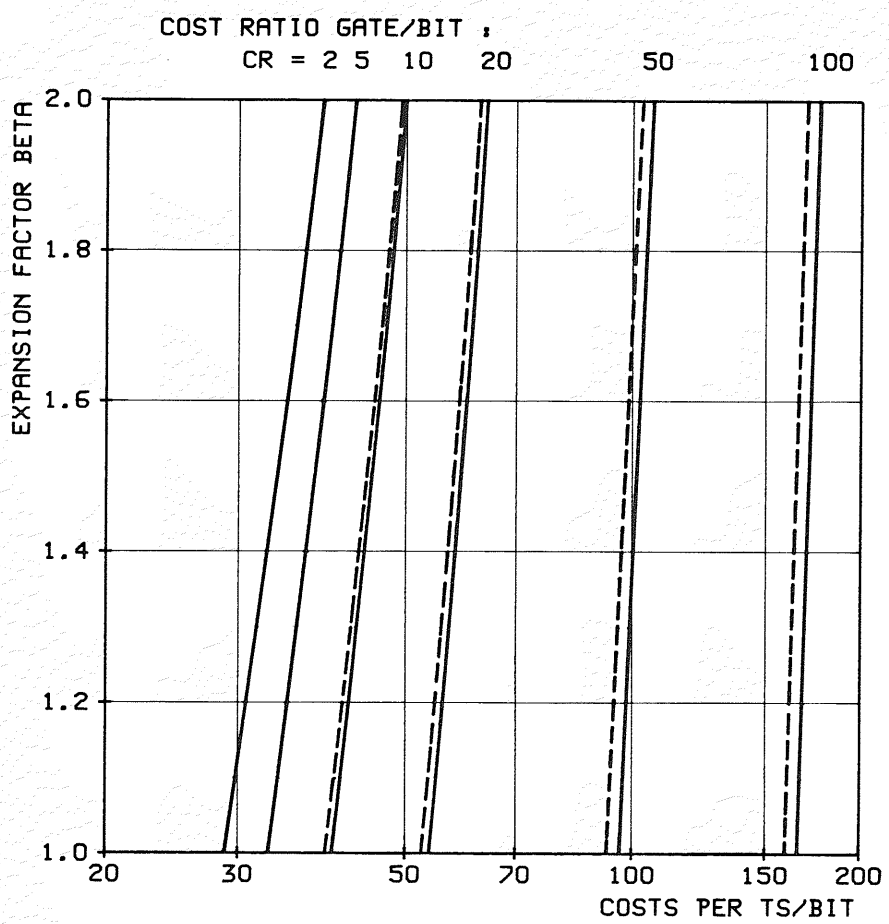
COMBINED SWITCHING 1 × 324 HW H_2 = 18 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 324 HW M = 30 --- SEPARATED SWITCHING

-CHART 23-

TSST





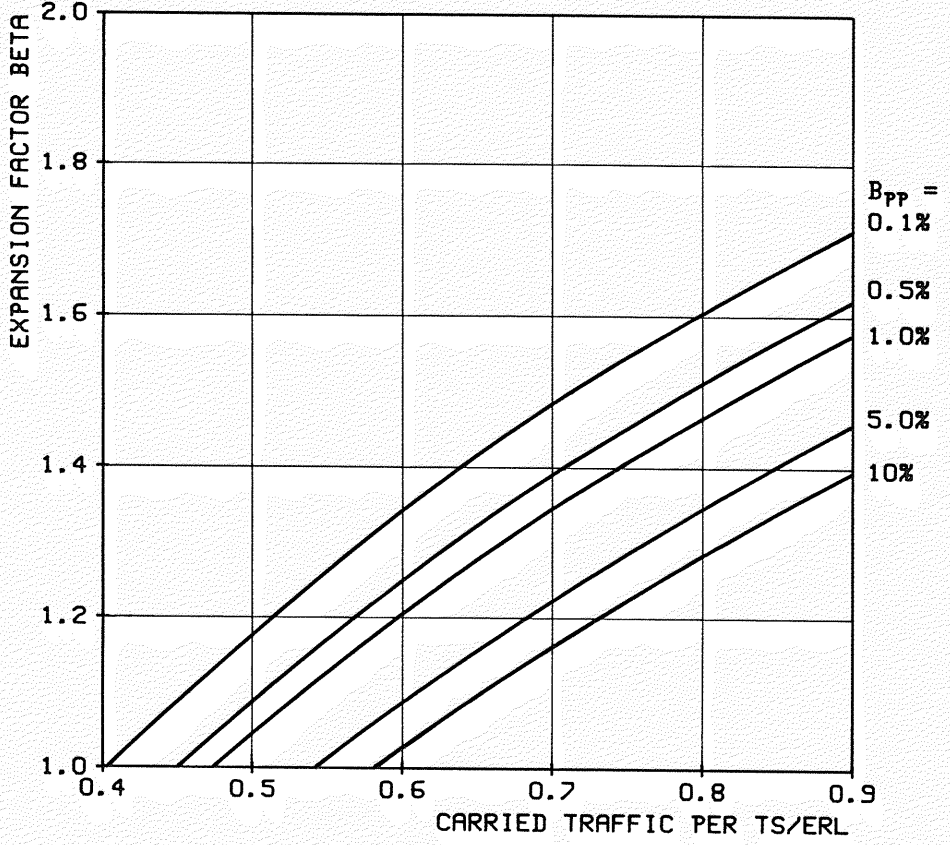
COMBINED SWITCHING 1 × 400 HW H_2 = 20

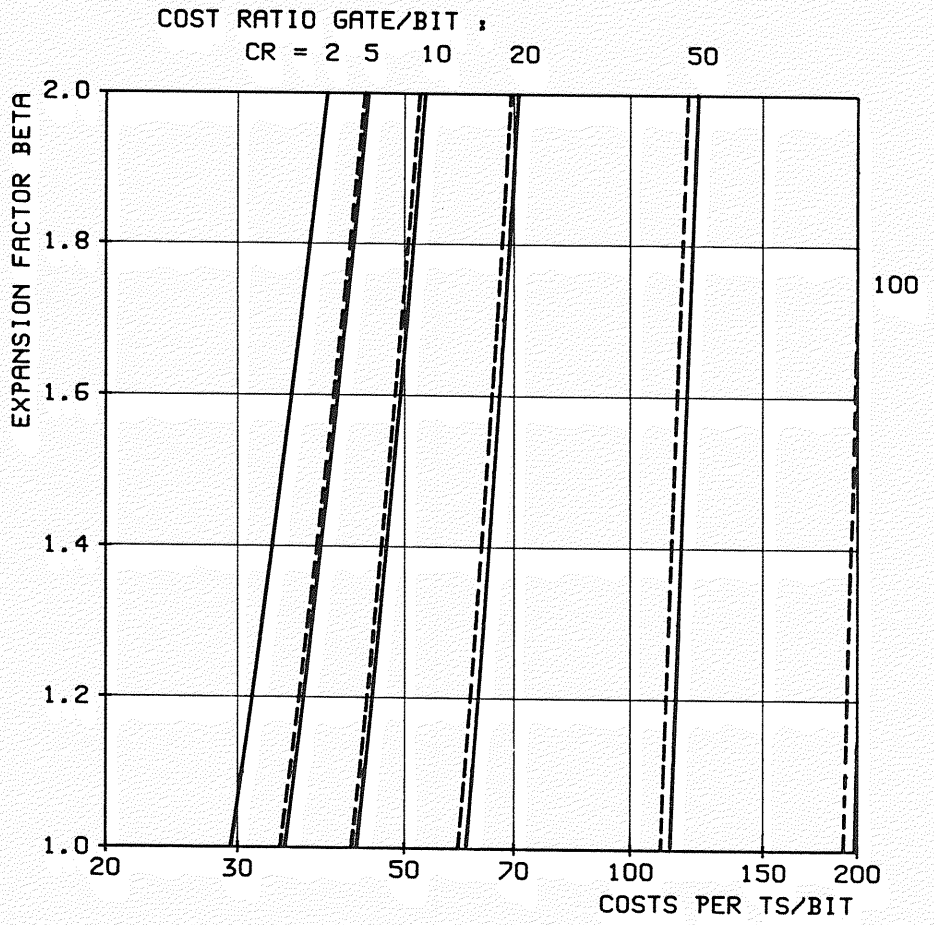
SEPARATED SWITCHING 2 × 400 HW M = 30

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

TSST



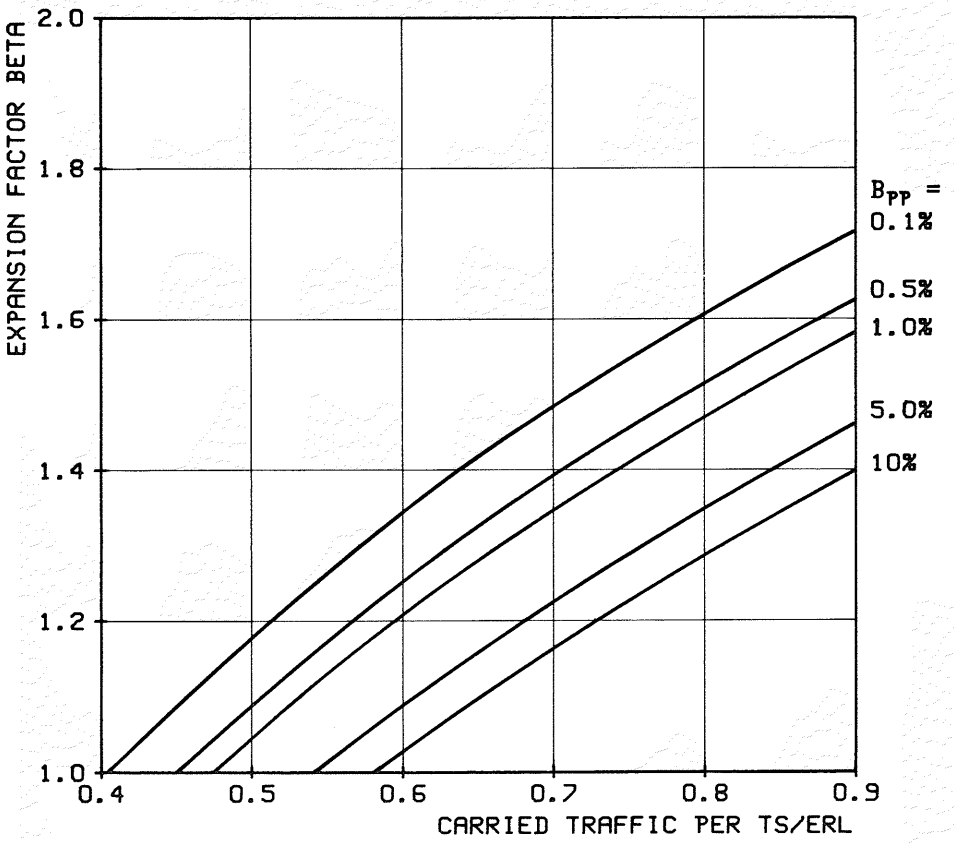


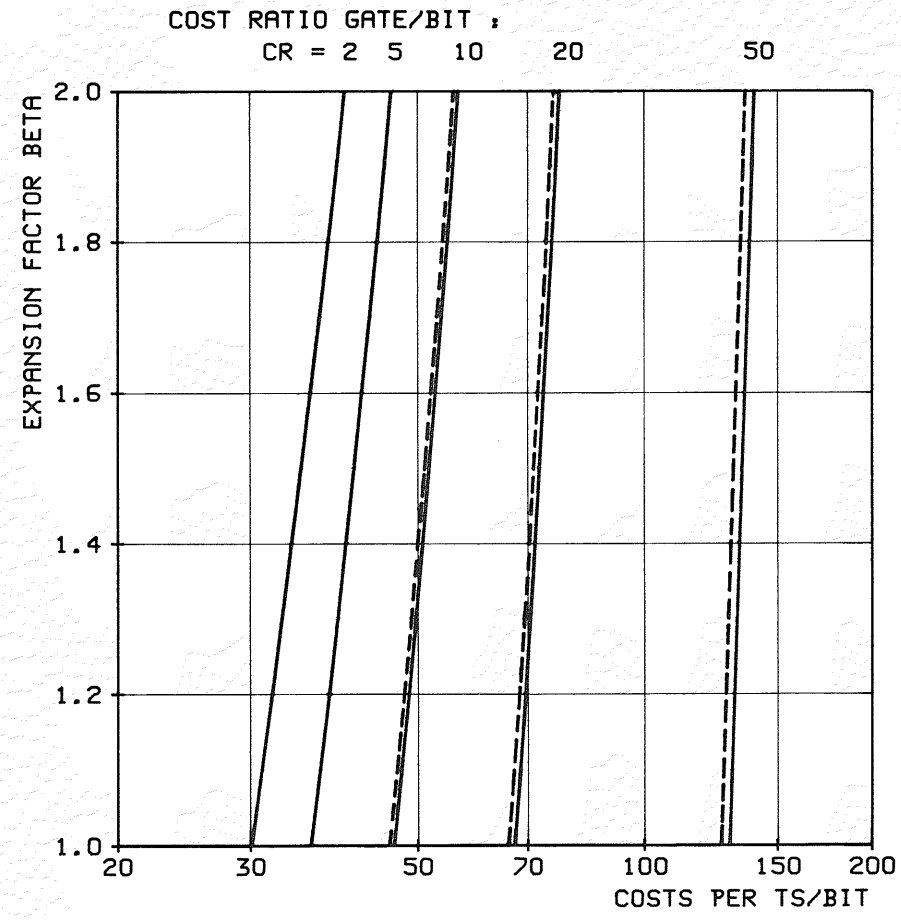
COMBINED SWITCHING 1 × 625 HW H_2 = 25
SEPARATED SWITCHING 2 × 625 HW M = 30

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

-CHART 25-

TSST

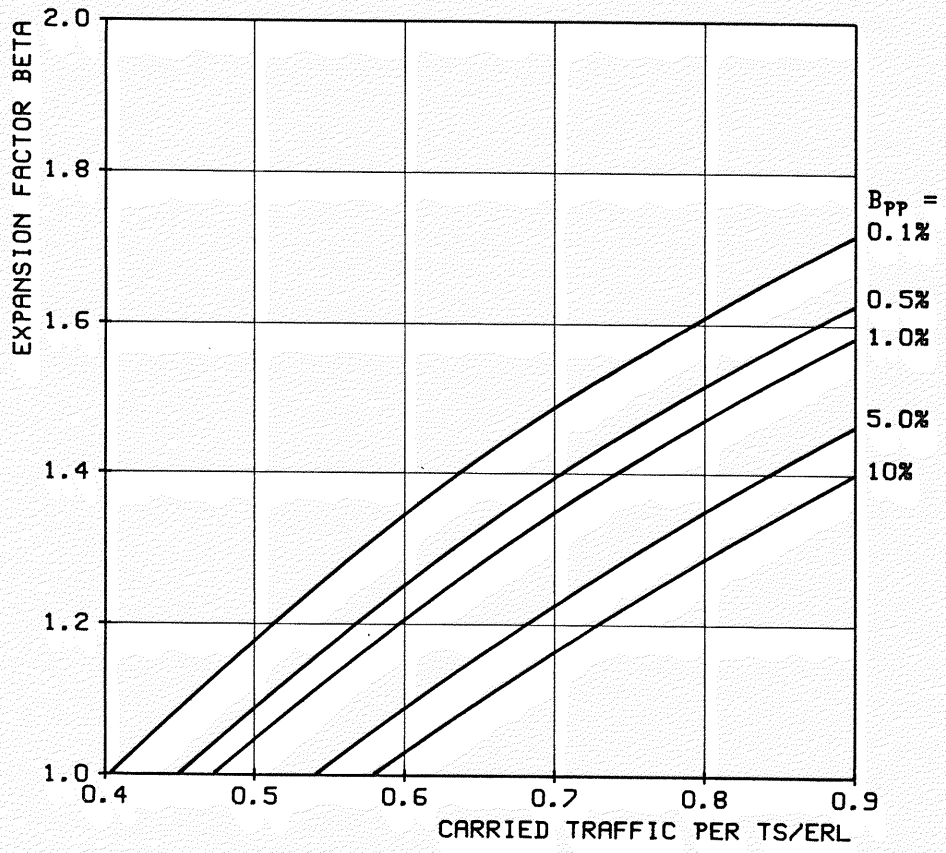


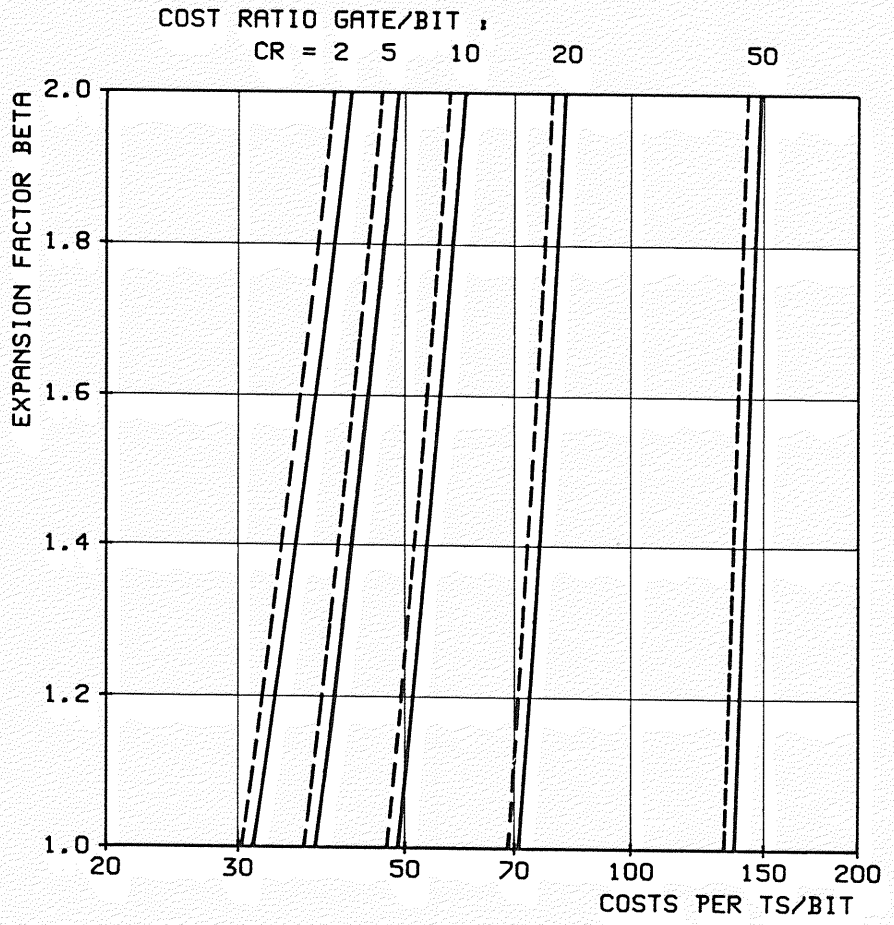


COMBINED SWITCHING 1 × 900 HW H_2 = 30 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 900 HW M = 30 --- SEPARATED SWITCHING

TSST



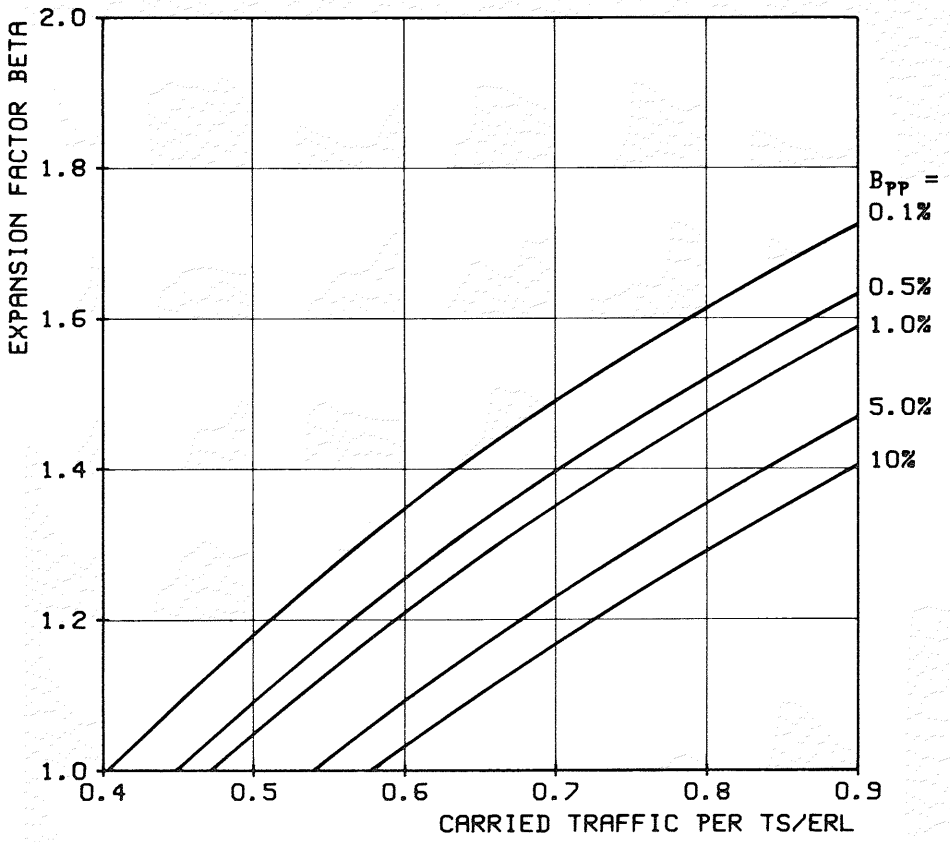


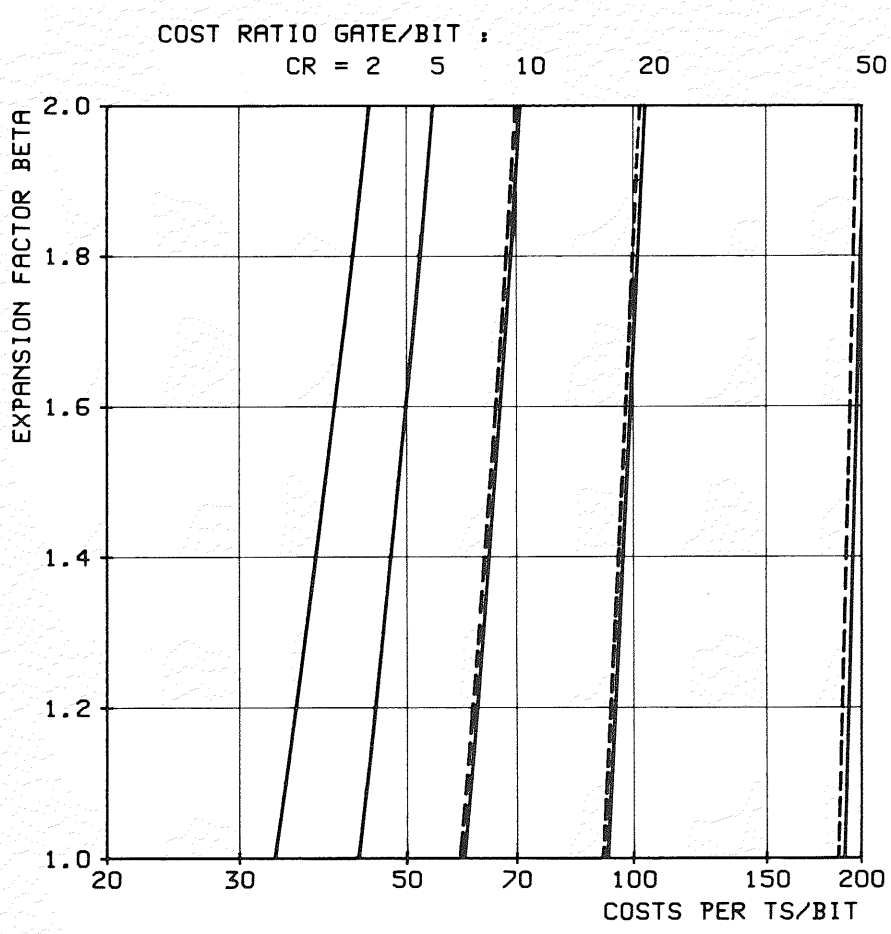
COMBINED SWITCHING 1 × 1024 HW H_2 = 32 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 1024 HW M = 30 --- SEPARATED SWITCHING

-CHART 27-

TSST

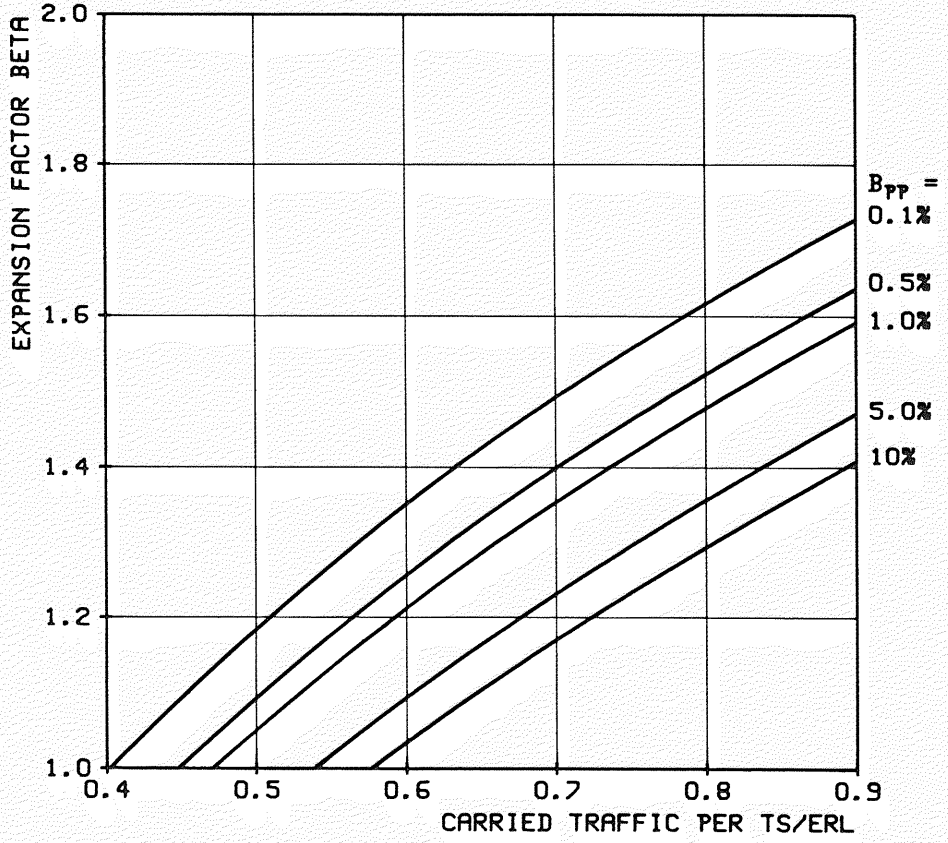


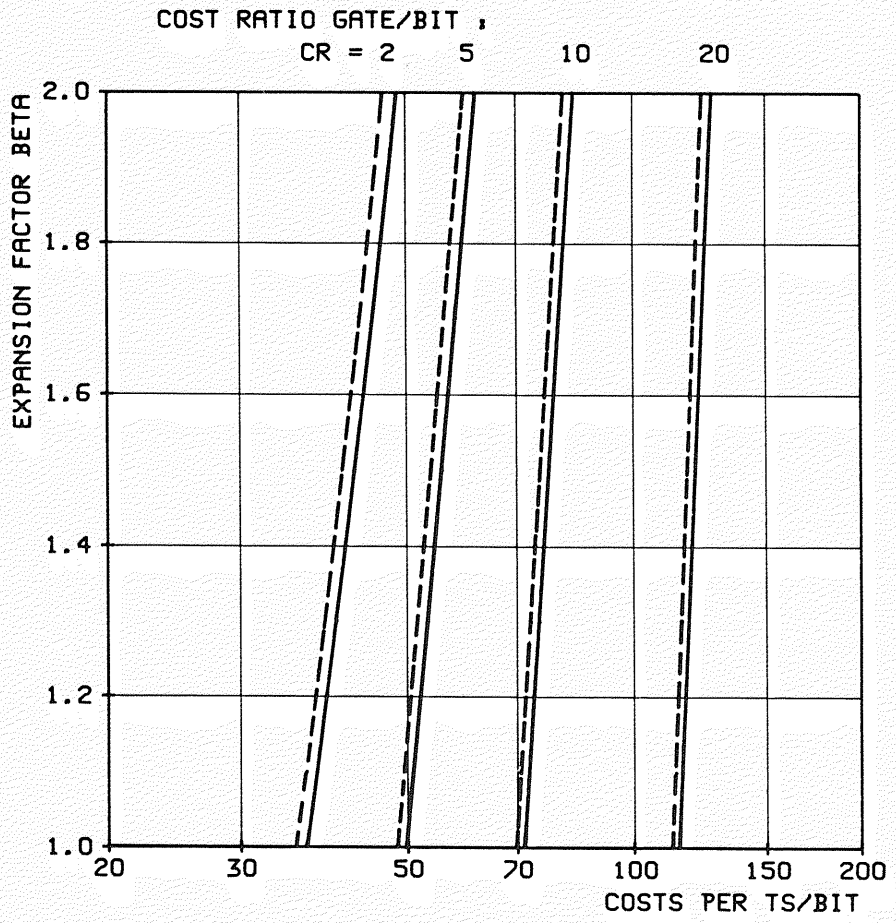


COMBINED SWITCHING 1 × 2304 HW H_2 = 48 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 2304 HW M = 30 --- SEPARATED SWITCHING

TSST





COMBINED SWITCHING 1 × 4096 HW H_2 = 64 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 4096 HW M = 30 --- SEPARATED SWITCHING

PCM SWITCHING ARRAY : TSSST

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 16, 25, 36, 64, 100,
144, 196, 256, 324, 400,
625, 900, 1024, 2304, 4096,

SEPARATED SWITCHING : HW = 32, 50, 72, 128, 200,
288, 392, 512, 648, 800,
1250, 1800, 2048, 4608, 8192,

TIME-SLOTS (TS) PER HW : M = 30 TS

POINT-TO-POINT LOSS, PCT1 : B_{PP} = 0.1, 0.5, 1.0, 5.0, 10.0%

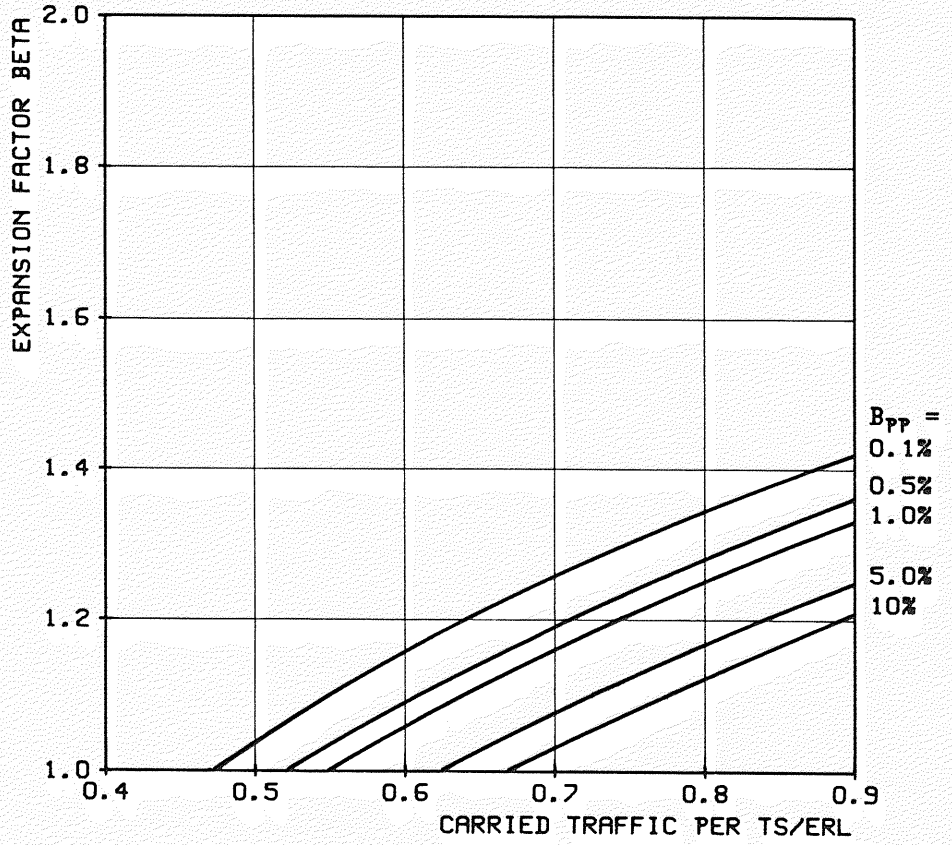
COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

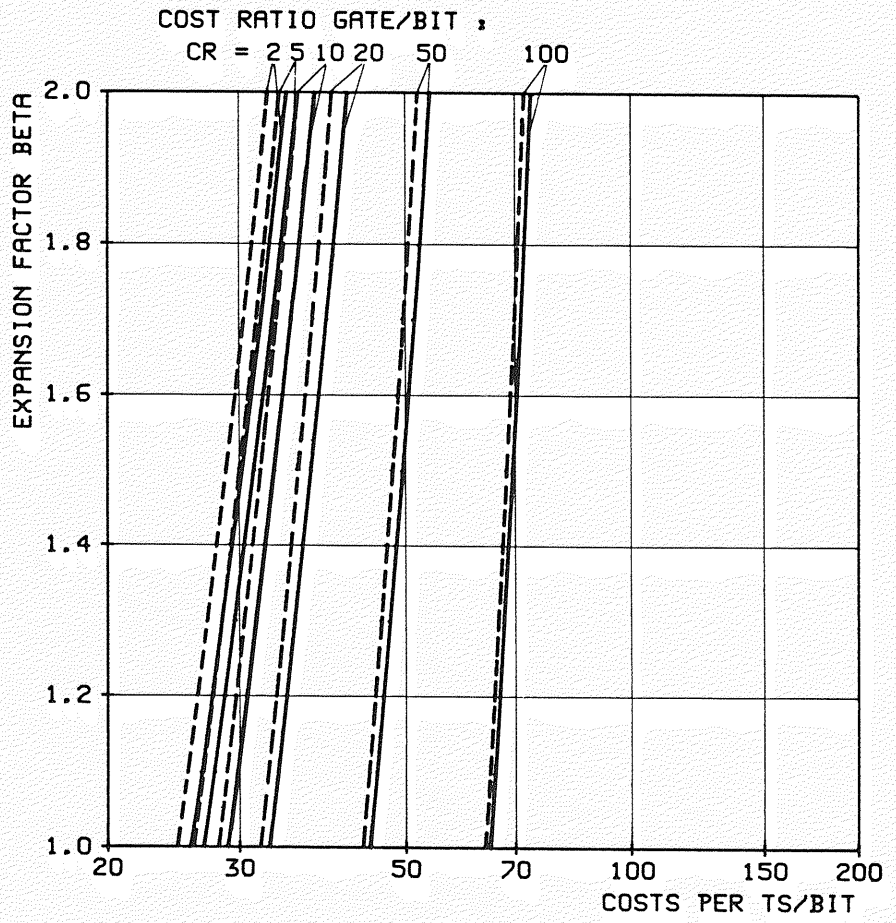
BLOCK SIZE

COMBINED SWITCHING : $H_2 = \sqrt{HW}$

SEPARATED SWITCHING : $H_2 = \sqrt{HW/2}$

TSSST



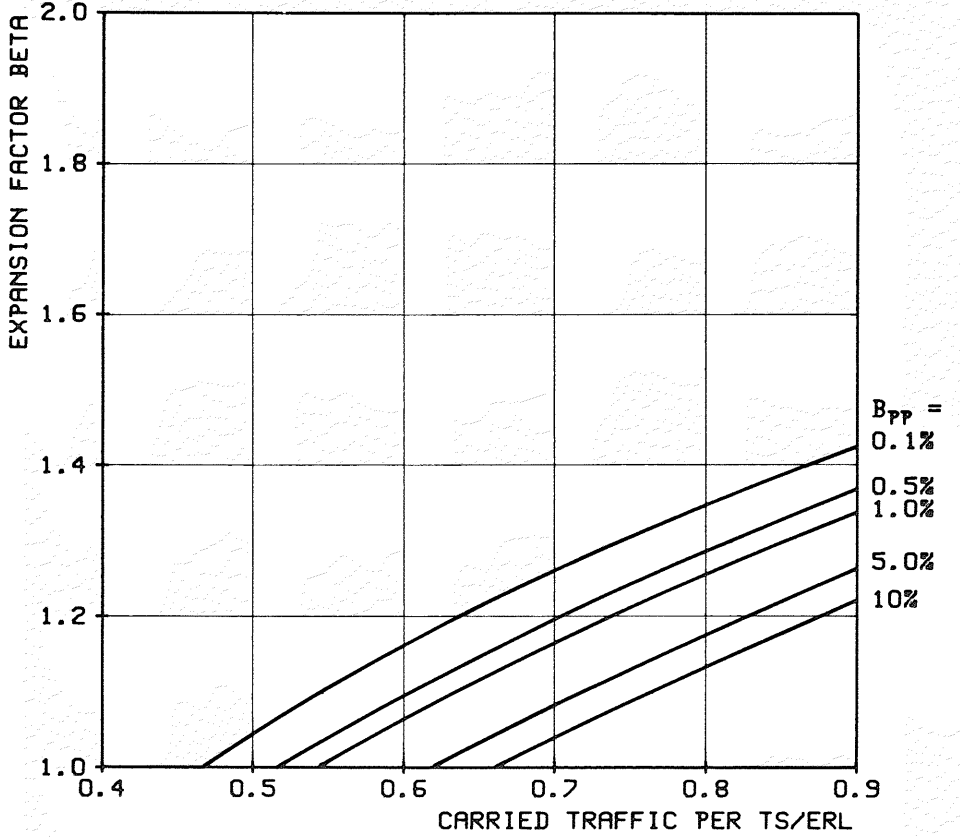


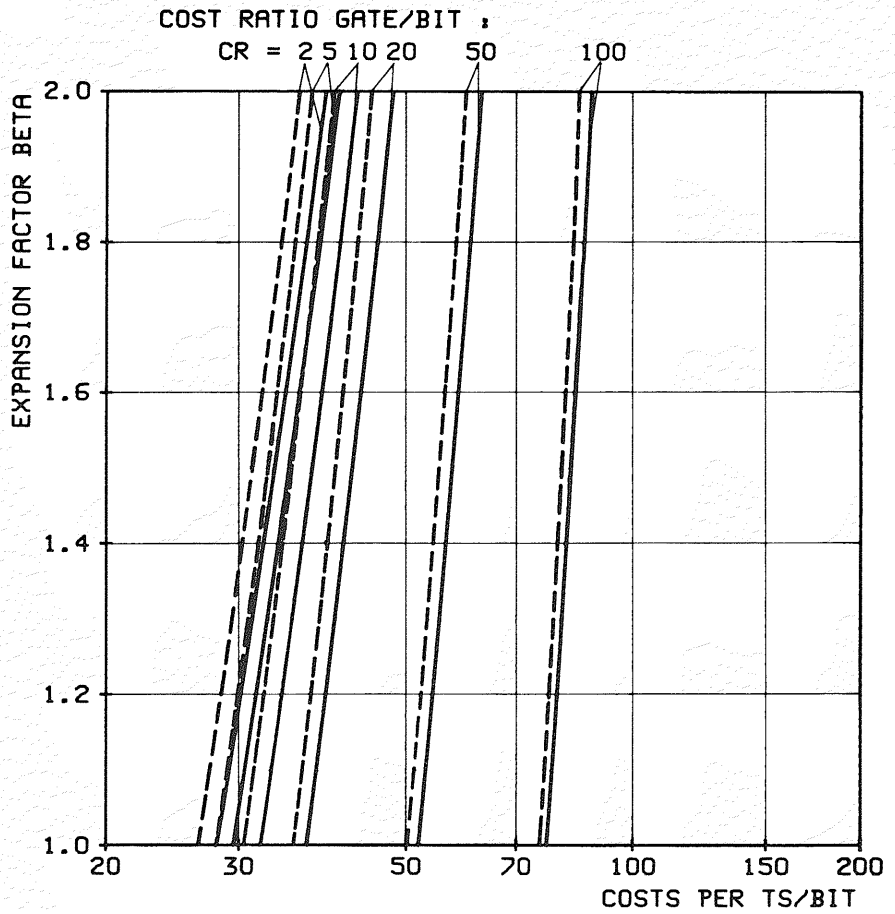
COMBINED SWITCHING 1 × 16 HW H_2 = 4
SEPARATED SWITCHING 2 × 16 HW M = 30

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

-CHART 30-

TSSST

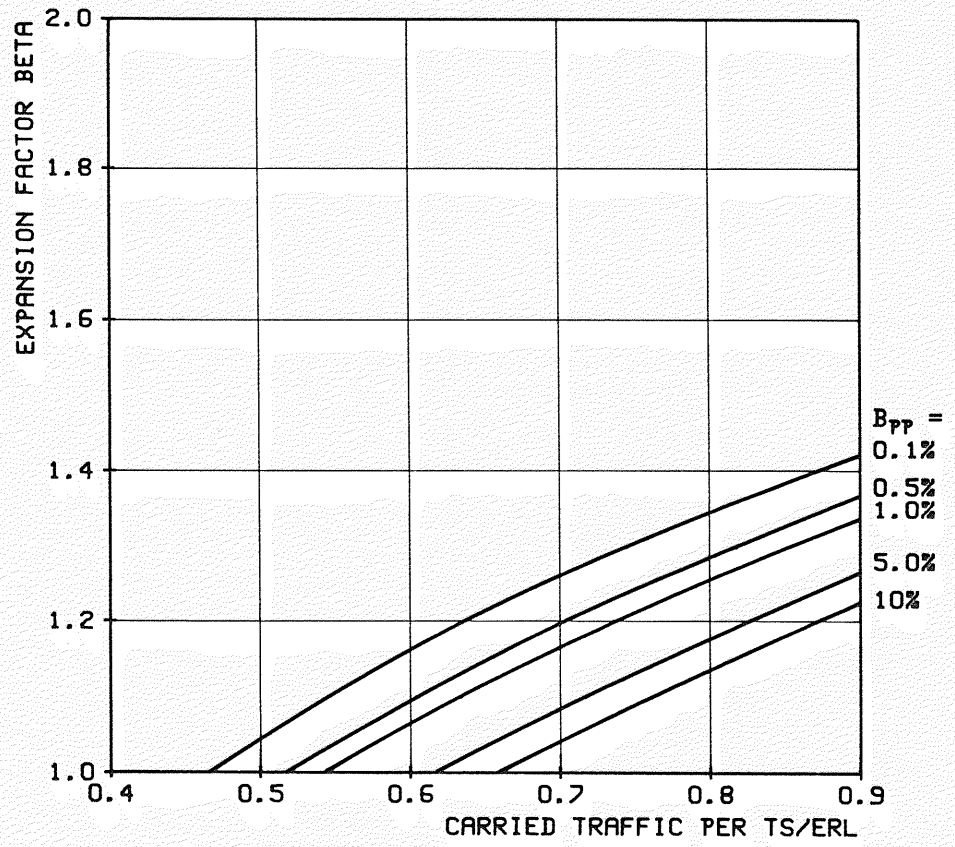


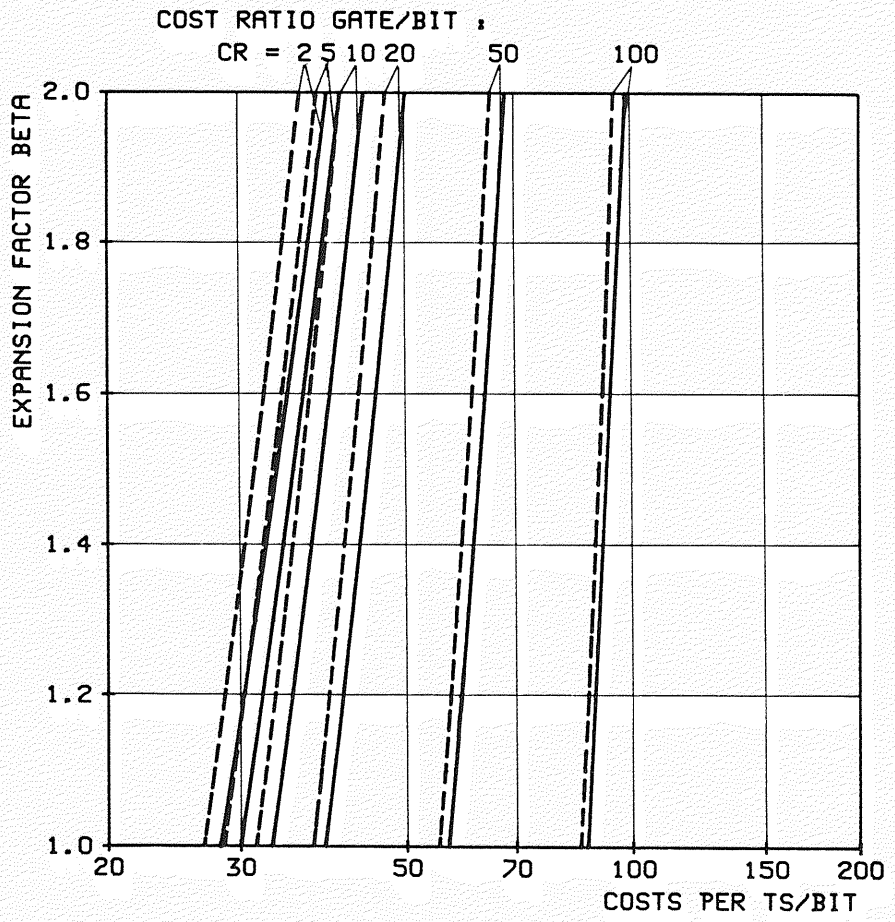


COMBINED SWITCHING 1 × 25 HW H_2 = 5 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 25 HW M = 30 --- SEPARATED SWITCHING

TSSST





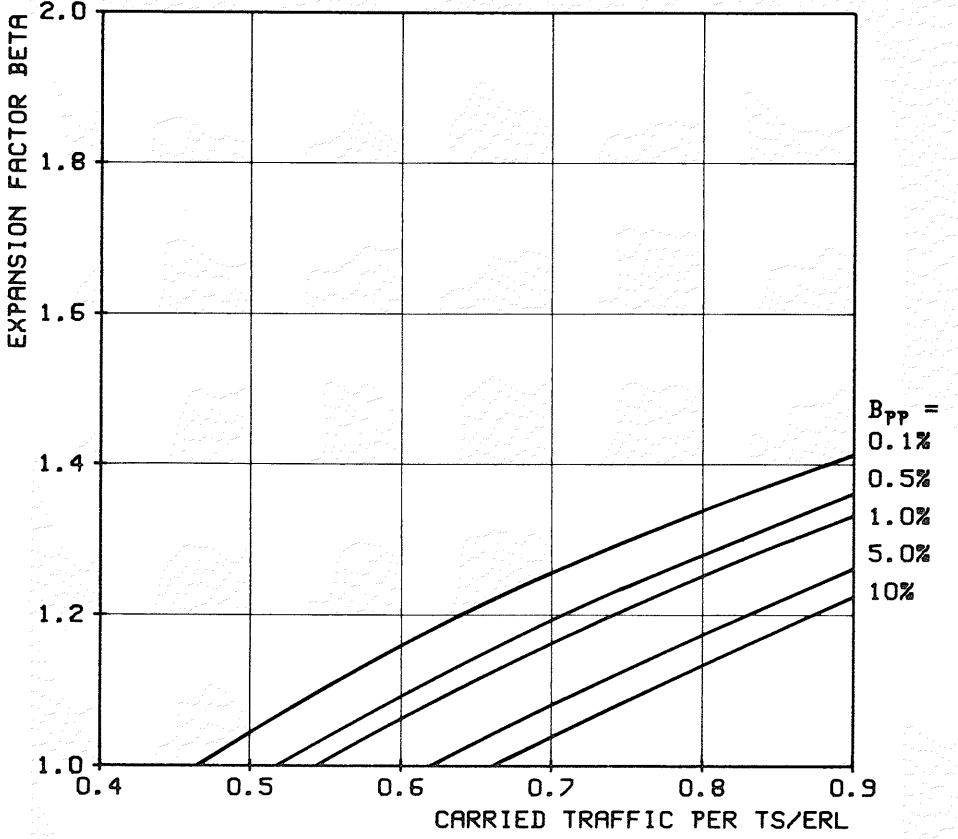
COMBINED SWITCHING 1 × 36 HW H_2 = 6

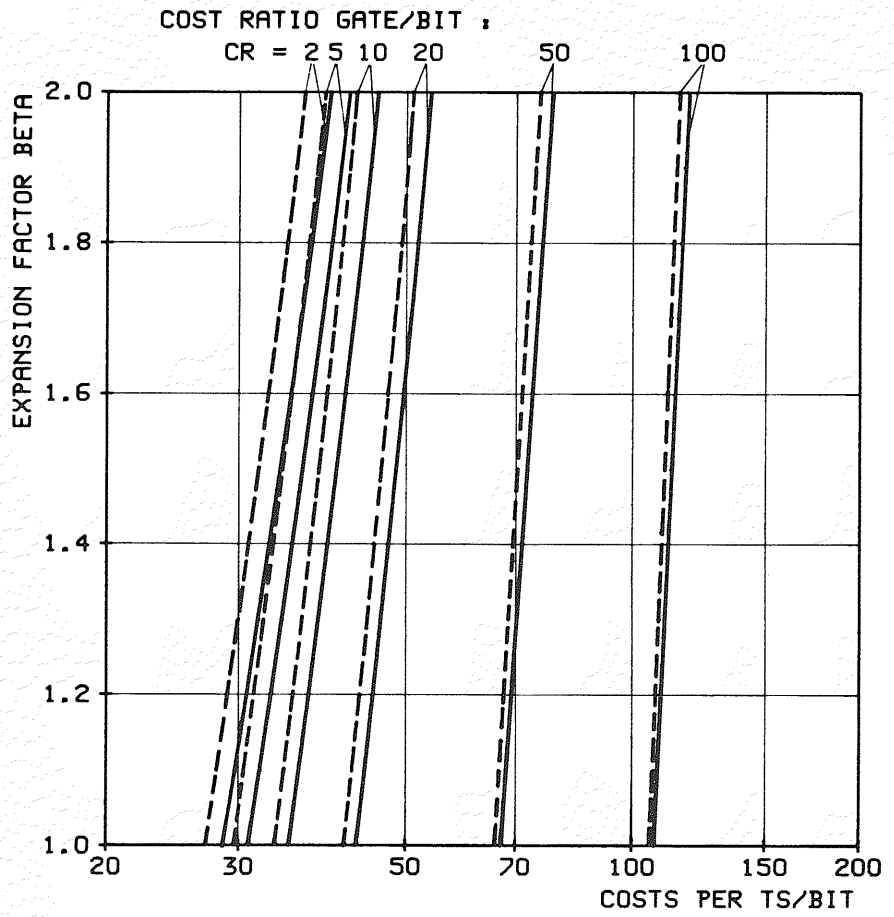
SEPARATED SWITCHING 2 × 36 HW M = 30

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

TSSST

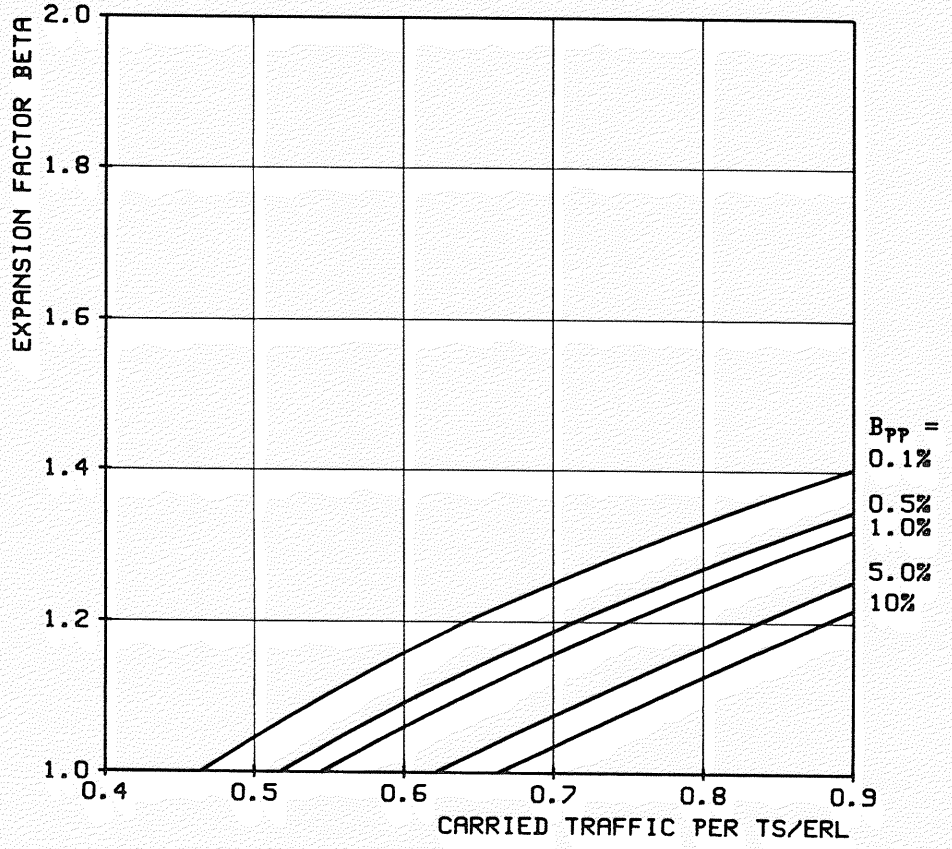


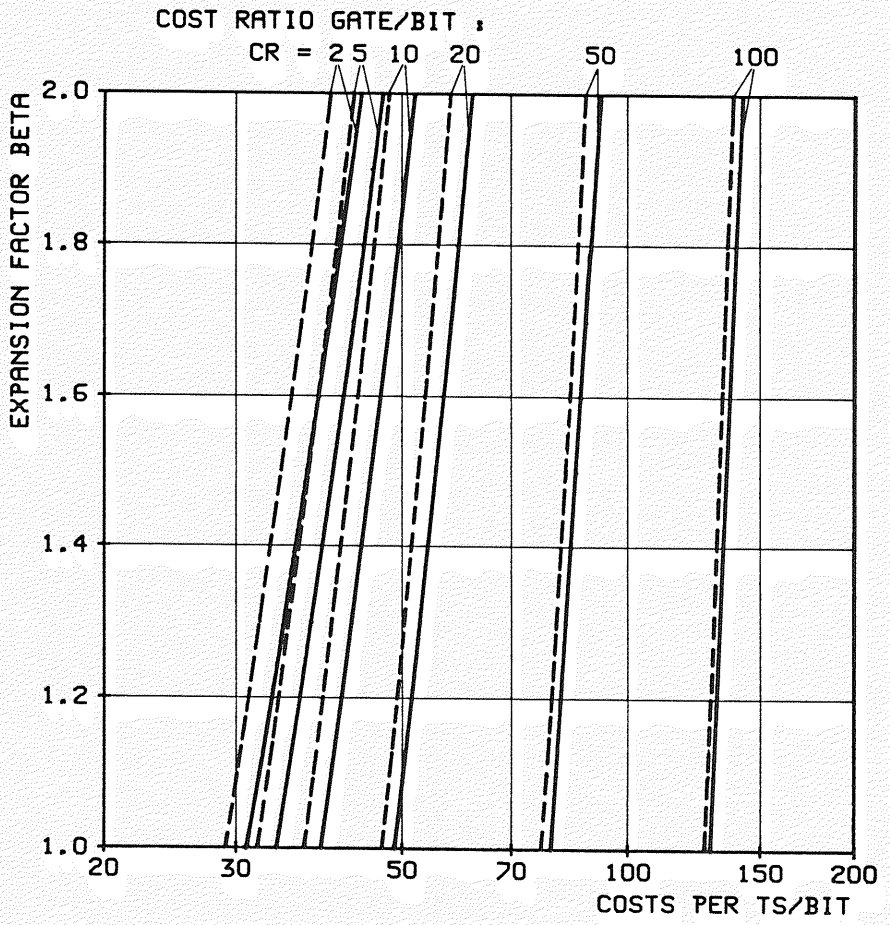


COMBINED SWITCHING 1 × 64 HW H_2 = 8 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 64 HW M = 30 --- SEPARATED SWITCHING

TSSST





COMBINED SWITCHING 1 × 100 HW H_2 = 10

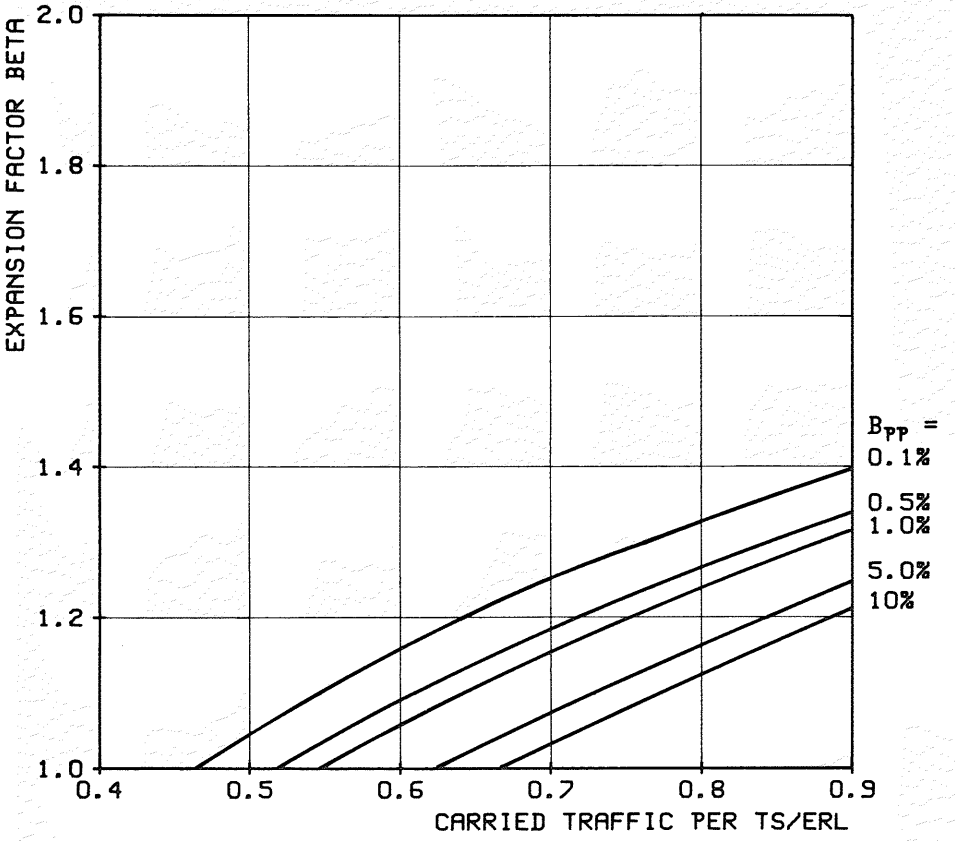
SEPARATED SWITCHING 2 × 100 HW M = 30

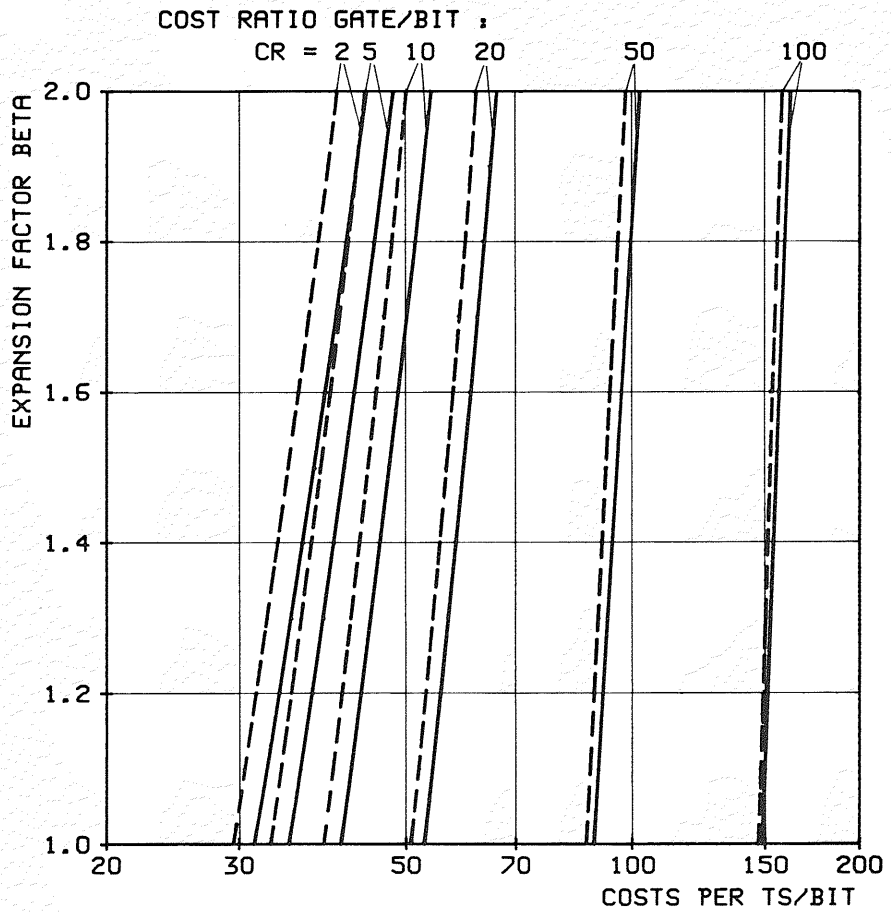
—— COMBINED SWITCHING

--- SEPARATED SWITCHING

-CHART 34-

TSSST

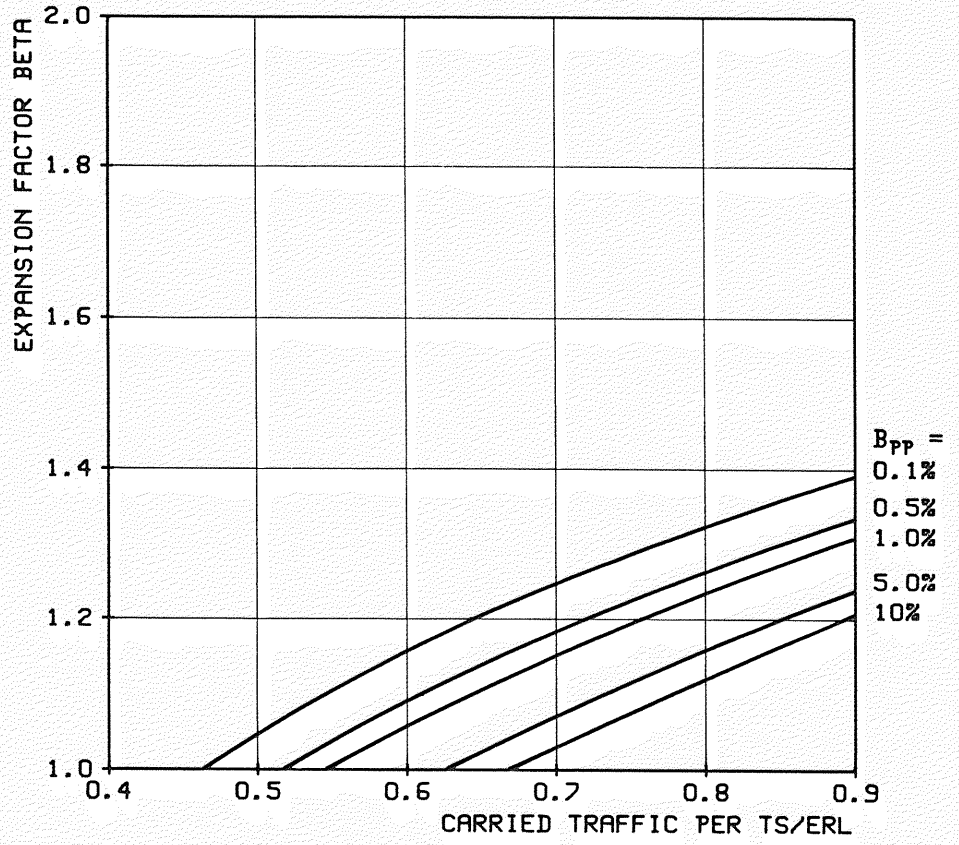


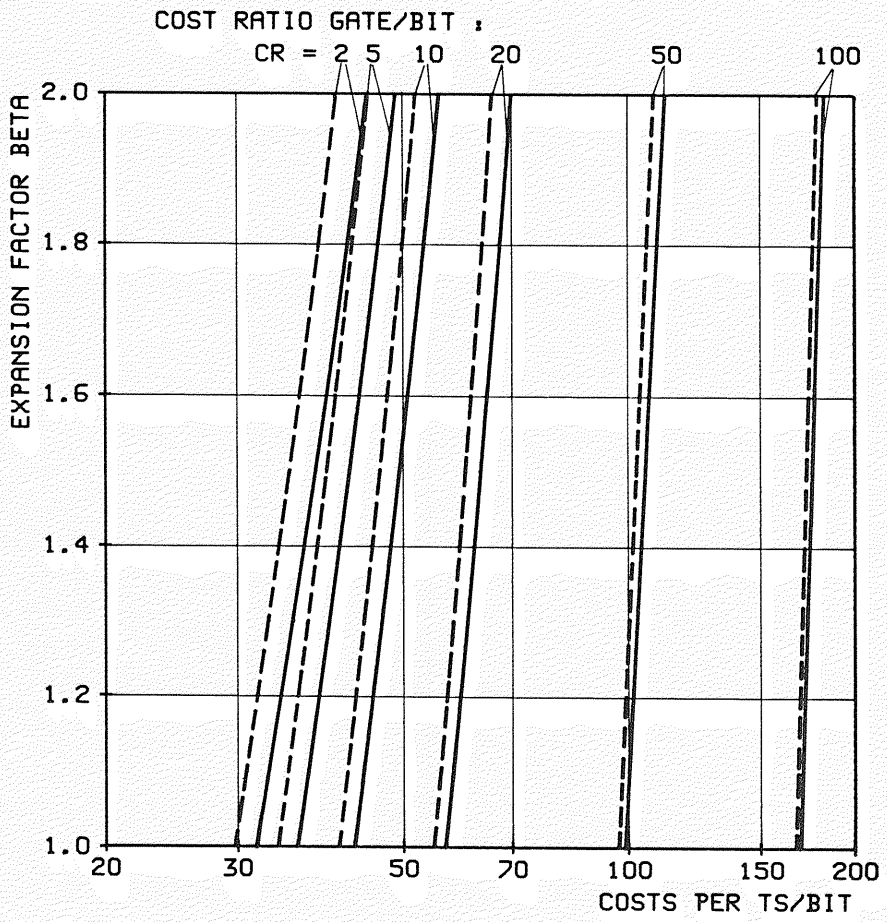


COMBINED SWITCHING 1 × 144 HW H_2 = 12 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 144 HW M = 30 --- SEPARATED SWITCHING

TSSST





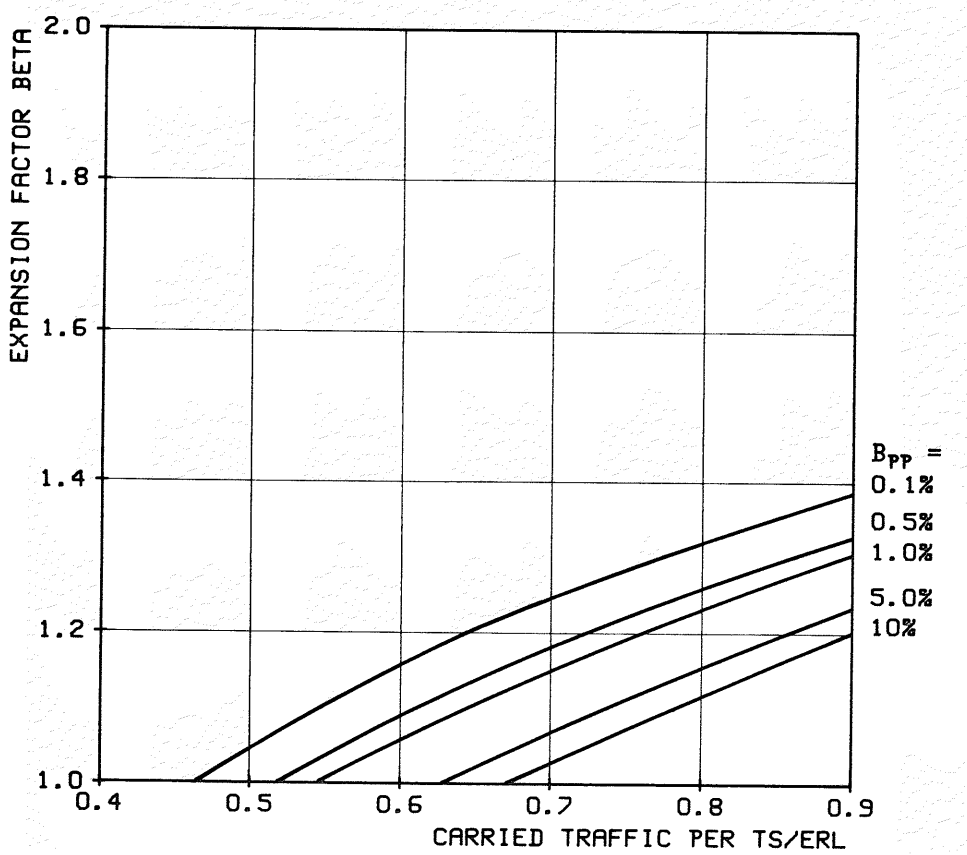
COMBINED SWITCHING 1 × 196 HW H_2 = 14

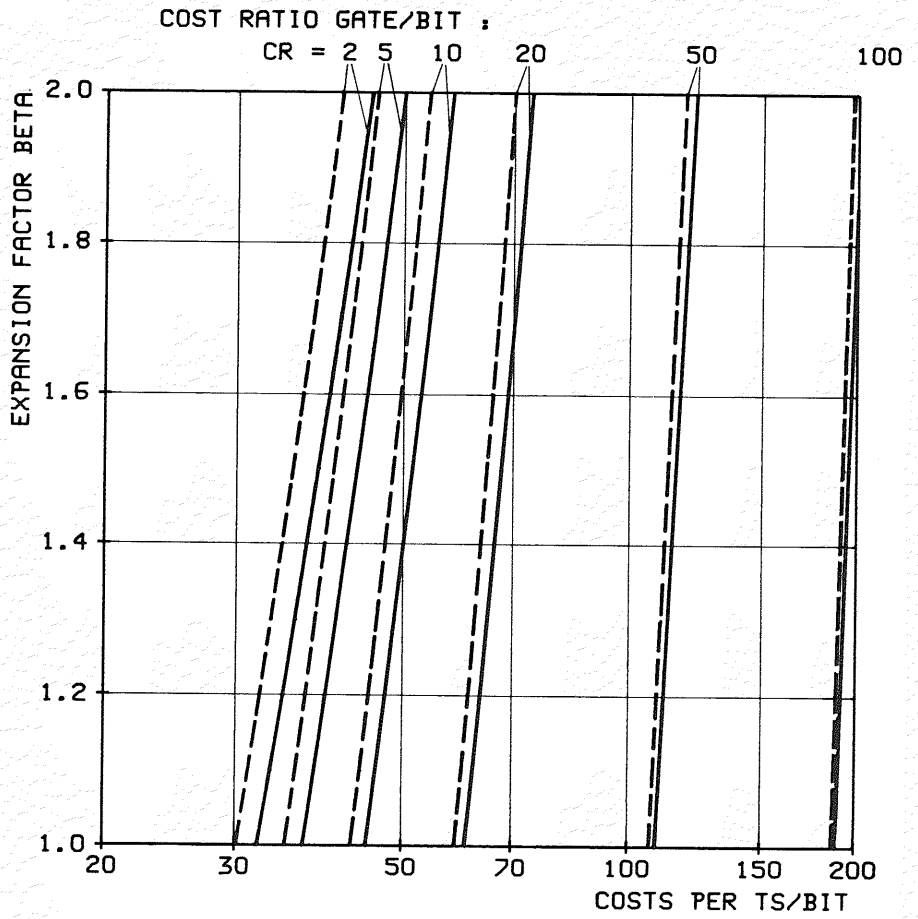
SEPARATED SWITCHING 2 × 196 HW M = 30

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

TSSST

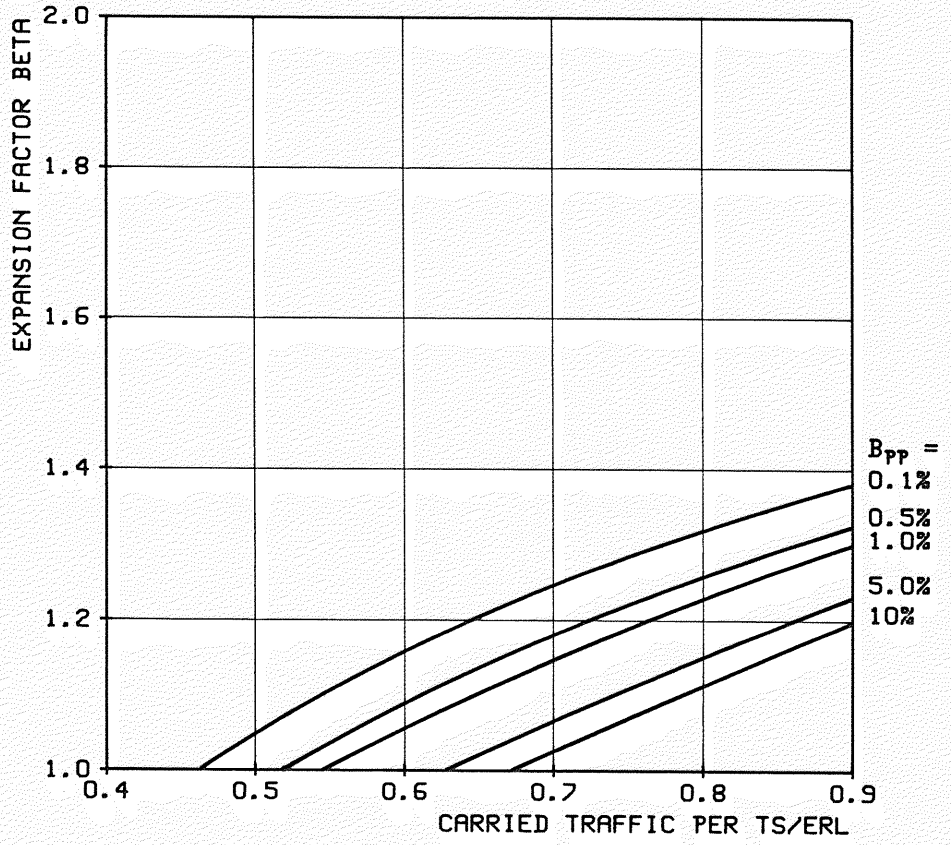


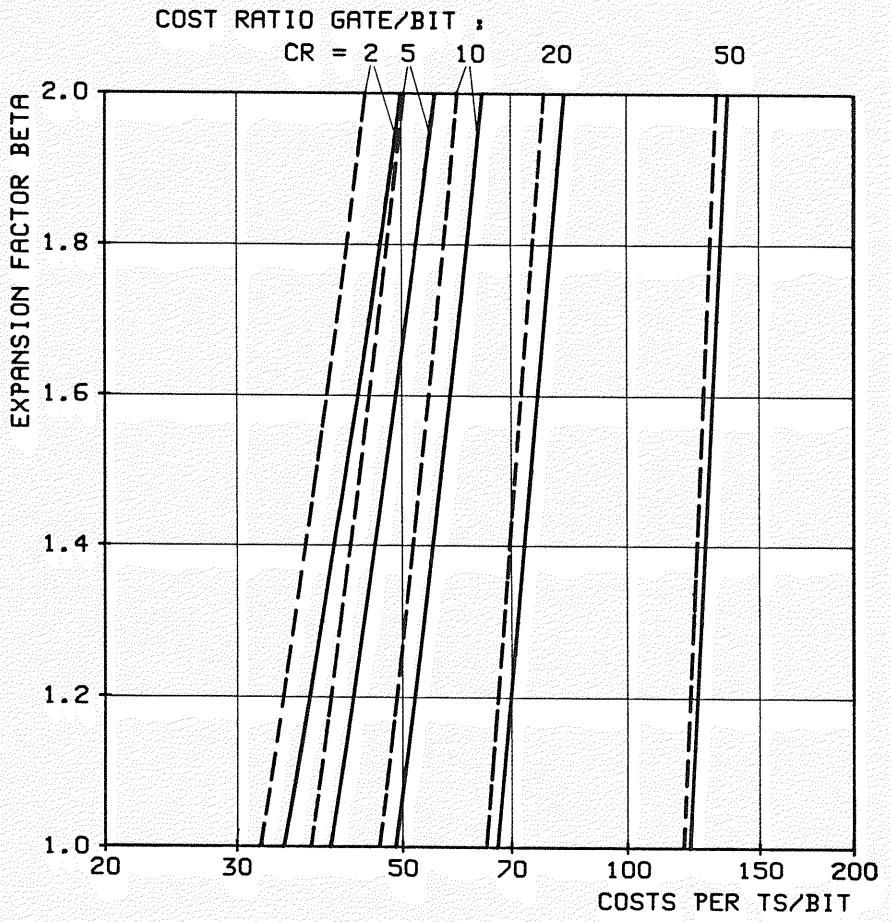


COMBINED SWITCHING 1 × 256 HW H_2 = 16 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 256 HW M = 30 --- SEPARATED SWITCHING

TSSST



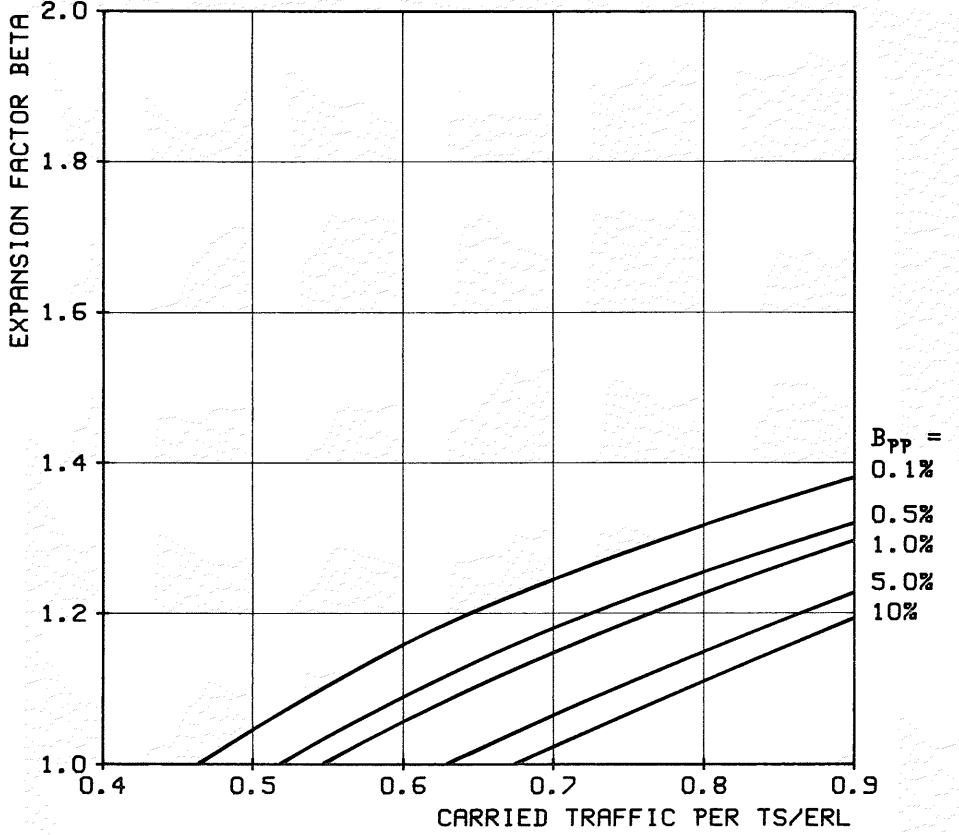


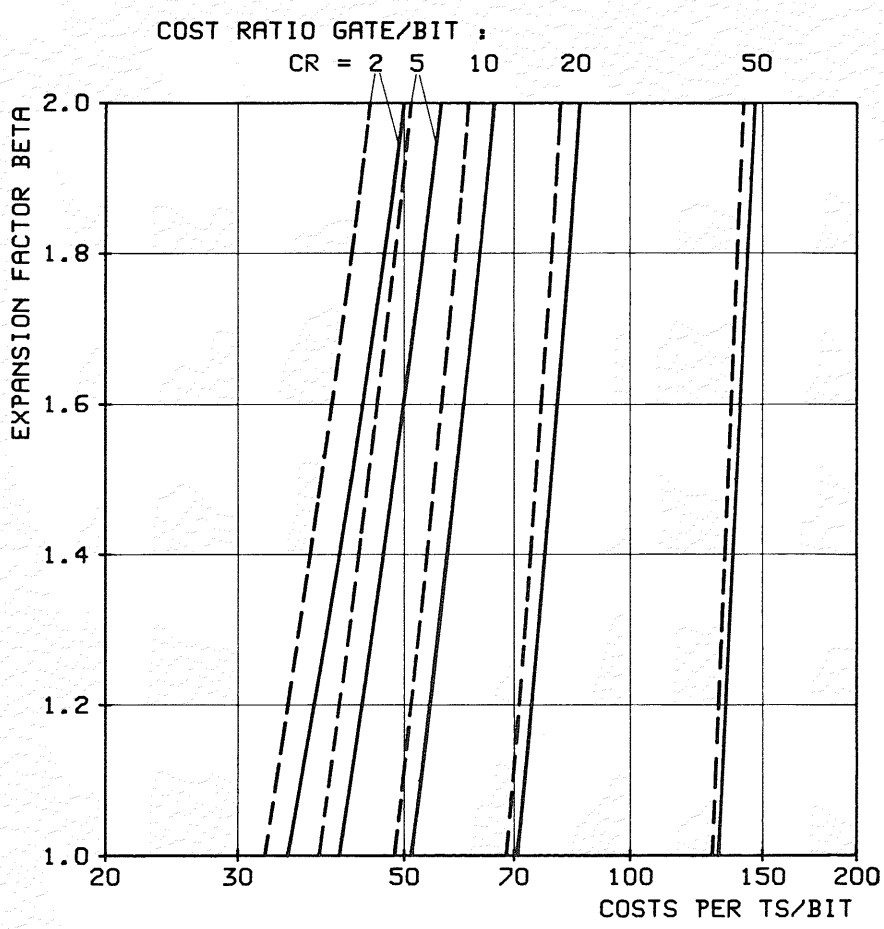
COMBINED SWITCHING 1 × 324 HW H_2 = 18
SEPARATED SWITCHING 2 × 324 HW M = 30

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

-CHART 38-

TSSST





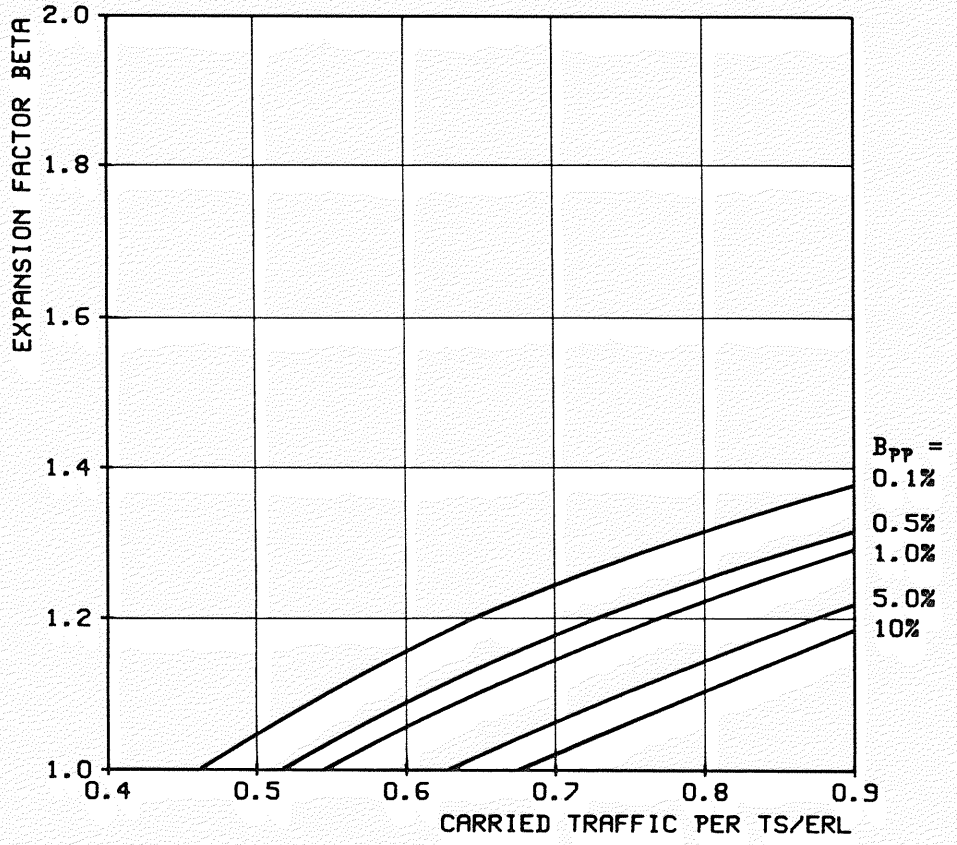
COMBINED SWITCHING 1 × 400 HW H_2 = 20

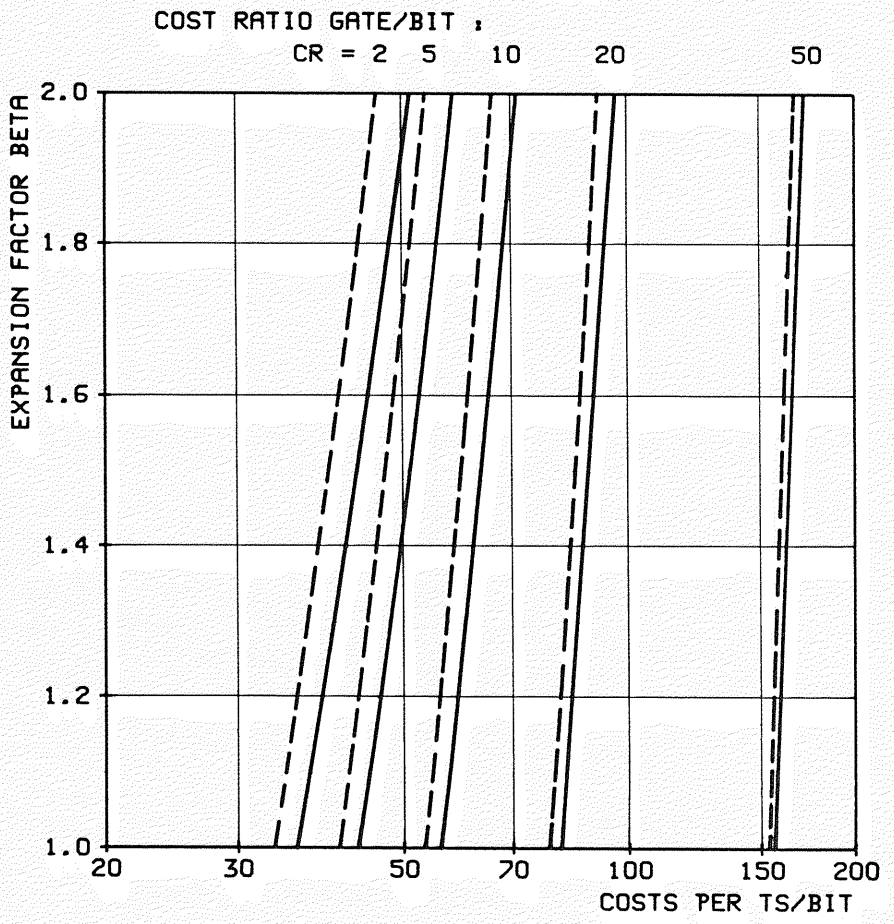
SEPARATED SWITCHING 2 × 400 HW M = 30

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

TSSST



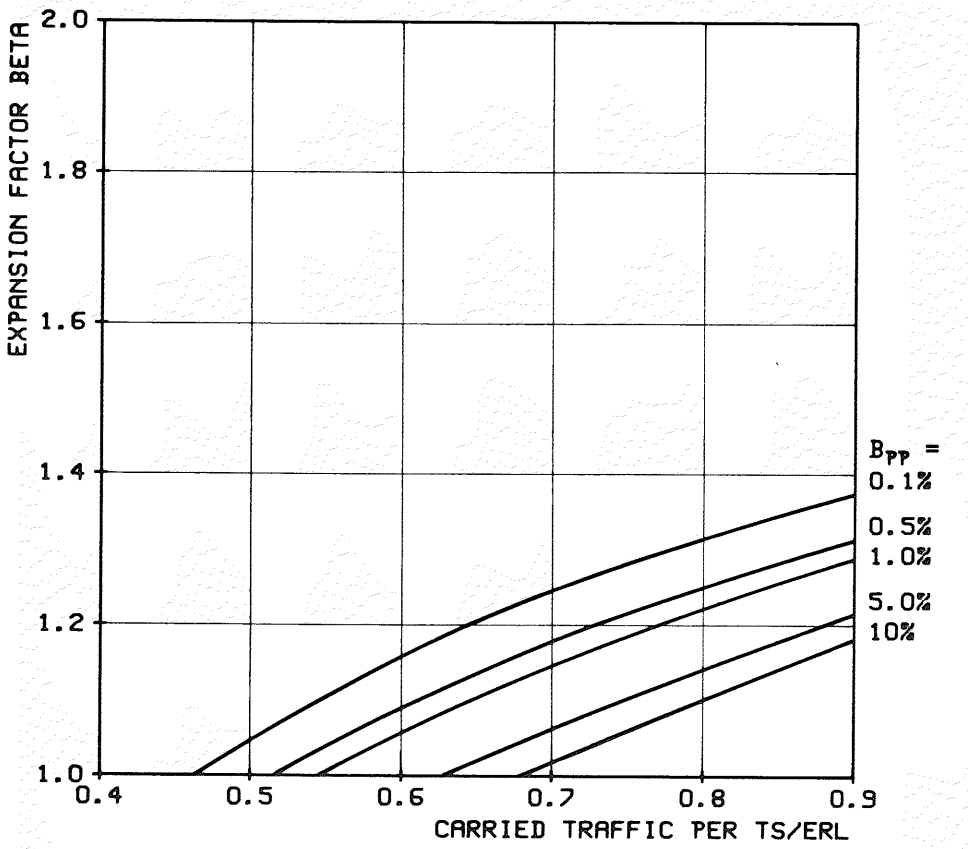


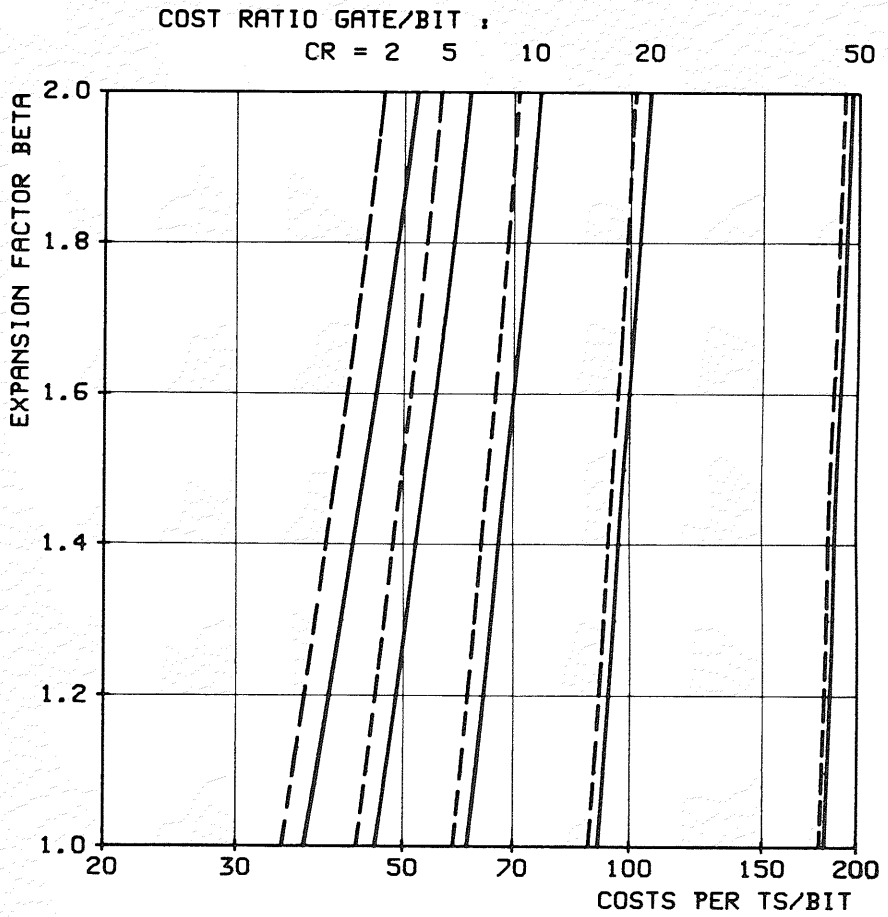
COMBINED SWITCHING 1 × 625 HW H_2 = 25
SEPARATED SWITCHING 2 × 625 HW M = 30

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

-CHART 40-

TSSST





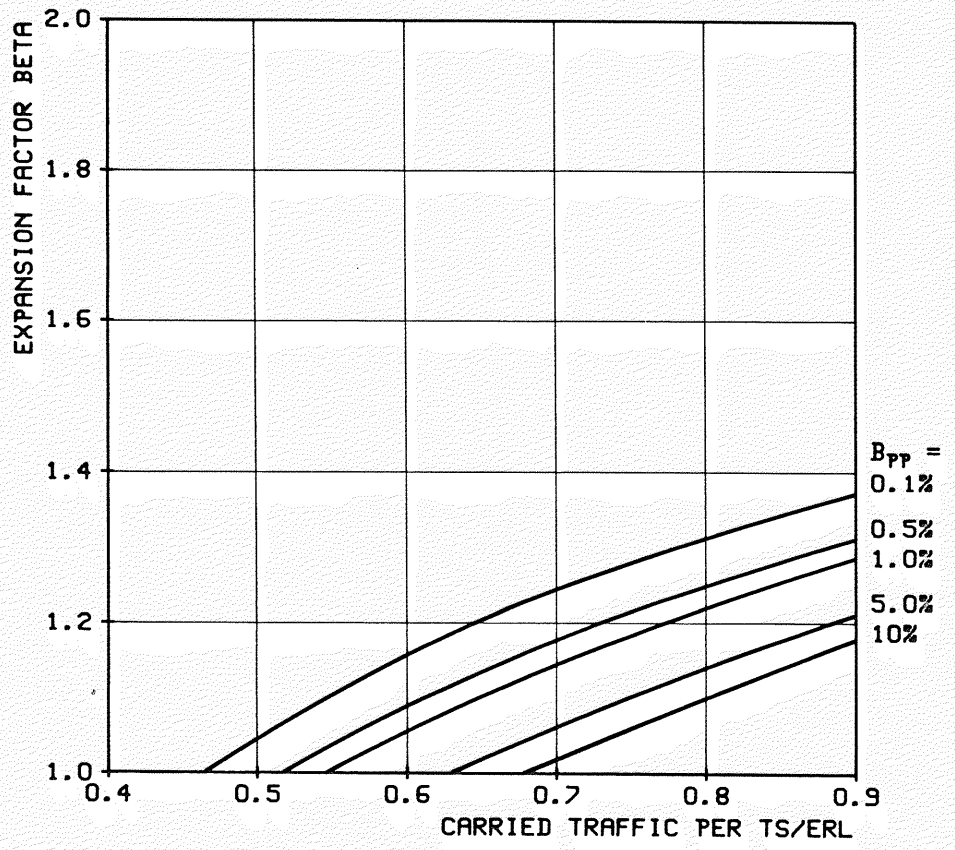
COMBINED SWITCHING 1 × 900 HW H_2 = 30

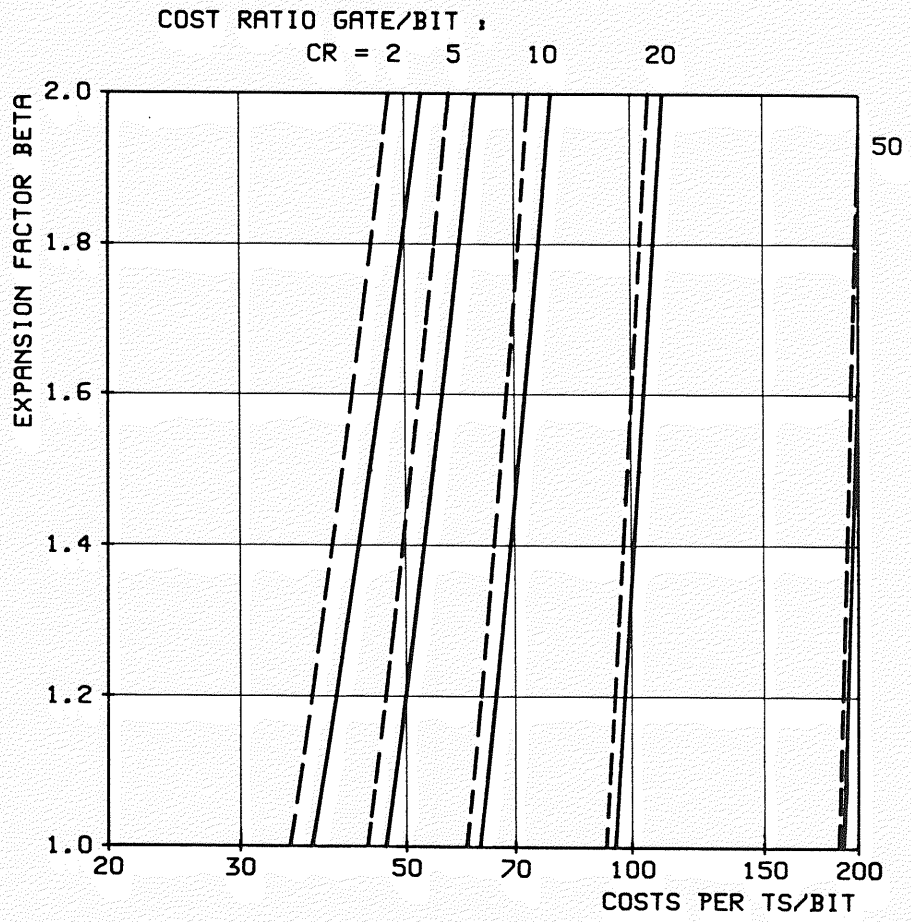
SEPARATED SWITCHING 2 × 900 HW M = 30

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

TSSST





COMBINED SWITCHING 1 × 1024 HW H_2 = 32

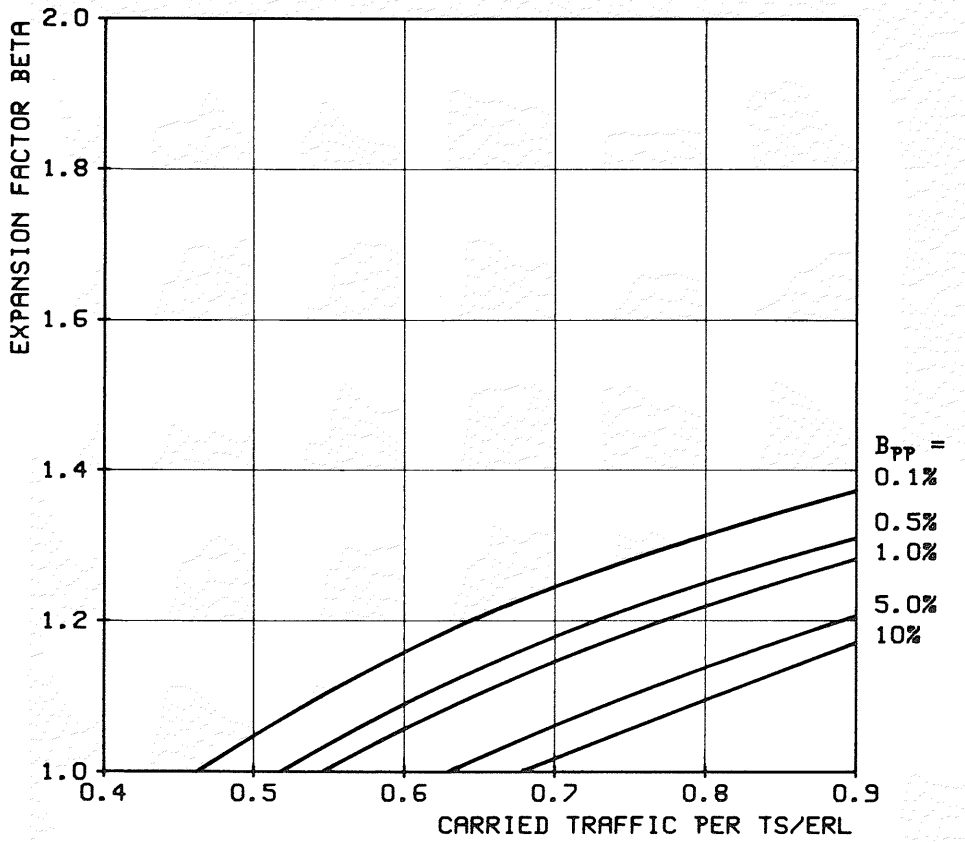
SEPARATED SWITCHING 2 × 1024 HW M = 30

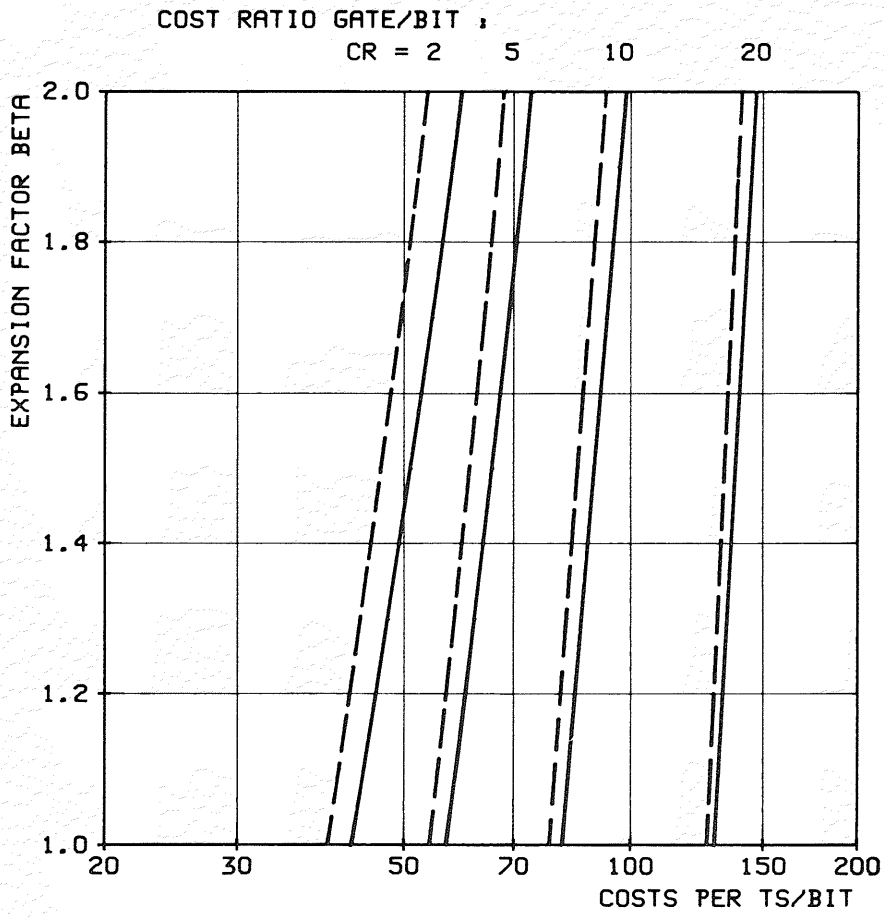
—— COMBINED SWITCHING

--- SEPARATED SWITCHING

-CHART 42-

TSSST

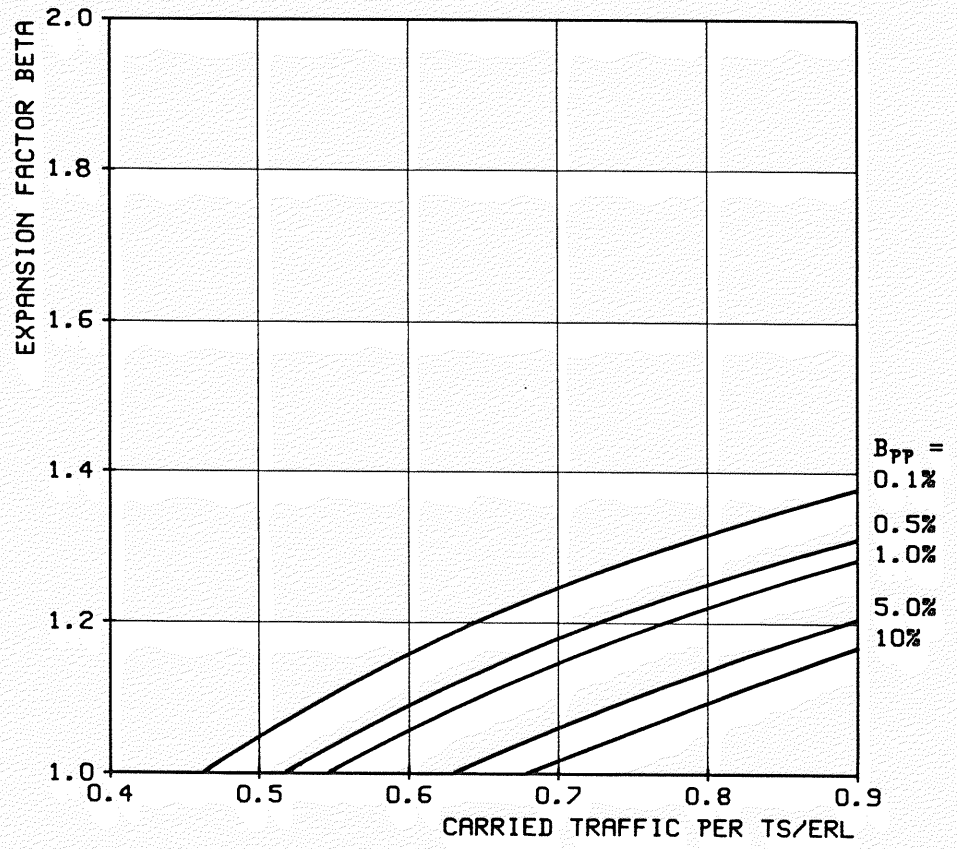


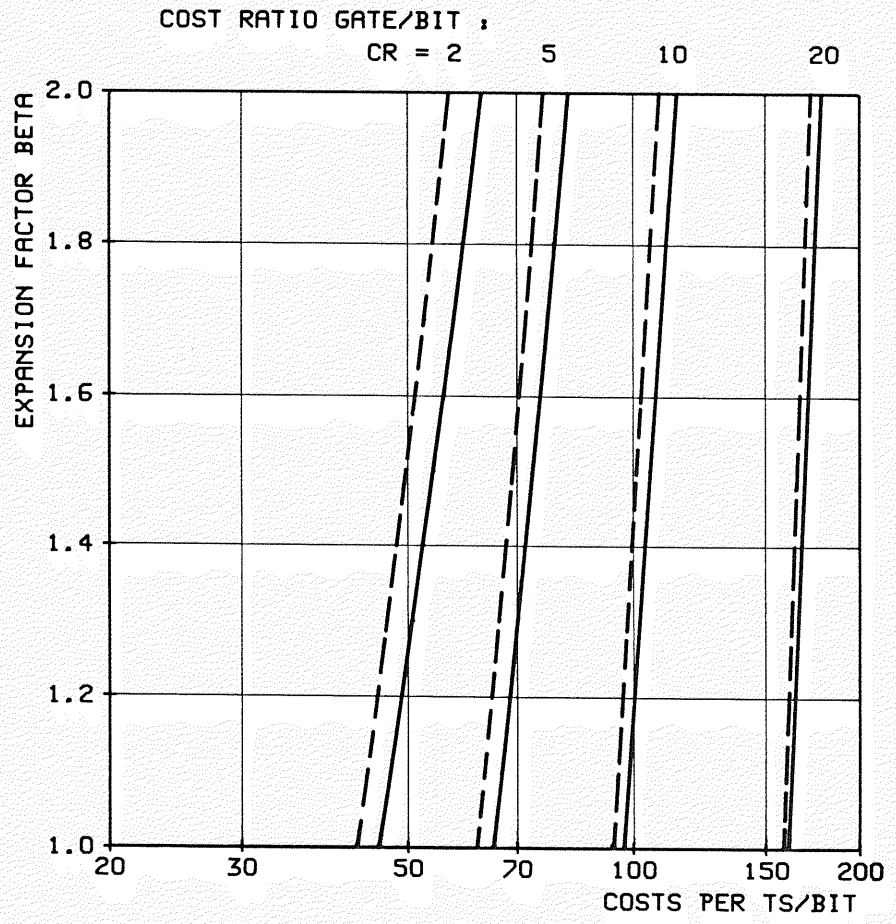


COMBINED SWITCHING 1 × 2304 HW H_2 = 48 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 2304 HW M = 30 --- SEPARATED SWITCHING

TSSST





COMBINED SWITCHING 1 × 4096 HW H_2 = 64 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 4096 HW M = 30 --- SEPARATED SWITCHING

PCM SWITCHING ARRAY : SSTSS

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 16, 25, 36, 64, 100,
144, 196, 256, 324, 400,
625, 900, 1024, 2304, 4096,

SEPARATED SWITCHING : HW = 32, 50, 72, 128, 200,
288, 392, 512, 648, 800,
1250, 1800, 2048, 4608, 8192,

TIME-SLOTS (TS) PER HW : M = 30 TS

POINT-TO-POINT LOSS, PCT1 : B_{PP} = 0.1, 0.5, 1.0, 5.0, 10.0%

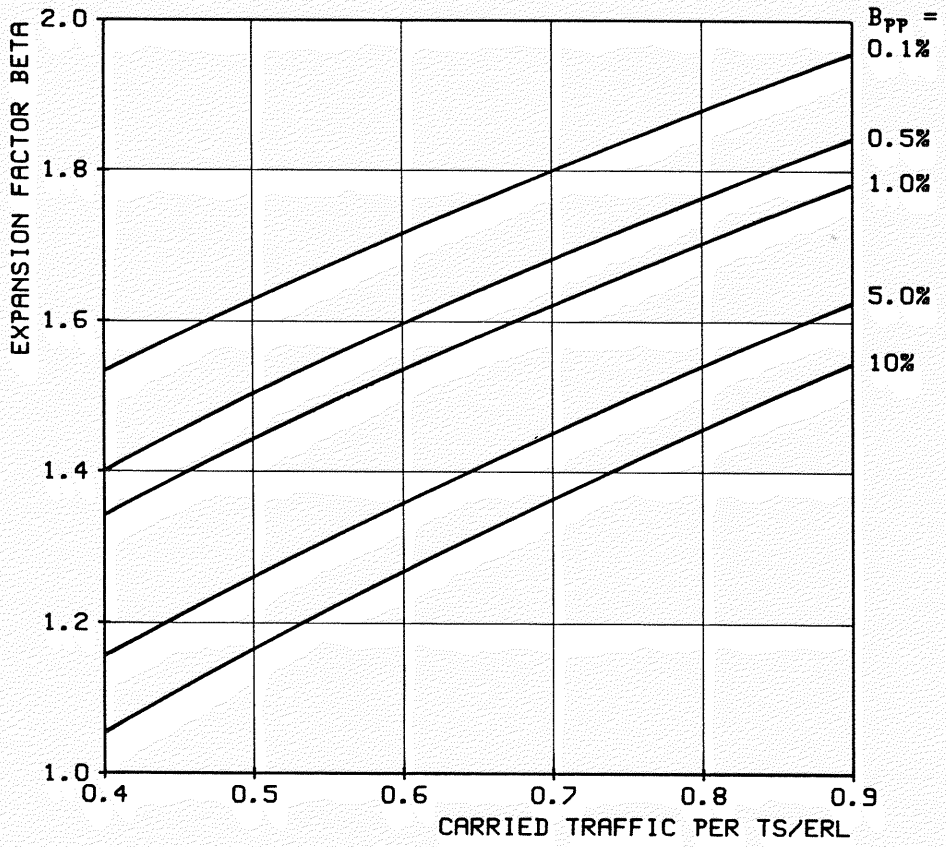
COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

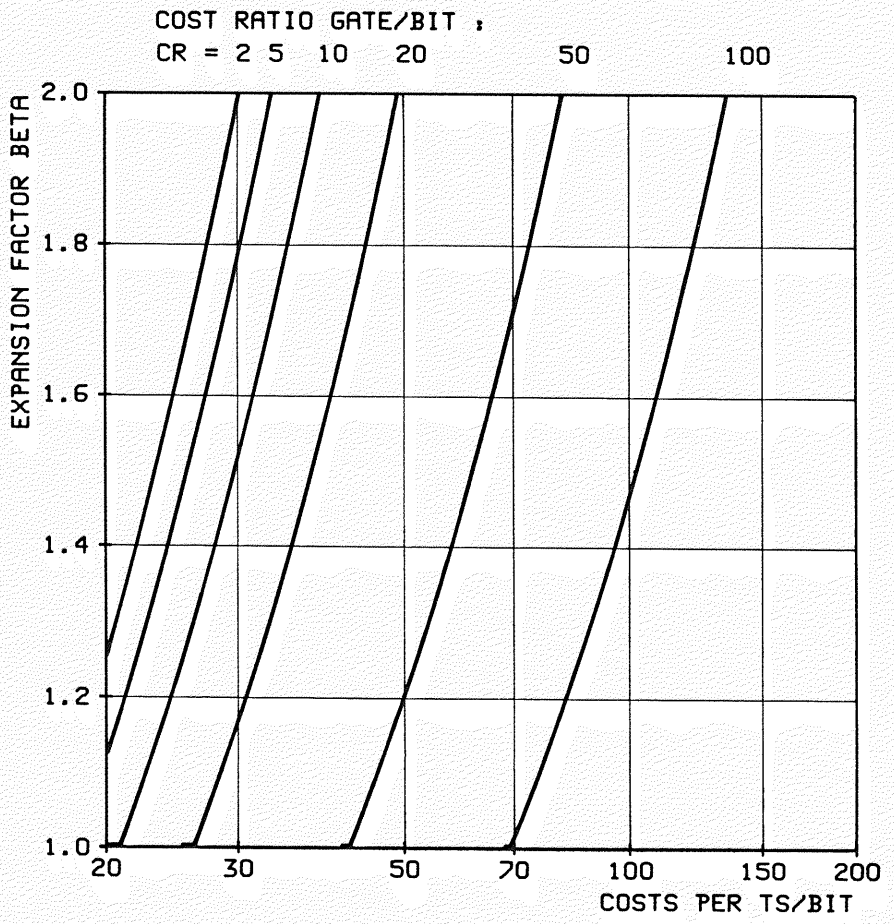
BLOCK SIZE

COMBINED SWITCHING : $H_1 = \sqrt{HW}$

SEPARATED SWITCHING : $H_1 = \sqrt{HW/2}$

SSTSS



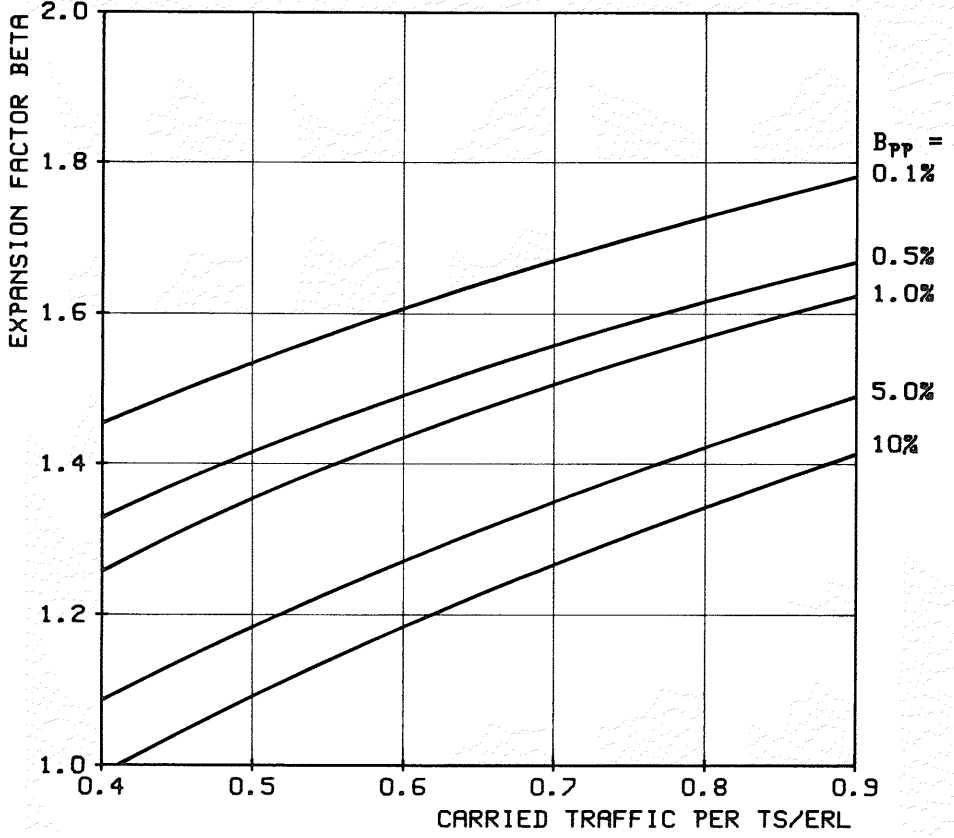


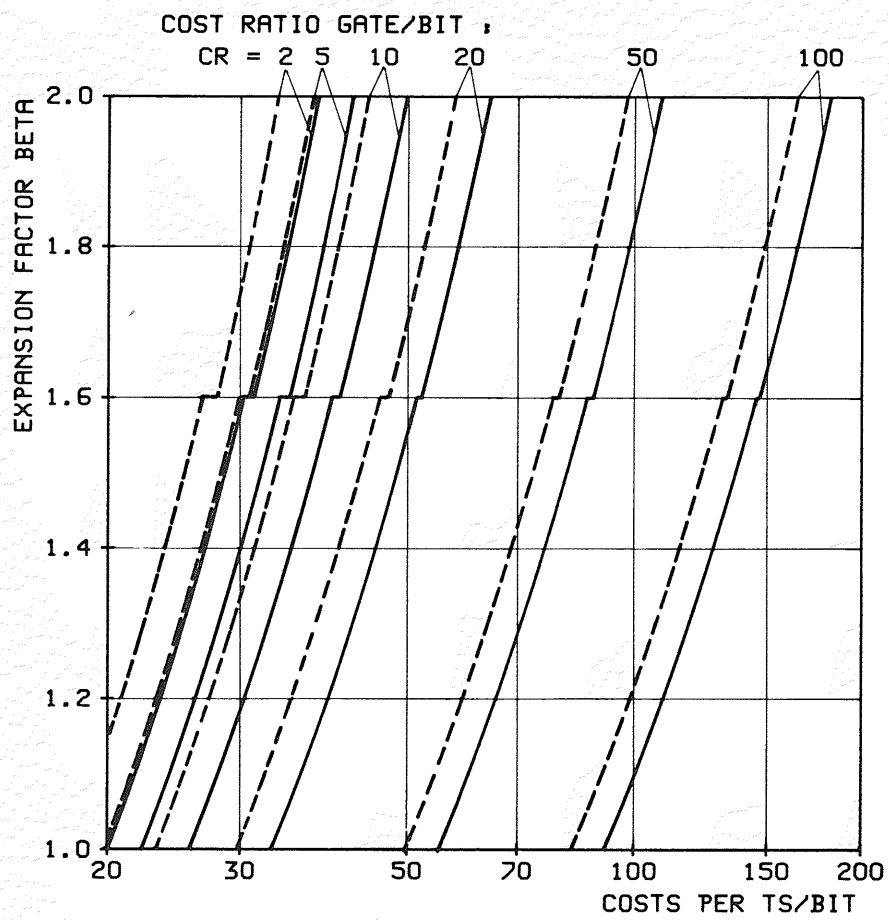
COMBINED SWITCHING 1 × 16 HW H_1 = 4
SEPARATED SWITCHING 2 × 16 HW M = 30

——{ COMBINED SWITCHING
SEPARATED SWITCHING

-CHART 45-

SSTSS

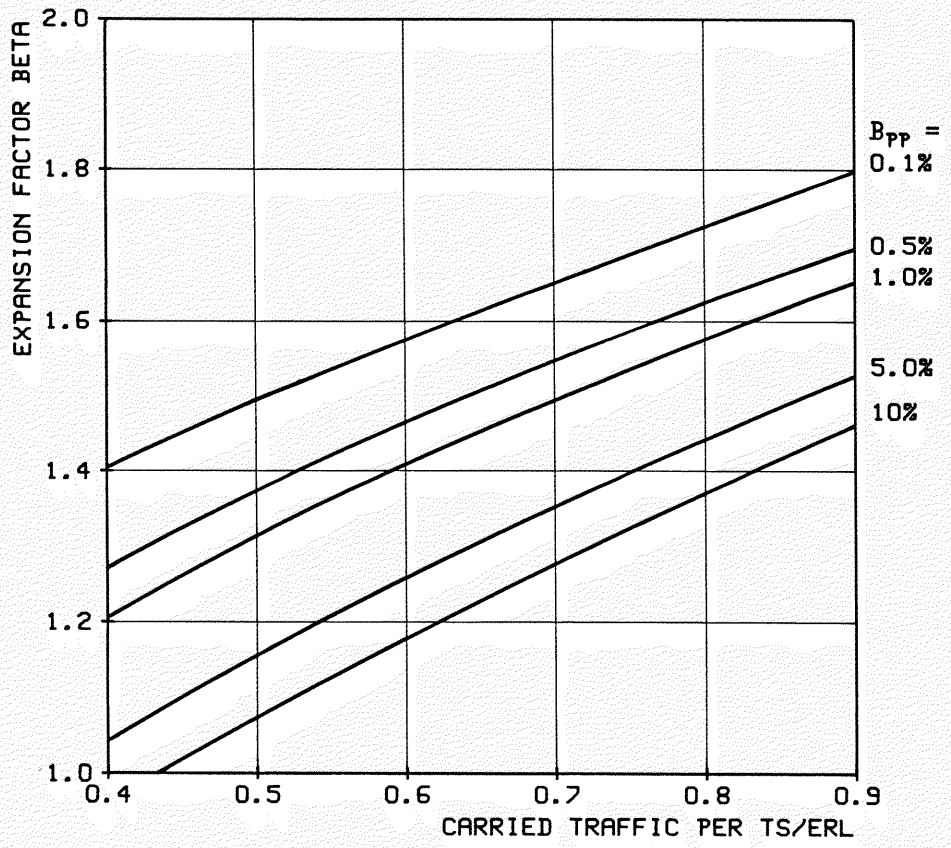


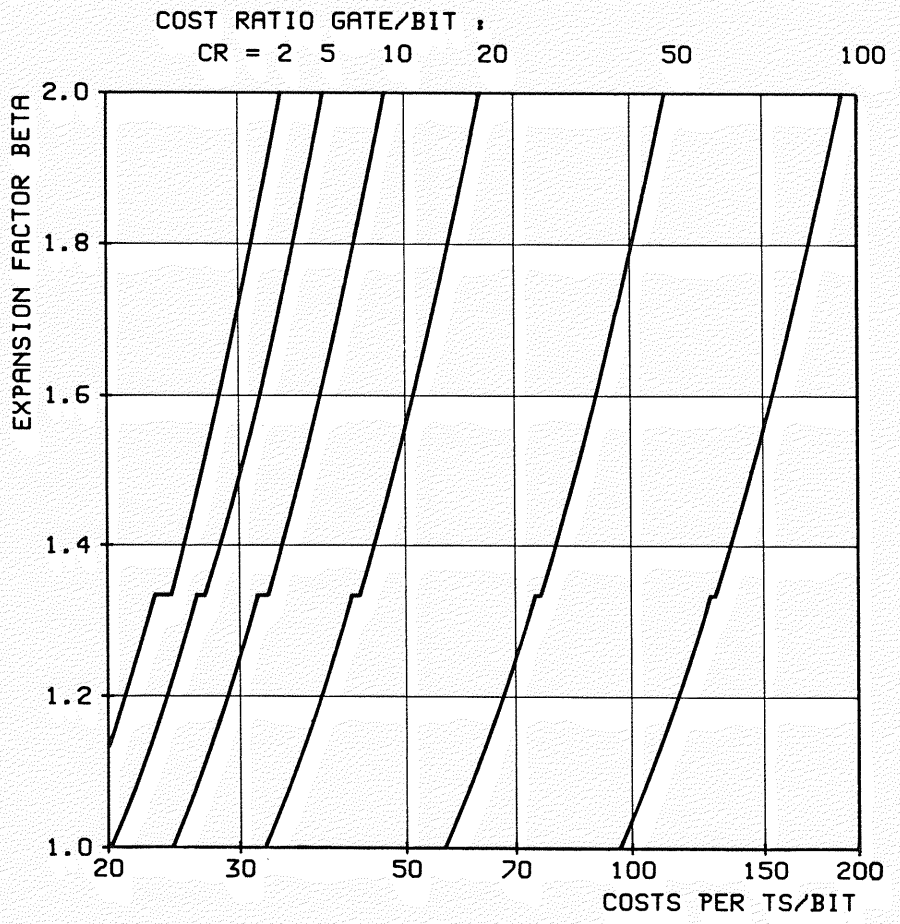


COMBINED SWITCHING 1 × 25 HW H_1 = 5
SEPARATED SWITCHING 2 × 25 HW M = 30

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

SSTSS

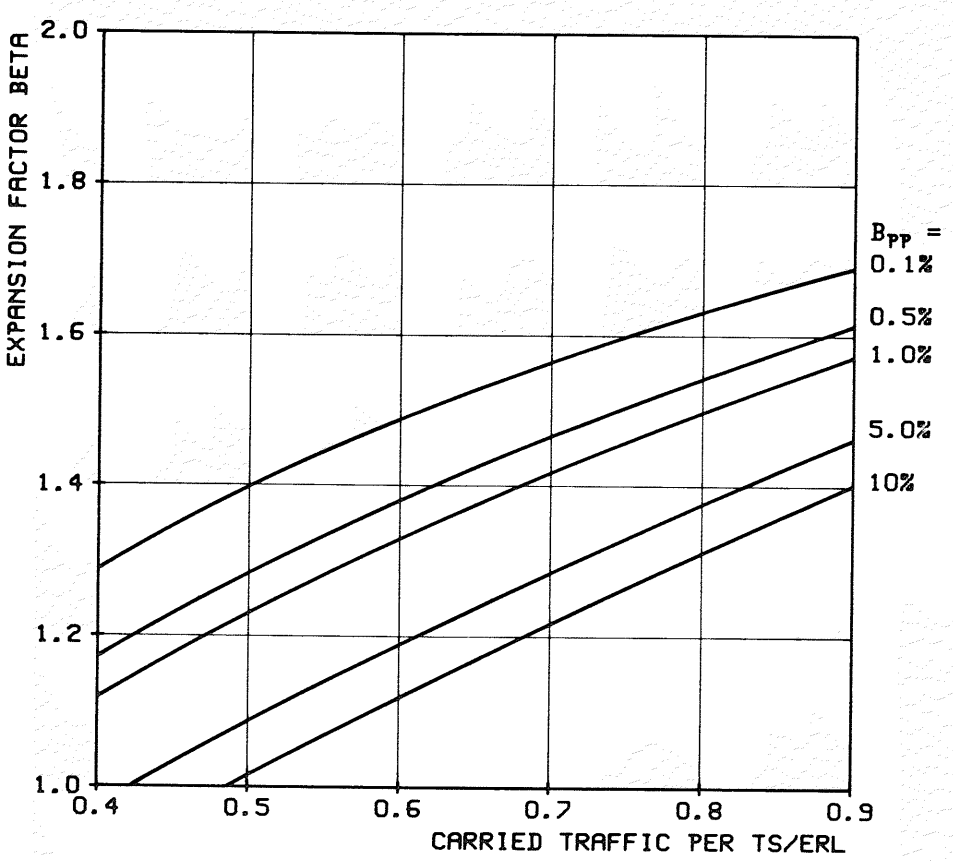


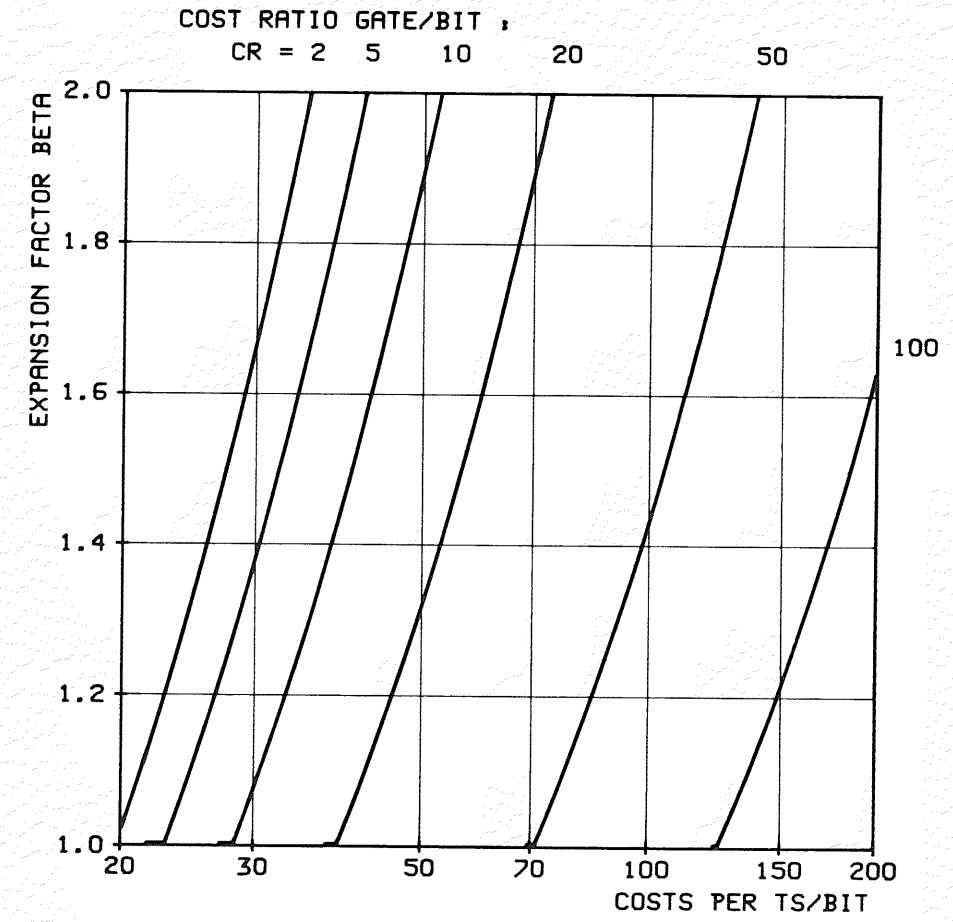


COMBINED SWITCHING	1 × 36 HW	H_1 = 6
SEPARATED SWITCHING	2 × 36 HW	M = 30

— { COMBINED SWITCHING
{ SEPARATED SWITCHING

SSTSS

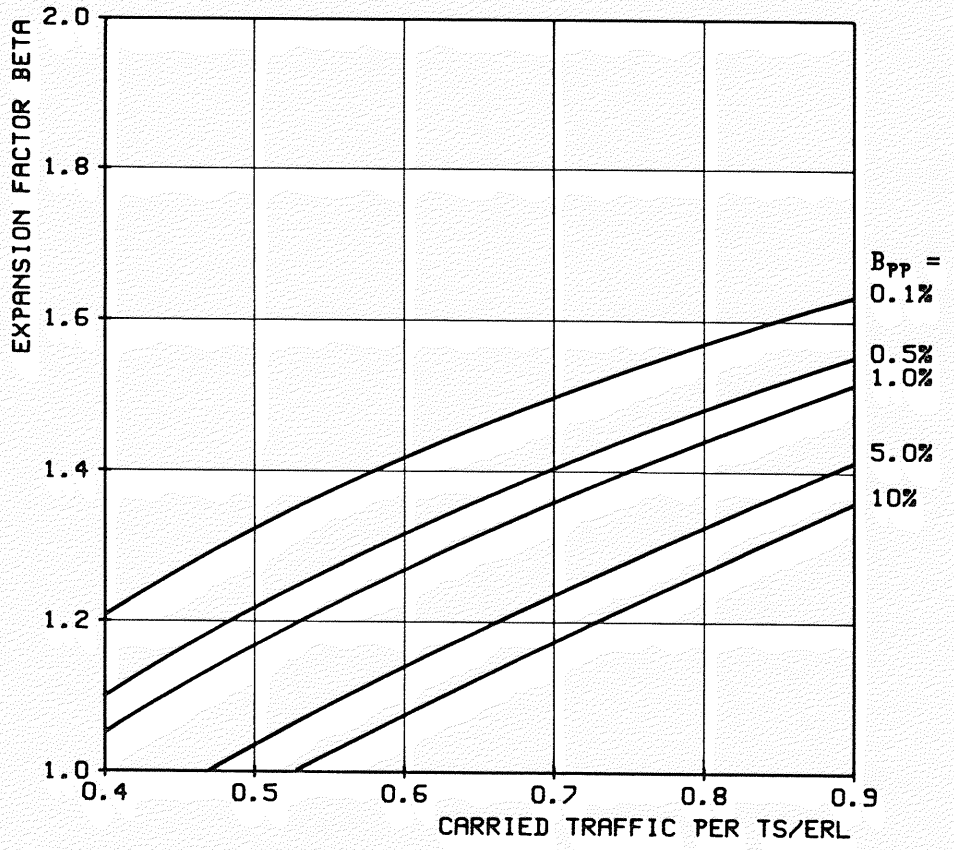


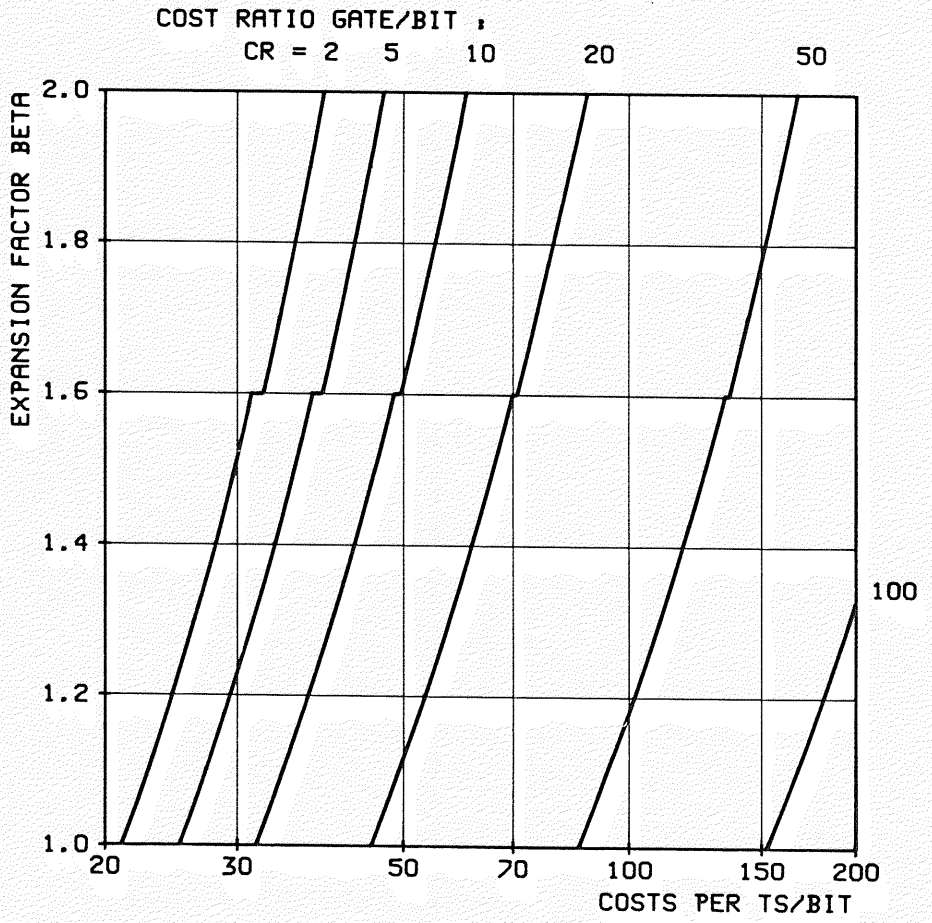


COMBINED SWITCHING 1 × 64 HW H_1 = 8
SEPARATED SWITCHING 2 × 64 HW M = 30

—— { COMBINED SWITCHING
SEPARATED SWITCHING

SSTSS

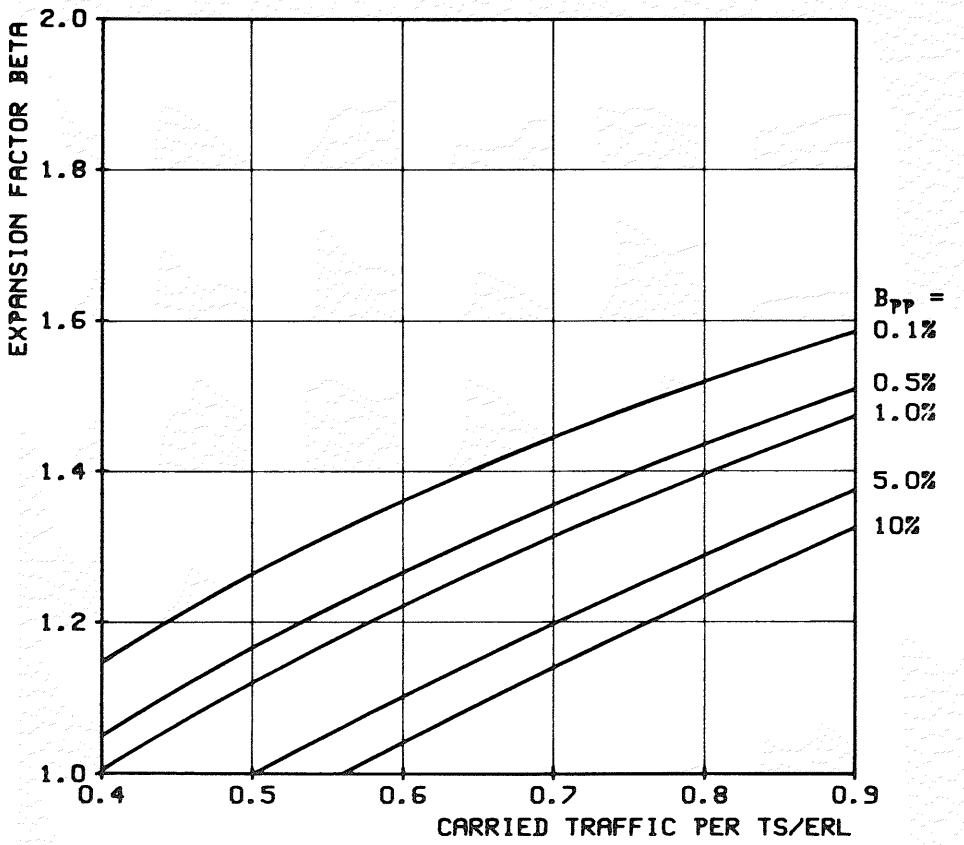


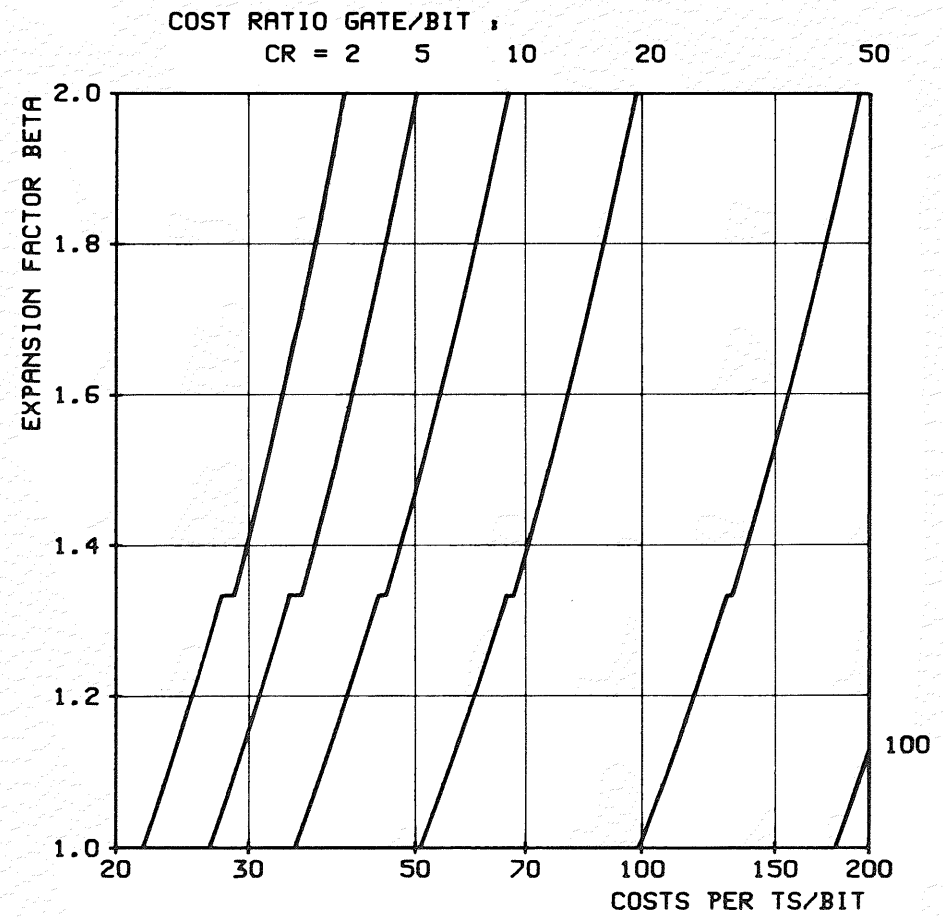


COMBINED SWITCHING 1 × 100 HW H_1 = 10
SEPARATED SWITCHING 2 × 100 HW M = 30

—— { COMBINED SWITCHING
SEPARATED SWITCHING

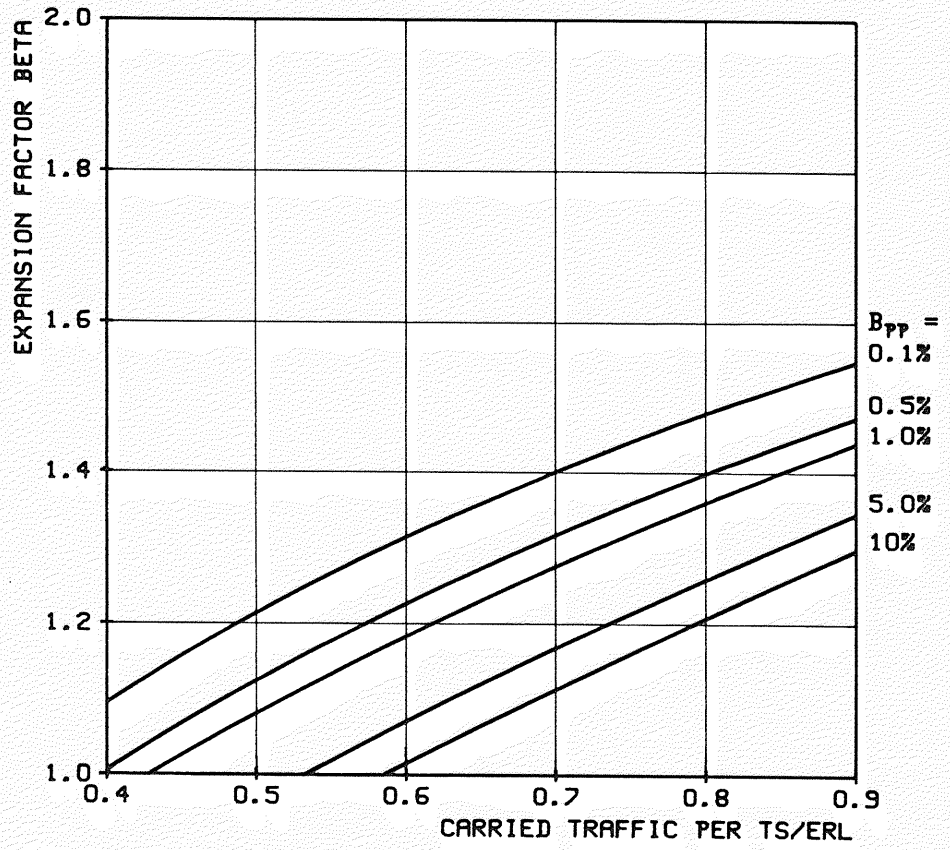
SSTSS

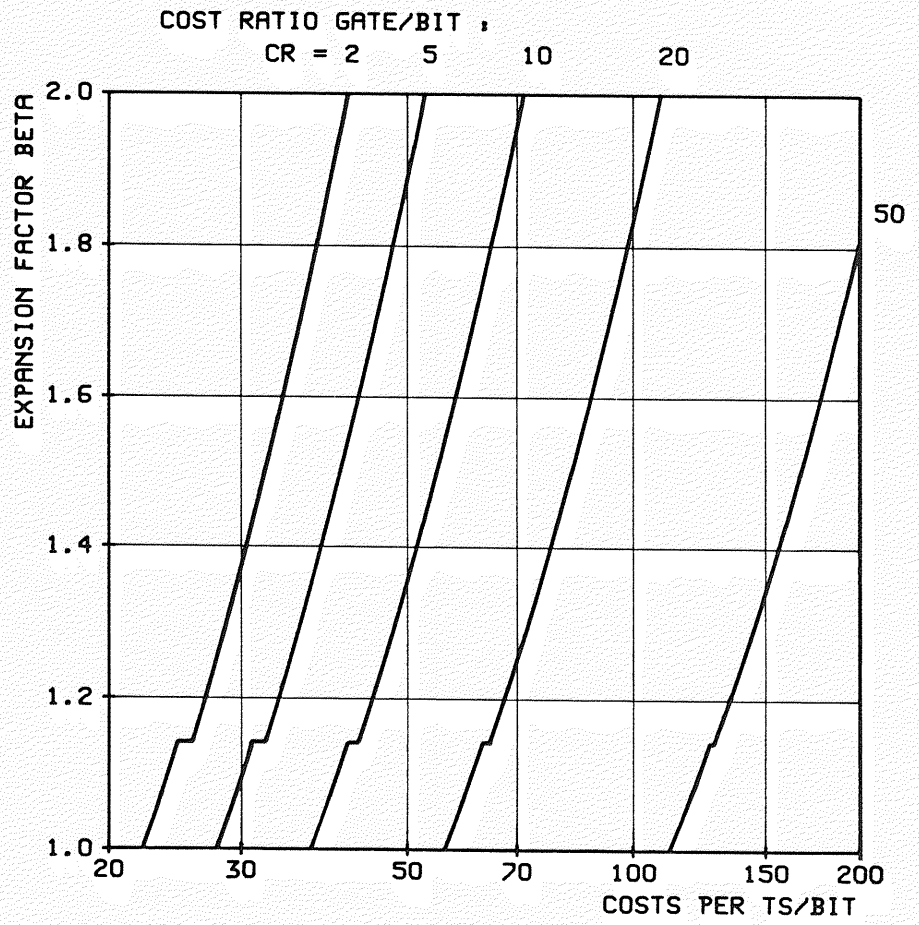




COMBINED SWITCHING	1 × 144 HW	H_1 = 12	——{ COMBINED SWITCHING
SEPARATED SWITCHING	2 × 144 HW	M = 30	{ SEPARATED SWITCHING

SSTSS



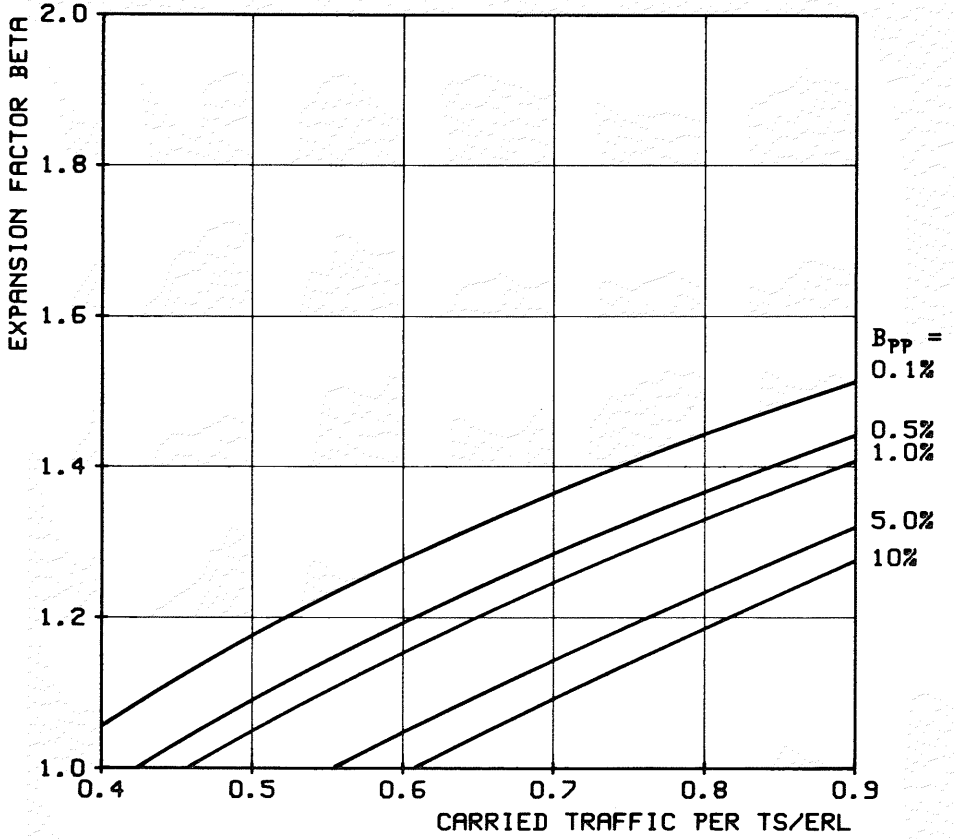


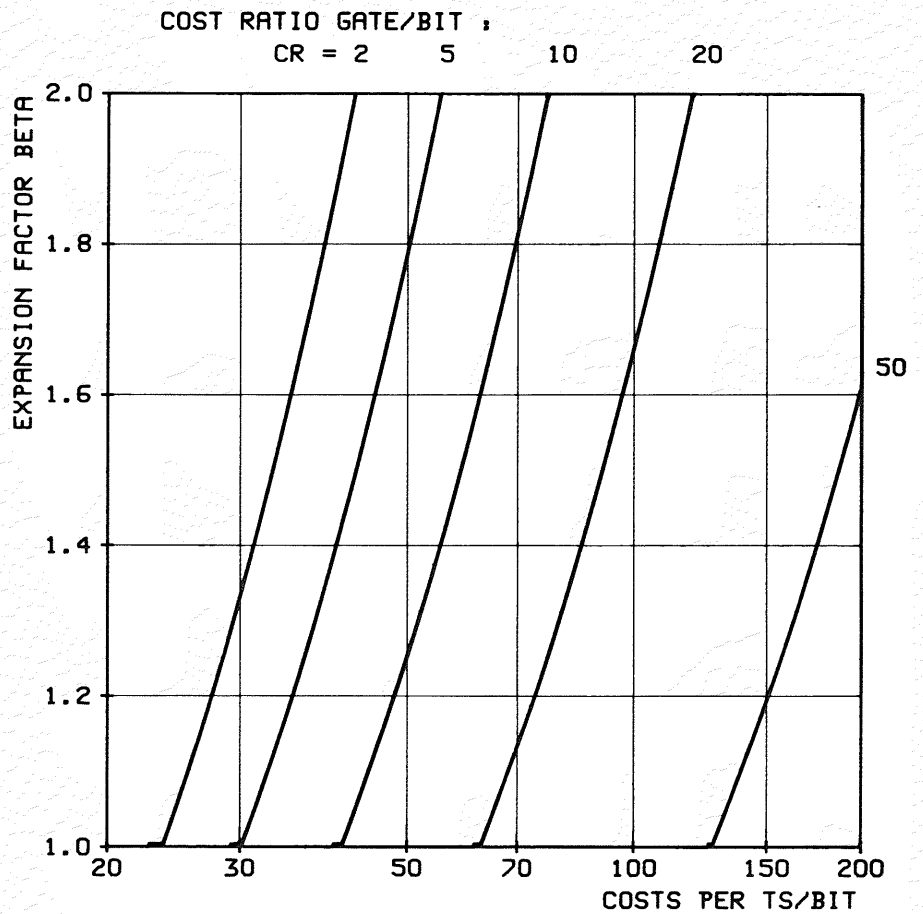
COMBINED SWITCHING 1 × 196 HW H_1 = 14
SEPARATED SWITCHING 2 × 196 HW M = 30

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

-CHART 51-

SSTSS

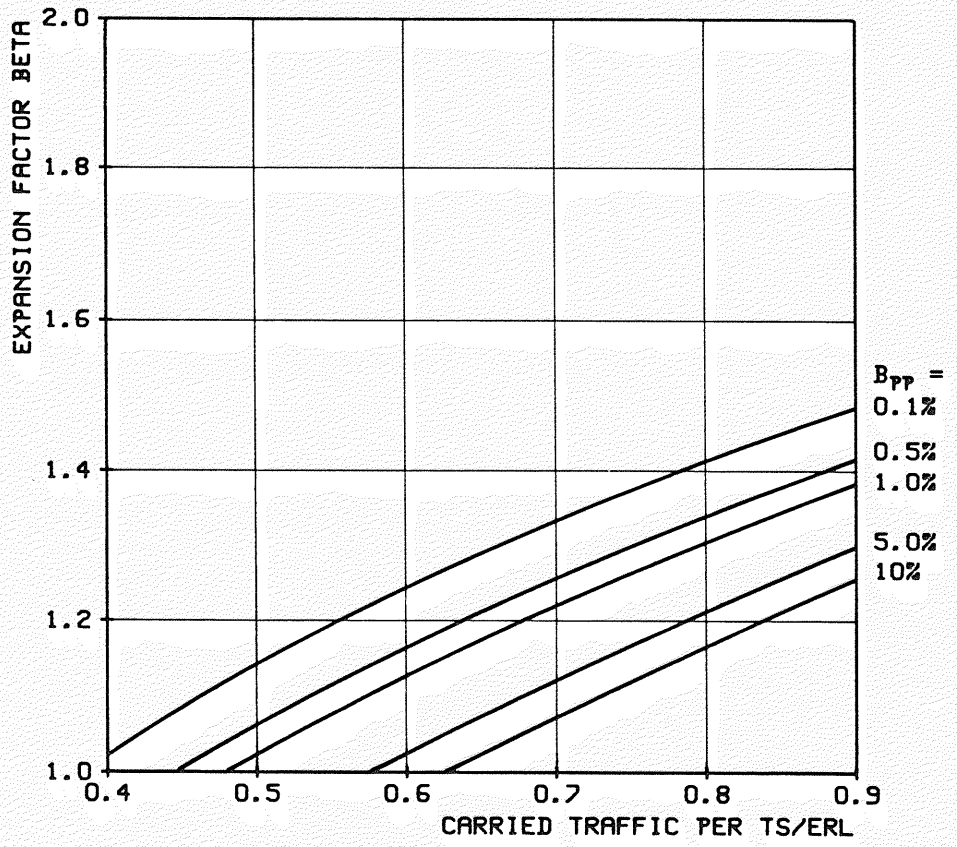


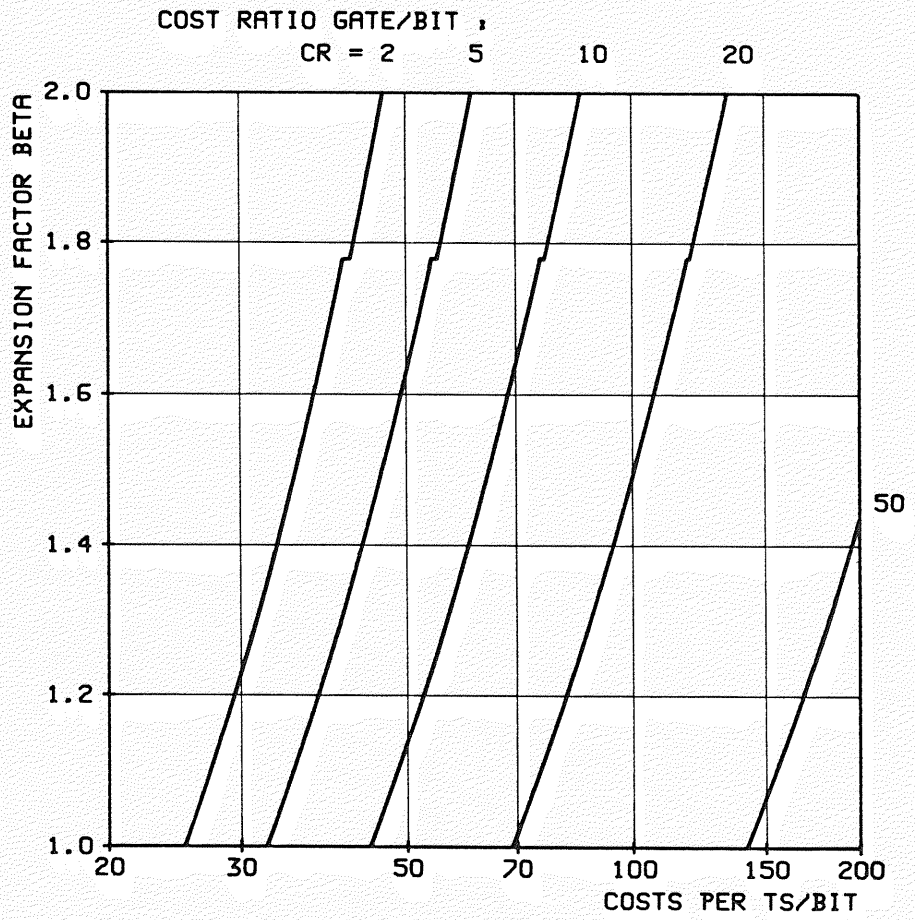


COMBINED SWITCHING 1 × 256 HW H_1 = 16
SEPARATED SWITCHING 2 × 256 HW M = 30

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

SSTSS



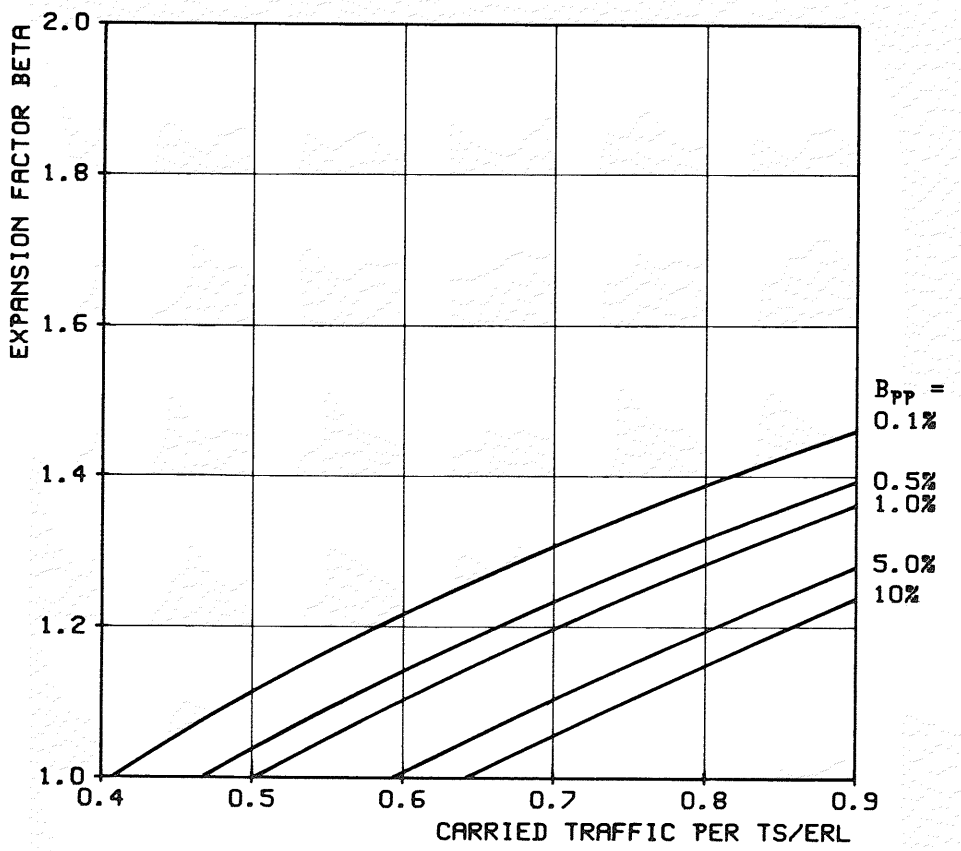


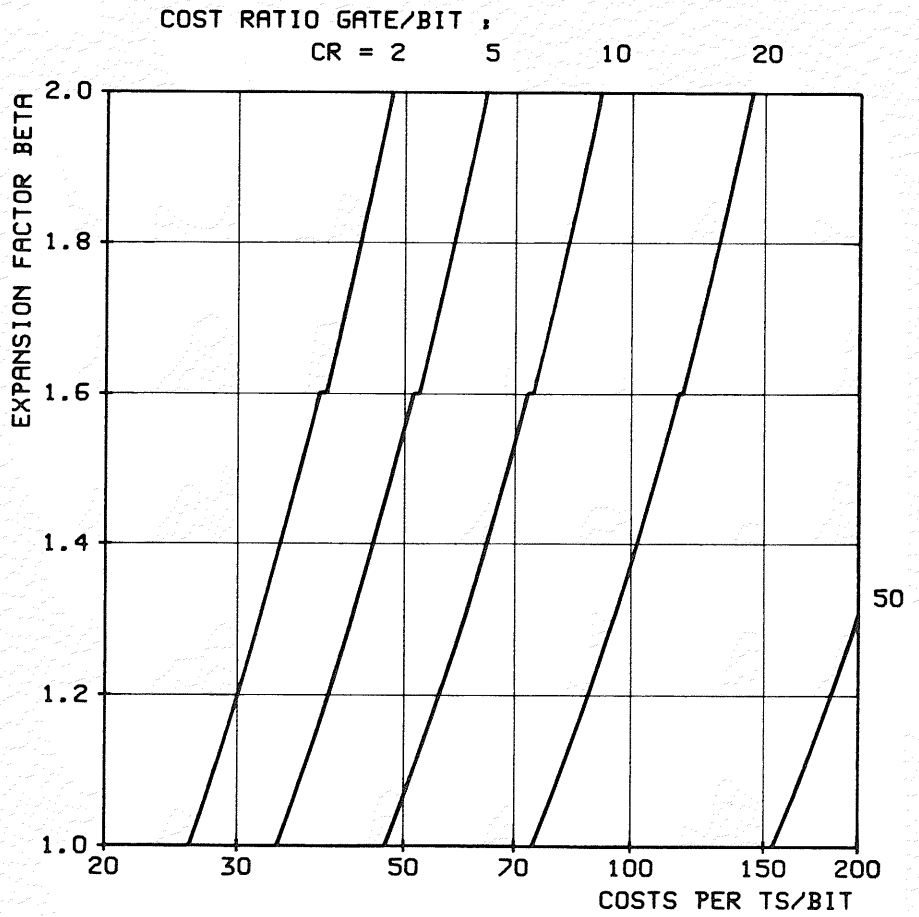
COMBINED SWITCHING 1 × 324 HW H_1 = 18
SEPARATED SWITCHING 2 × 324 HW M = 30

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

-CHART 53-

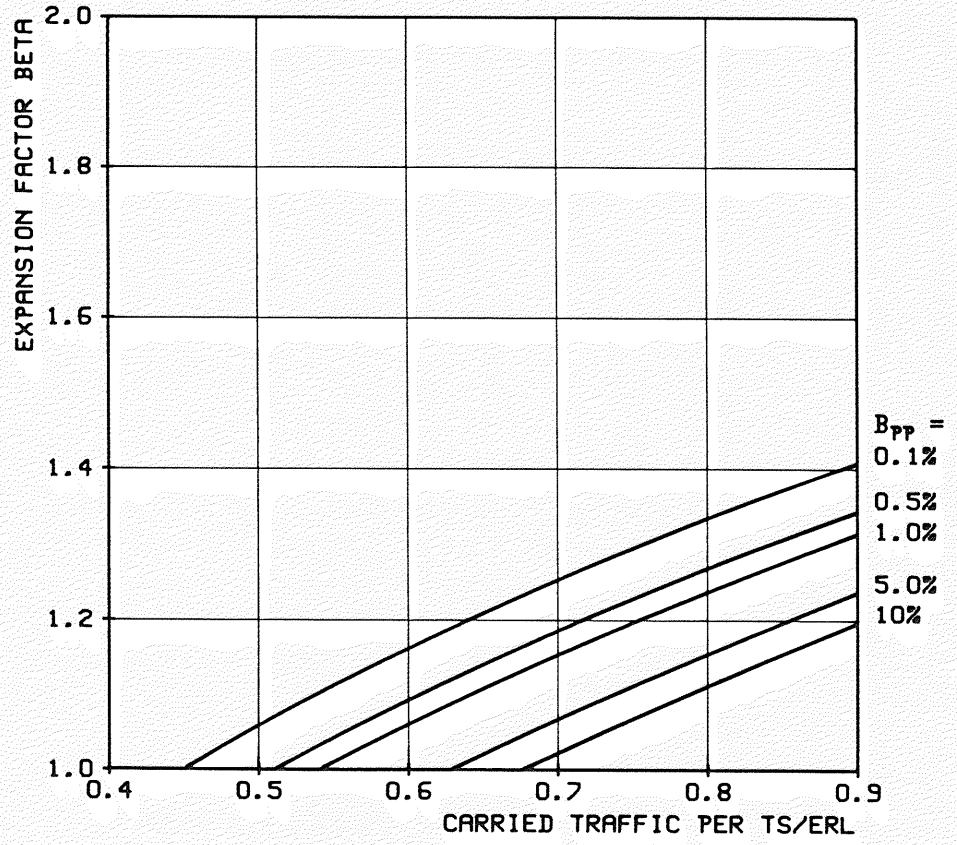
SSTSS

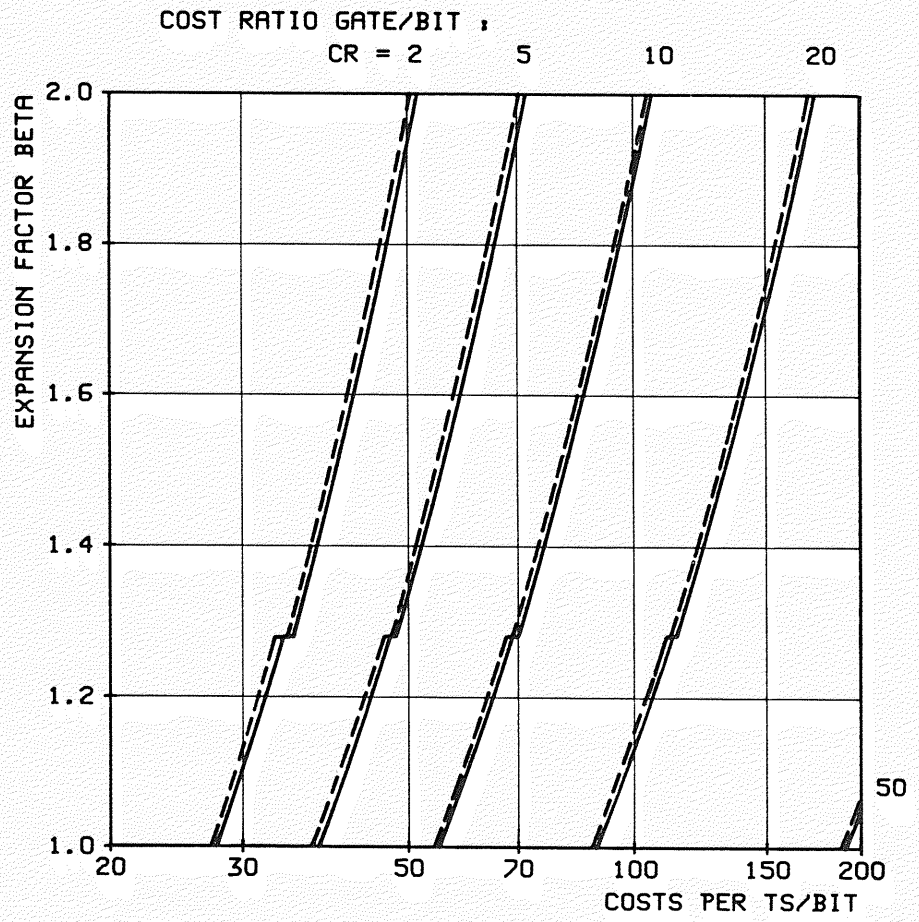




COMBINED SWITCHING	1 × 400 HW	H_1 = 20	—— { COMBINED SWITCHING
SEPARATED SWITCHING	2 × 400 HW	M = 30	{ SEPARATED SWITCHING

SSTSS





COMBINED SWITCHING 1 × 625 HW H_1 = 25

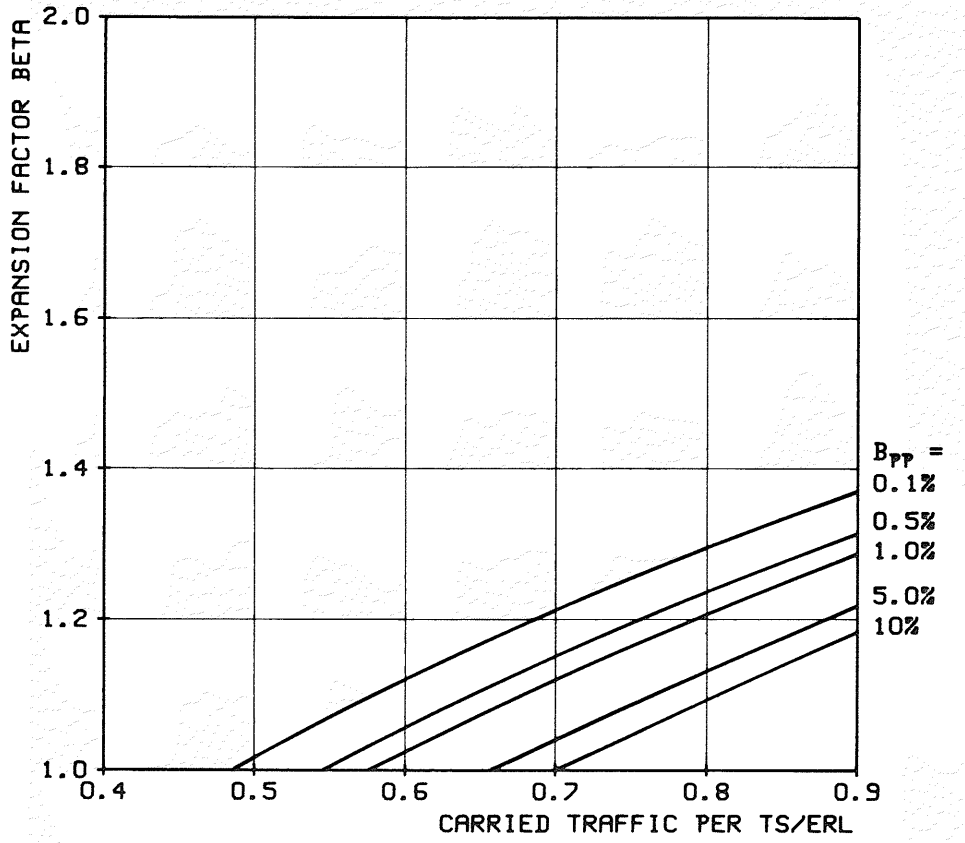
SEPARATED SWITCHING 2 × 625 HW M = 30

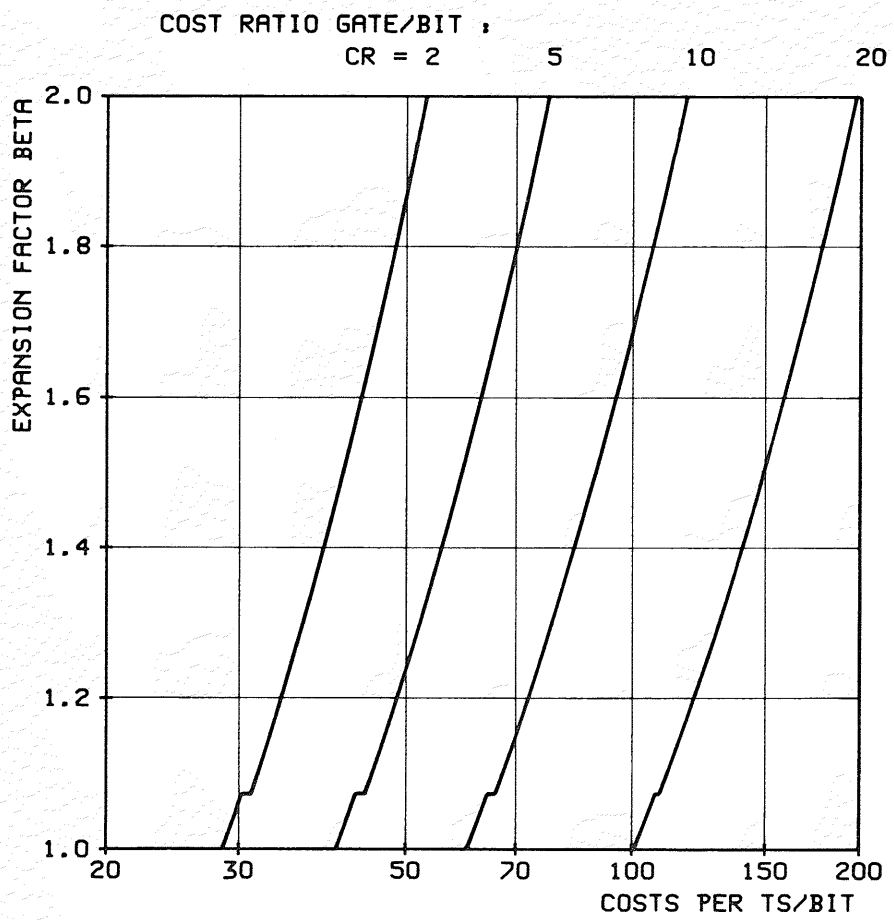
—— COMBINED SWITCHING

--- SEPARATED SWITCHING

-CHART 55-

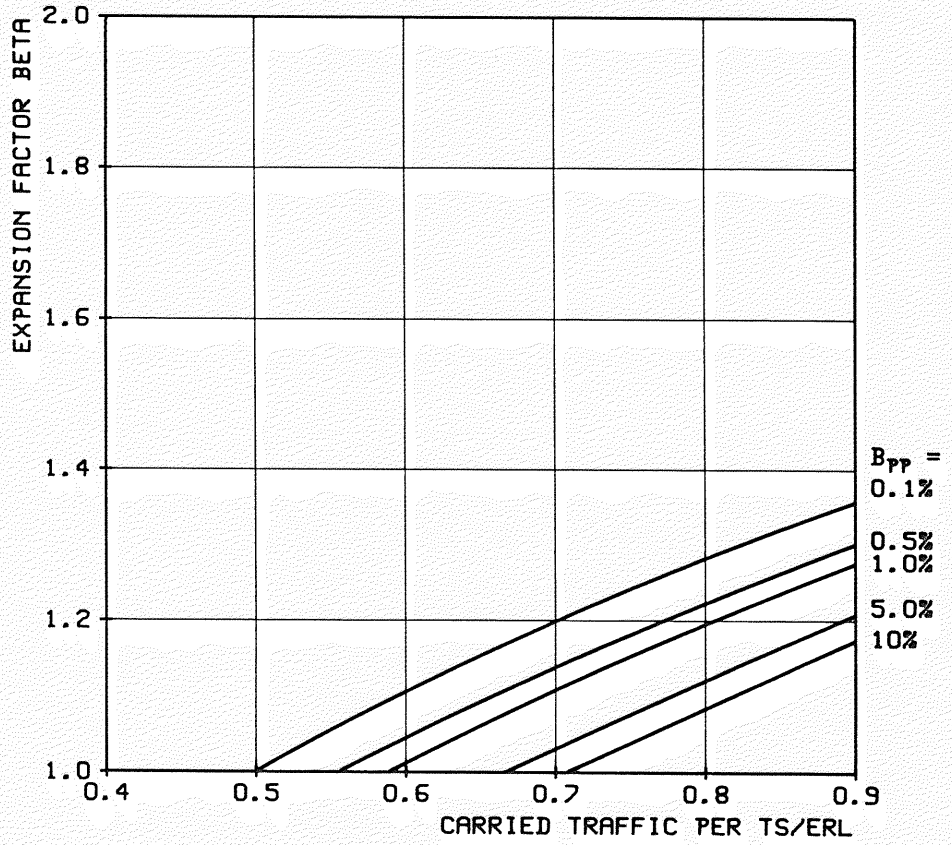
SSTSS

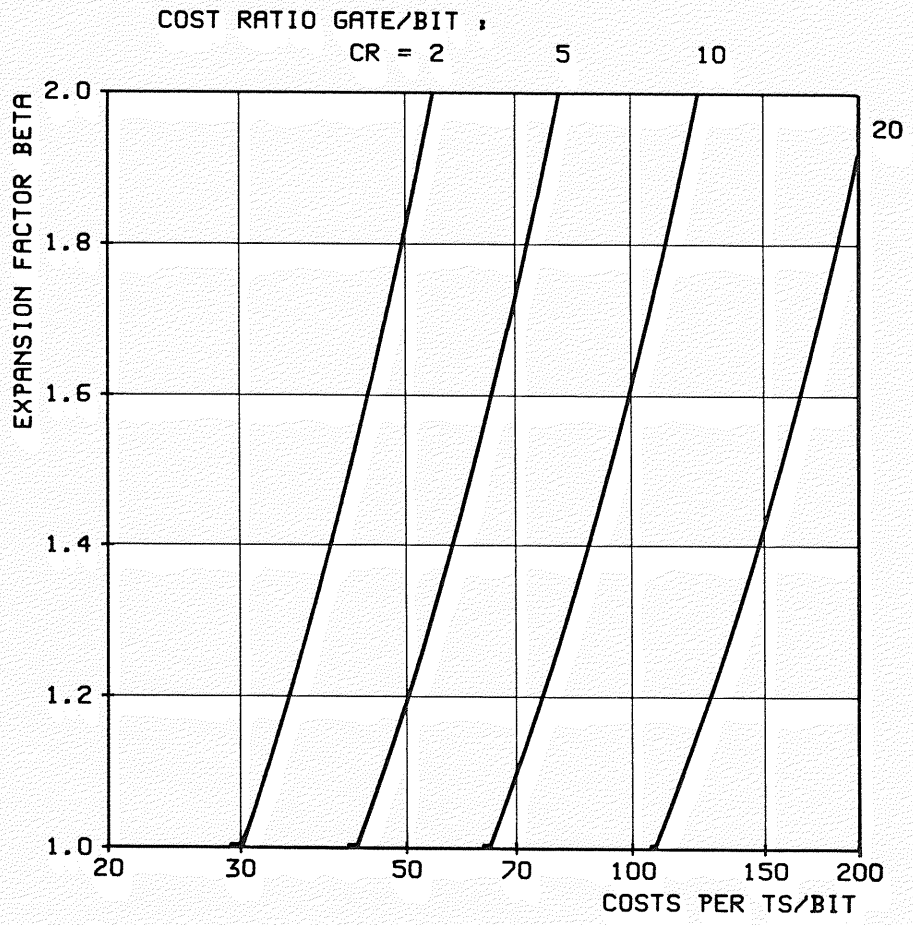




COMBINED SWITCHING	1 × 900 HW	H_1 = 30	—— { COMBINED SWITCHING
SEPARATED SWITCHING	2 × 900 HW	M = 30	{ SEPARATED SWITCHING

SSTSS



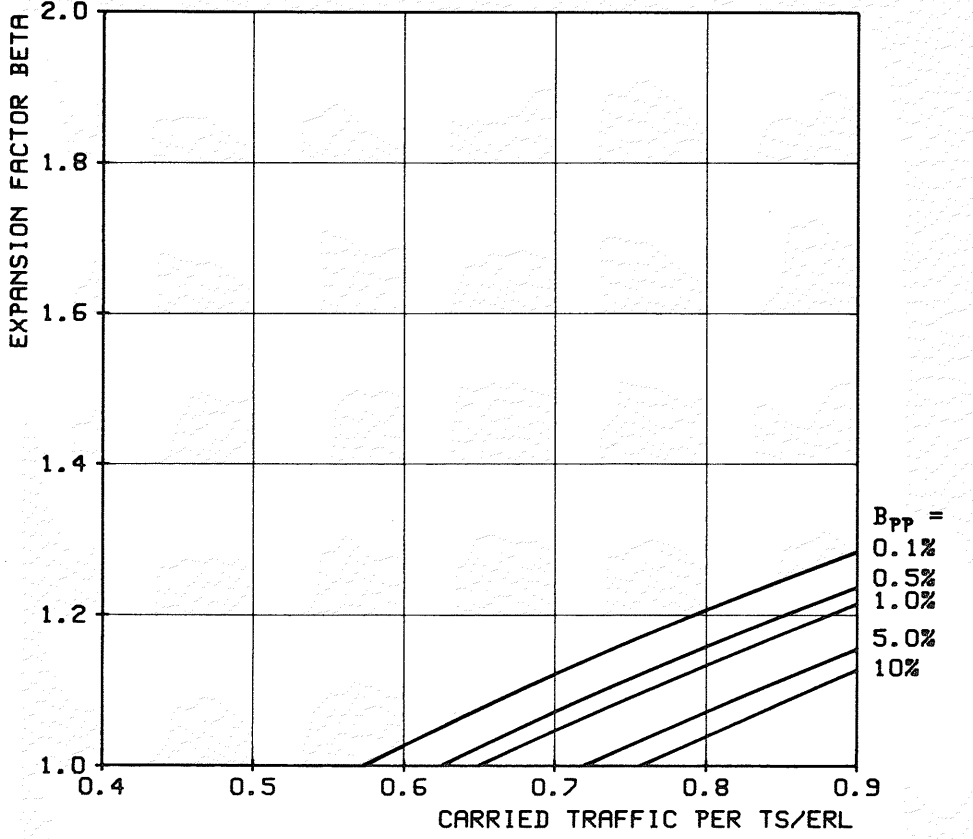


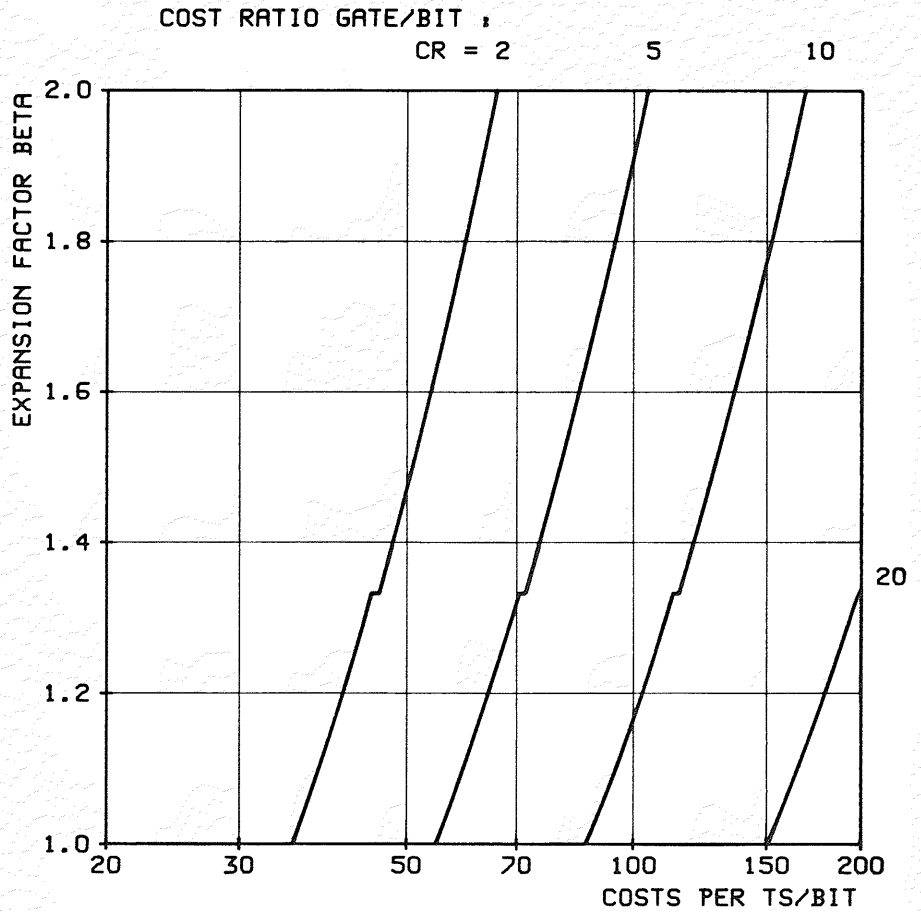
COMBINED SWITCHING 1 × 1024 HW H_1 = 32

SEPARATED SWITCHING 2 × 1024 HW M = 30

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

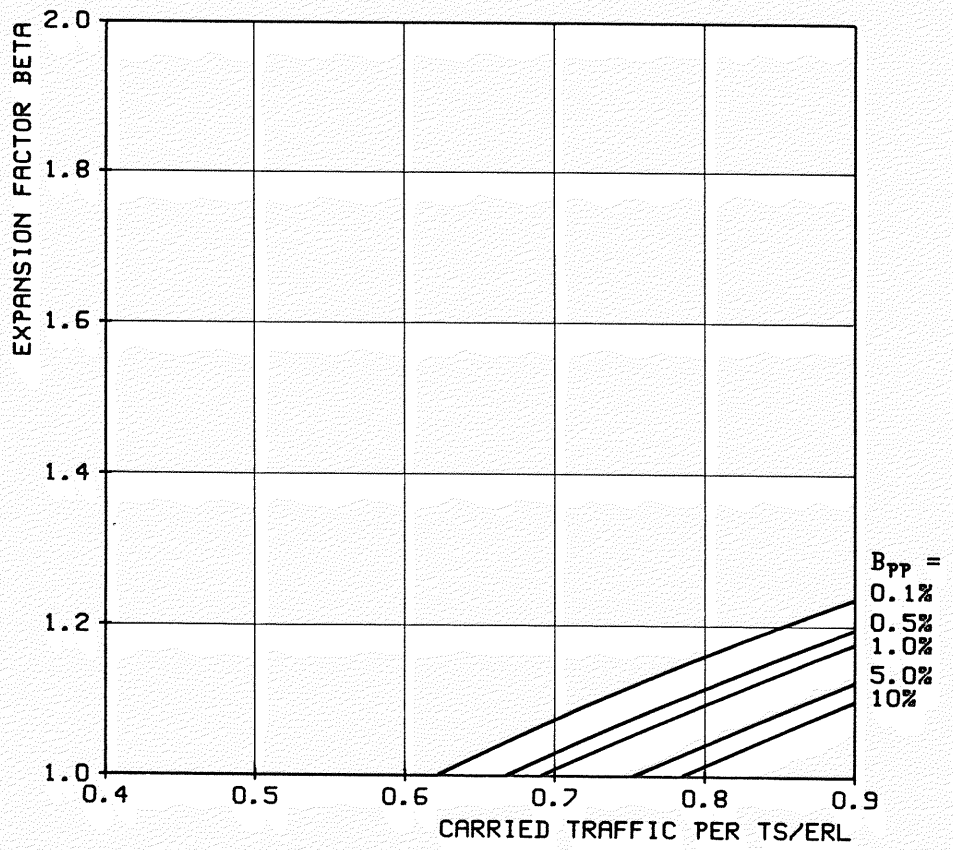
SSTSS

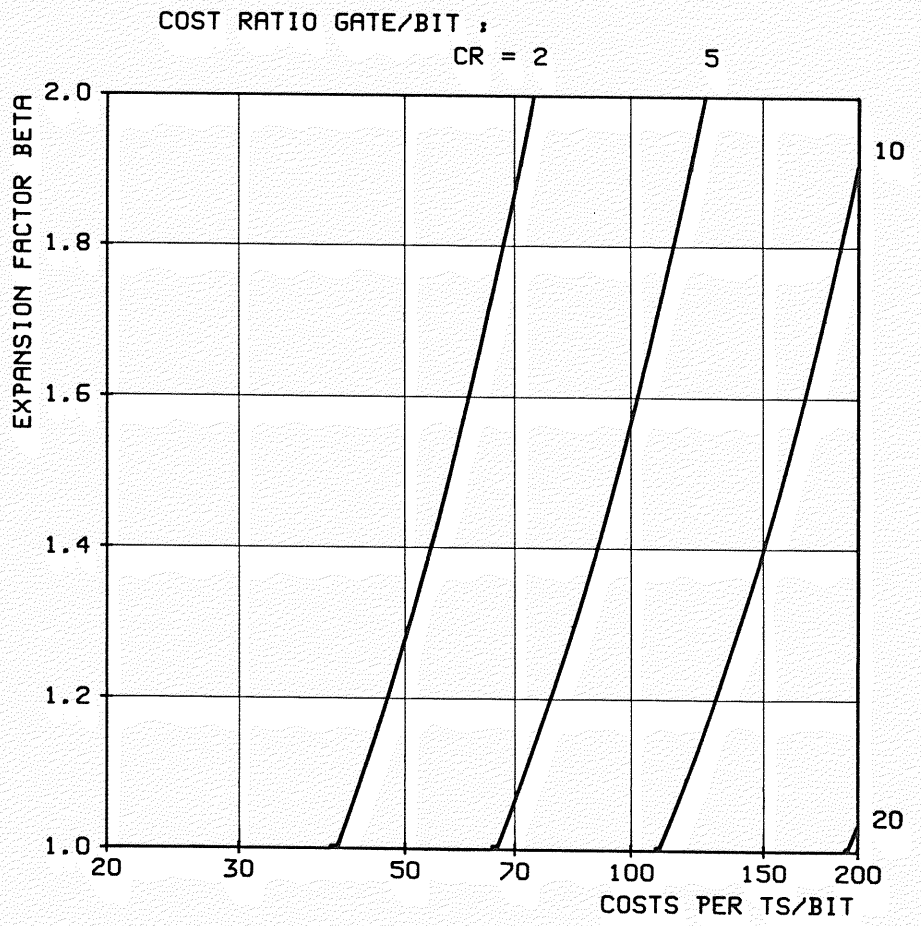




COMBINED SWITCHING	1 × 2304 HW	H_1 = 48	——{ COMBINED SWITCHING
SEPARATED SWITCHING	2 × 2304 HW	M = 30	{ SEPARATED SWITCHING

SSTSS





COMBINED SWITCHING	1 × 4096 HW	H_1 = 64	—— { COMBINED SWITCHING
SEPARATED SWITCHING	2 × 4096 HW	M = 30	{ SEPARATED SWITCHING

PCM SWITCHING ARRAY : TSSSST

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 64, 125, 216, 343, 512, 729, 1000, 1331, 1728, 2197, 2744, 3375, 4096,

SEPARATED SWITCHING : HW = 128, 250, 432, 686, 1024, 1458, 2000, 2662, 3456, 4394, 5488, 6750, 8192,

TIME-SLOTS (TS) PER HW : M = 30 TS

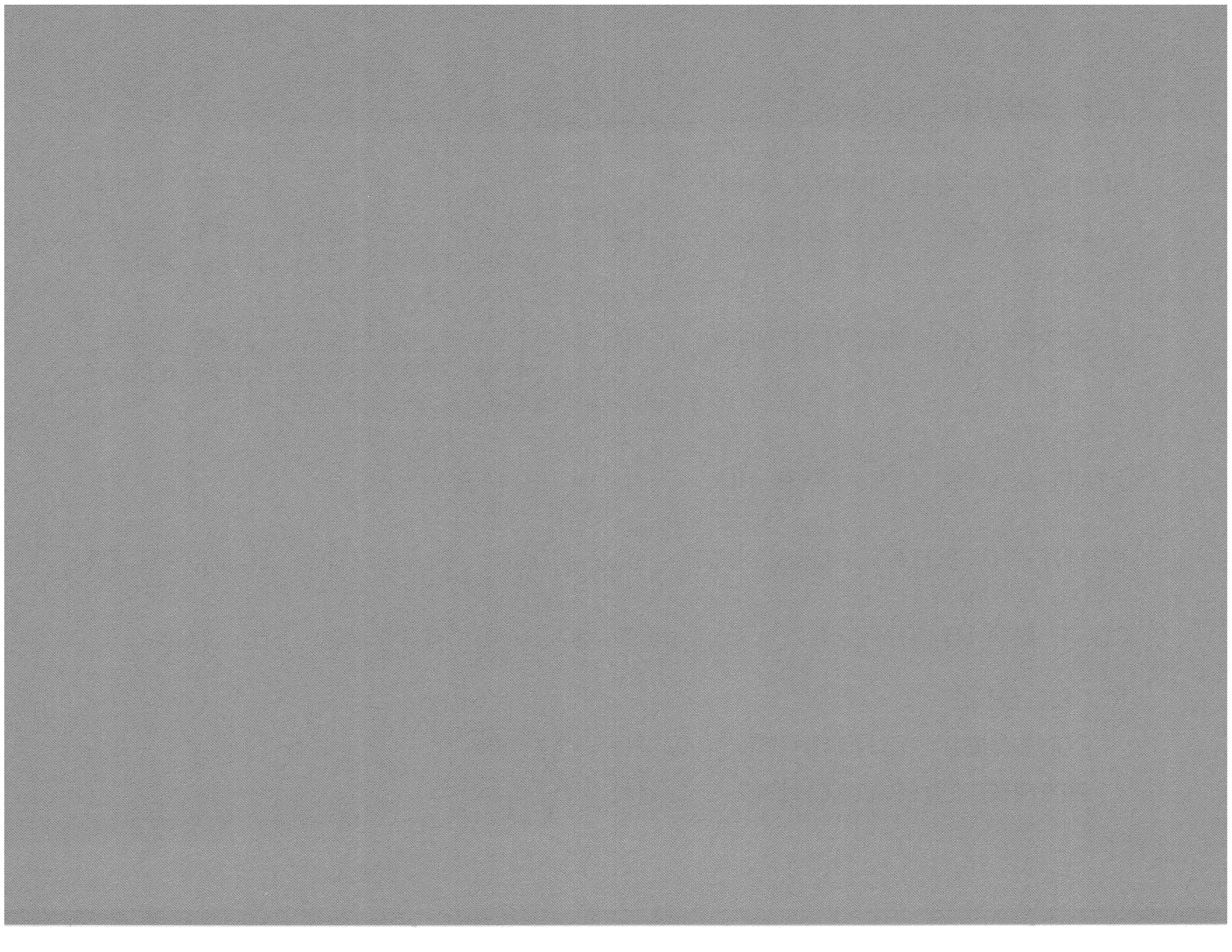
POINT-TO-POINT LOSS, PCT1 : B_{PP} = 0.1, 0.5, 1.0, 5.0, 10.0%

COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

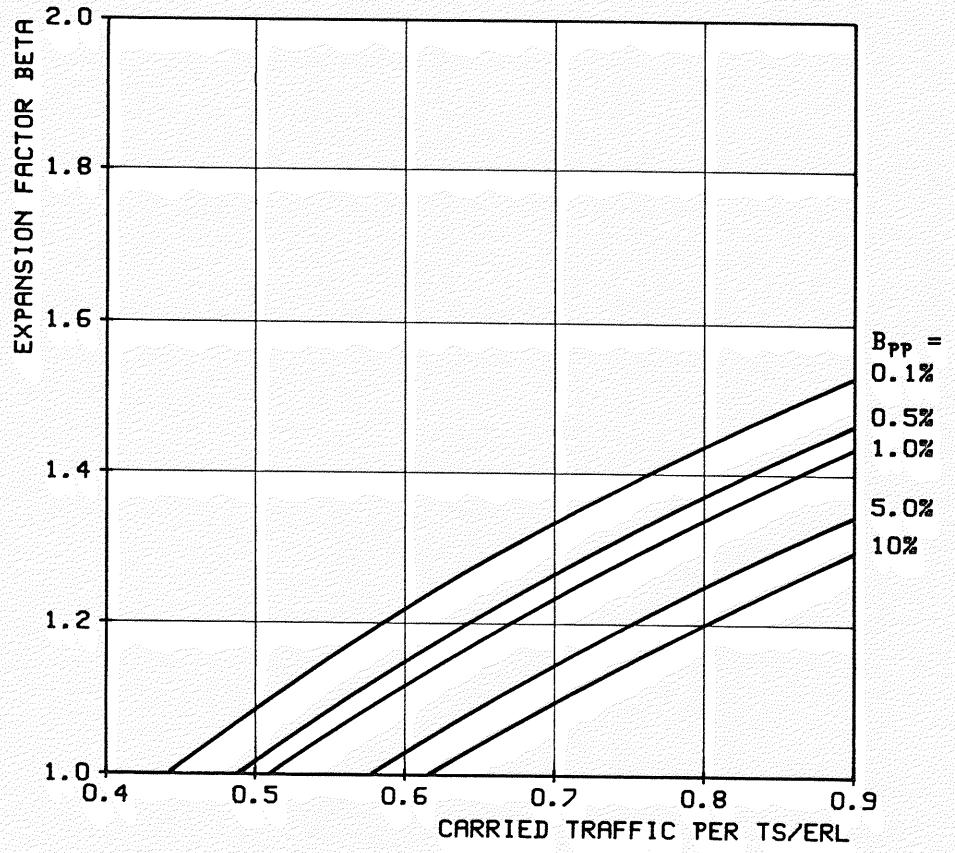
BLOCK SIZE

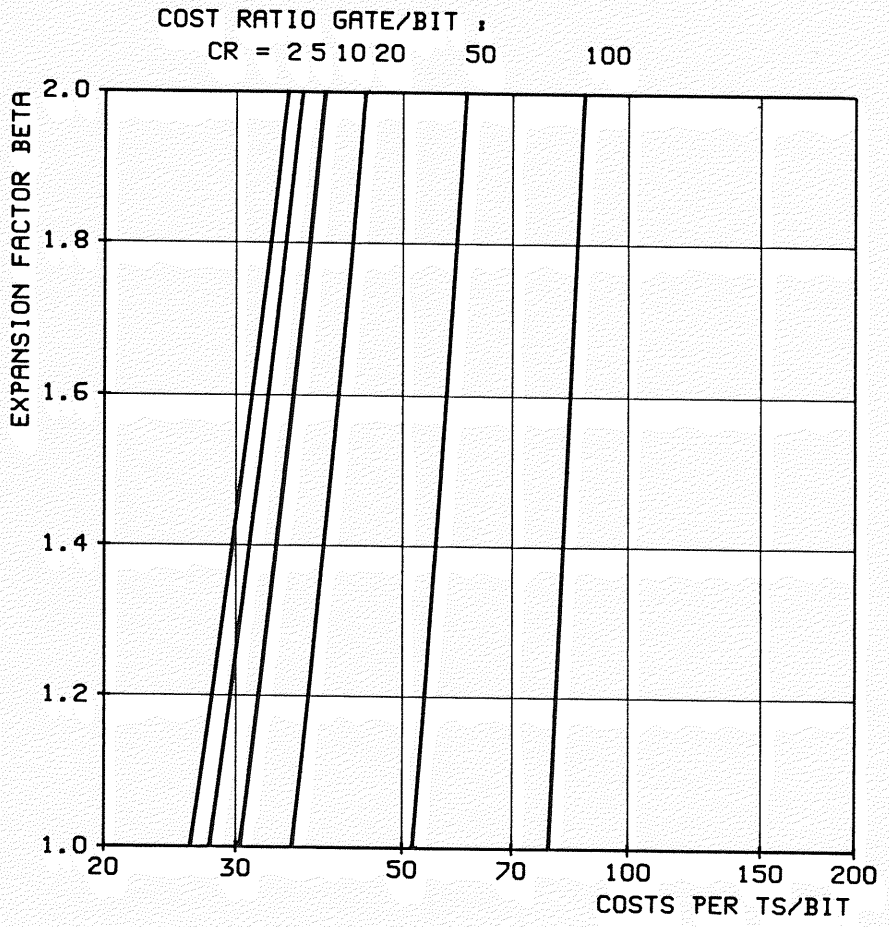
COMBINED SWITCHING : $H_2 = \sqrt[3]{HW}$

SEPARATED SWITCHING : $H_2 = \sqrt[3]{HW/2}$



TSSSST



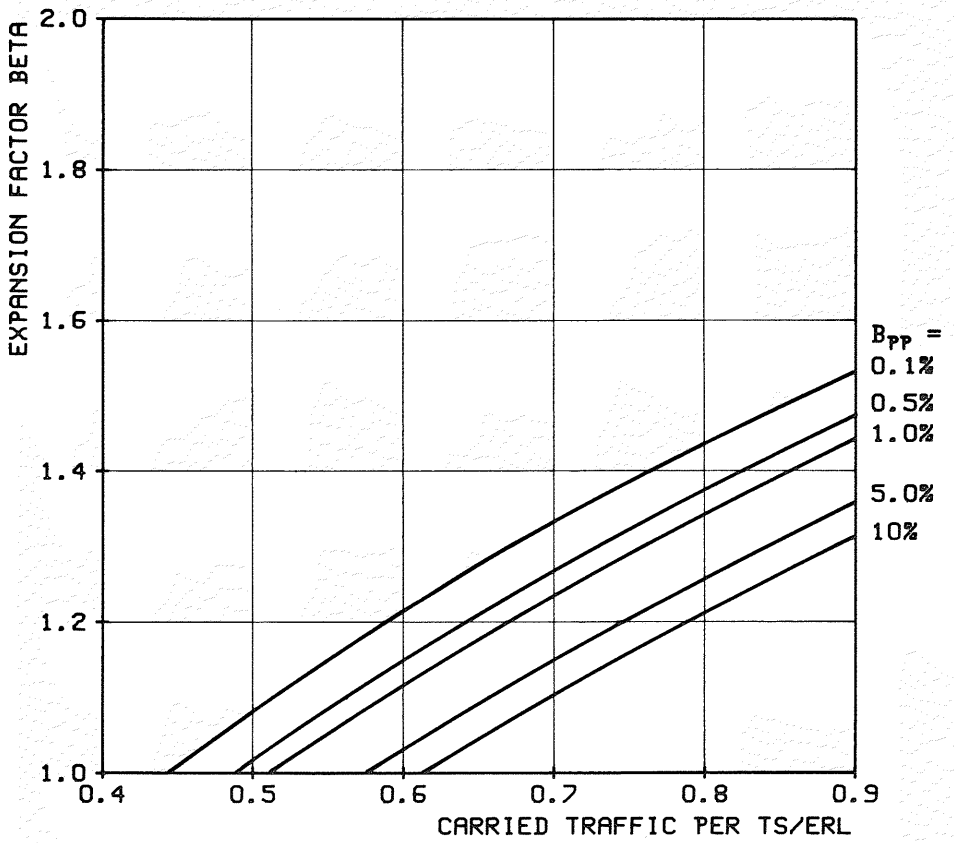


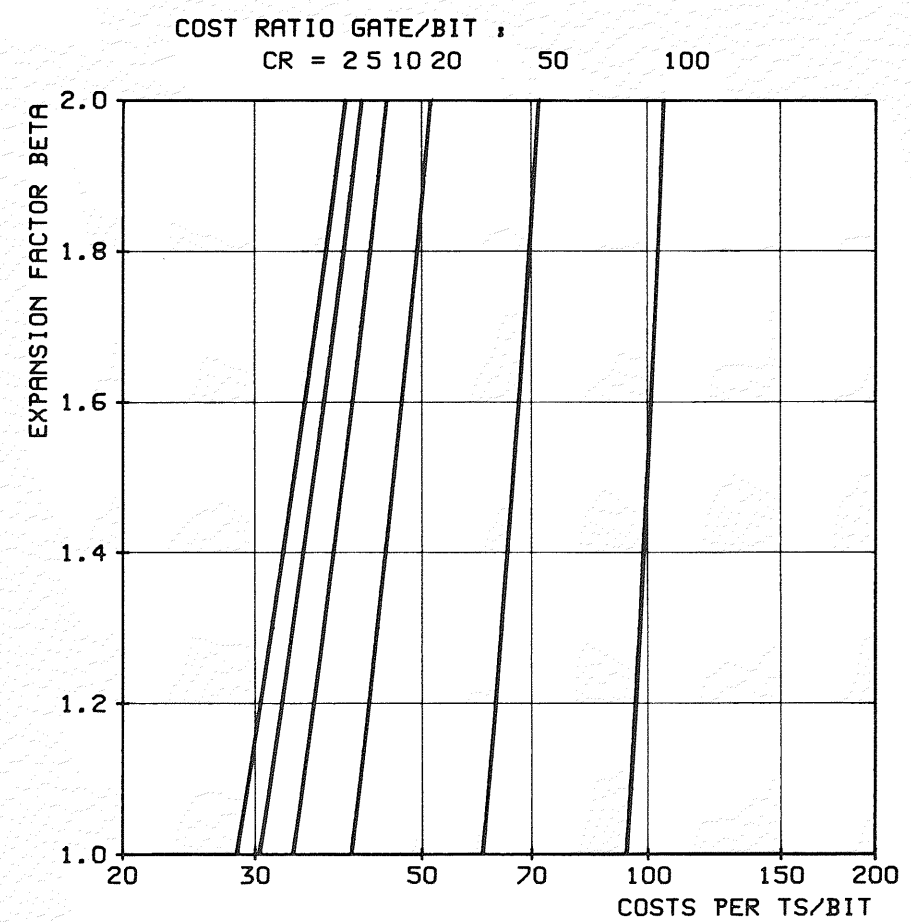
COMBINED SWITCHING 1 × 64 HW H_2 = 4
SEPARATED SWITCHING 2 × 64 HW M = 30

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

-CHART 60-

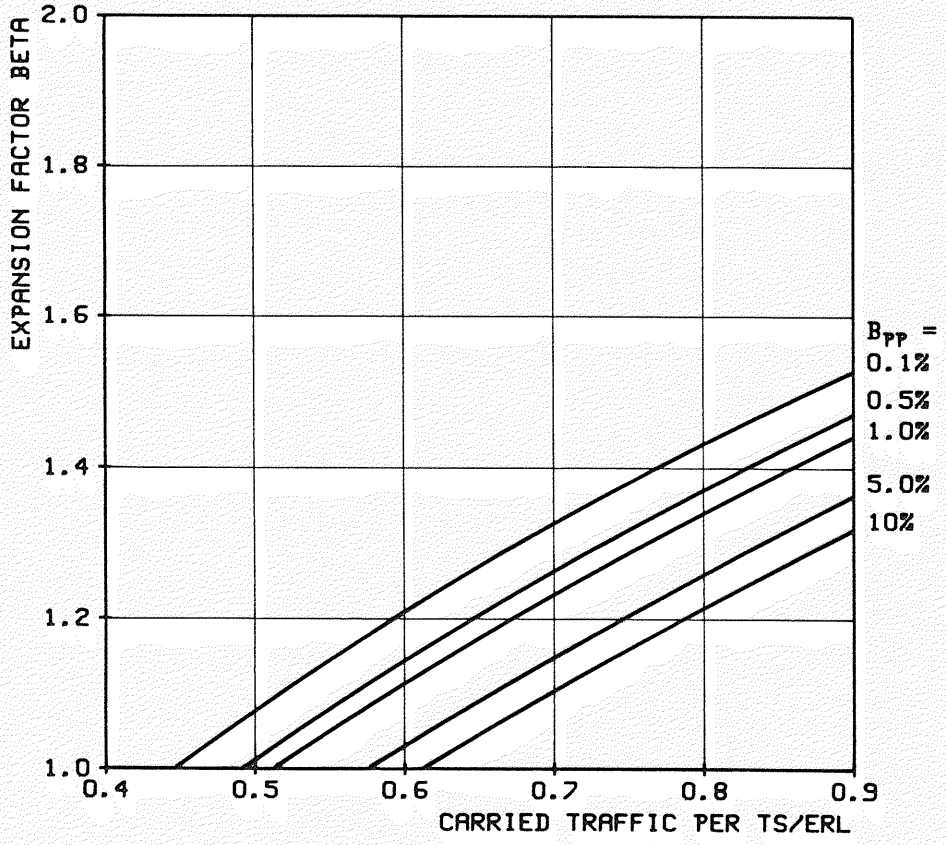
TSSSST

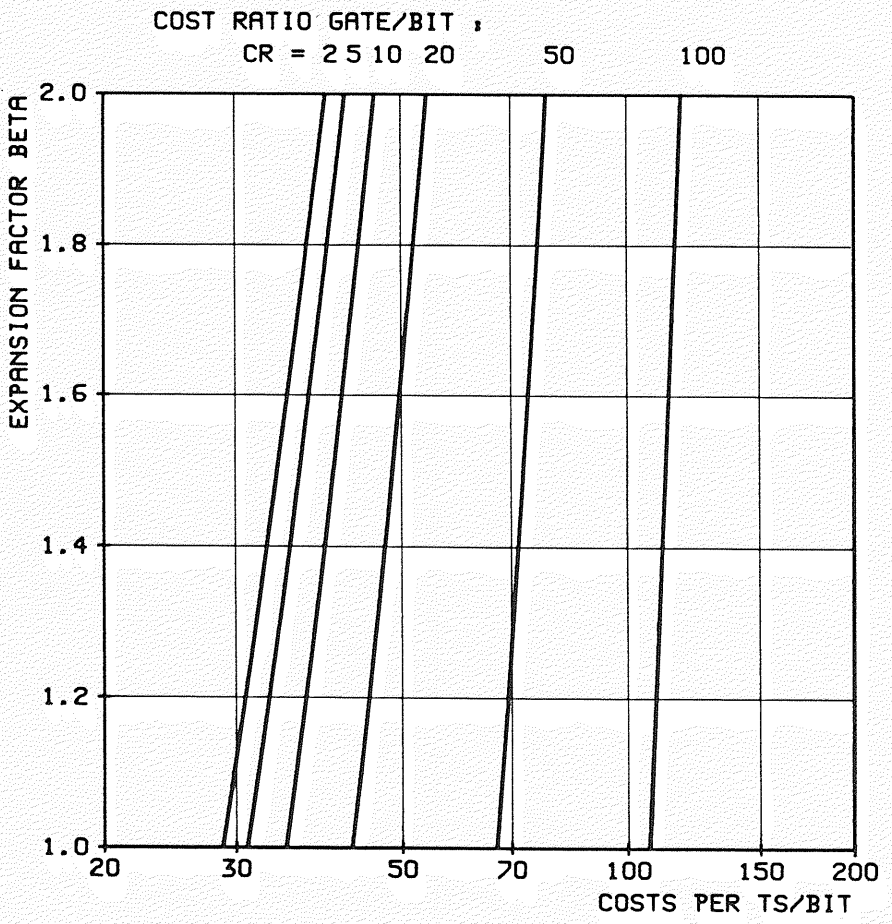




COMBINED SWITCHING	1 × 125 HW	H_2 = 5	—— { COMBINED SWITCHING
SEPARATED SWITCHING	2 × 125 HW	M = 30	{ SEPARATED SWITCHING

TSSSST

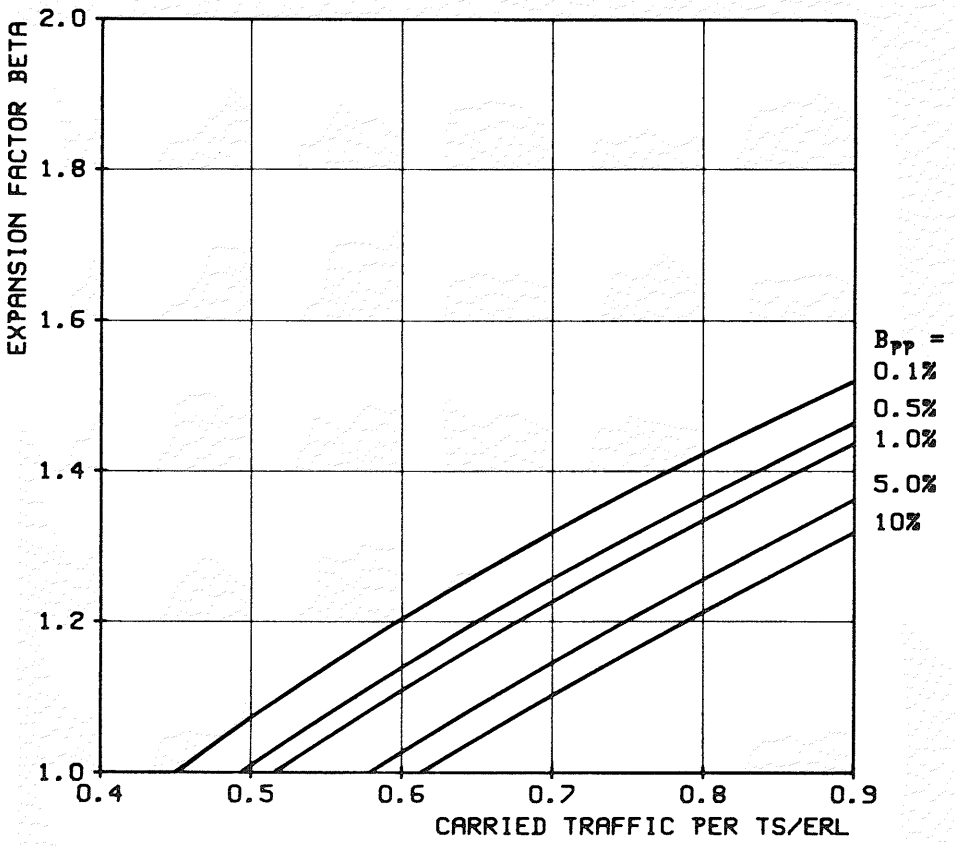


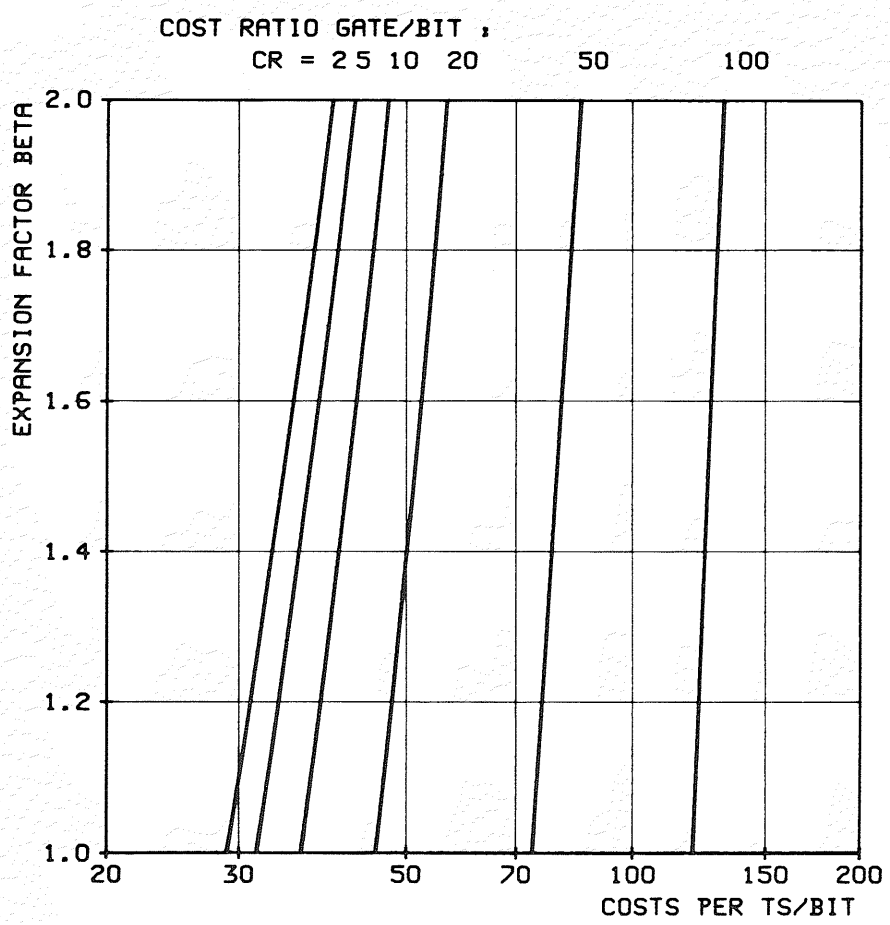


COMBINED SWITCHING 1 × 216 HW H_2 = 6
SEPARATED SWITCHING 2 × 216 HW M = 30

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

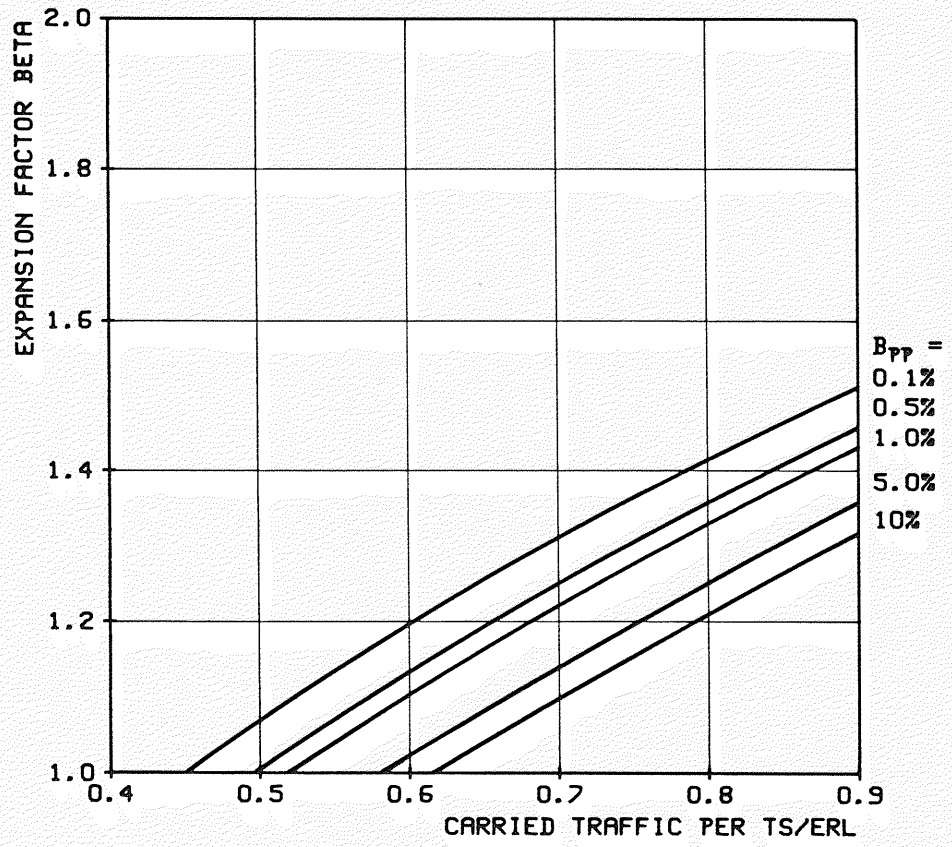
TSSSST

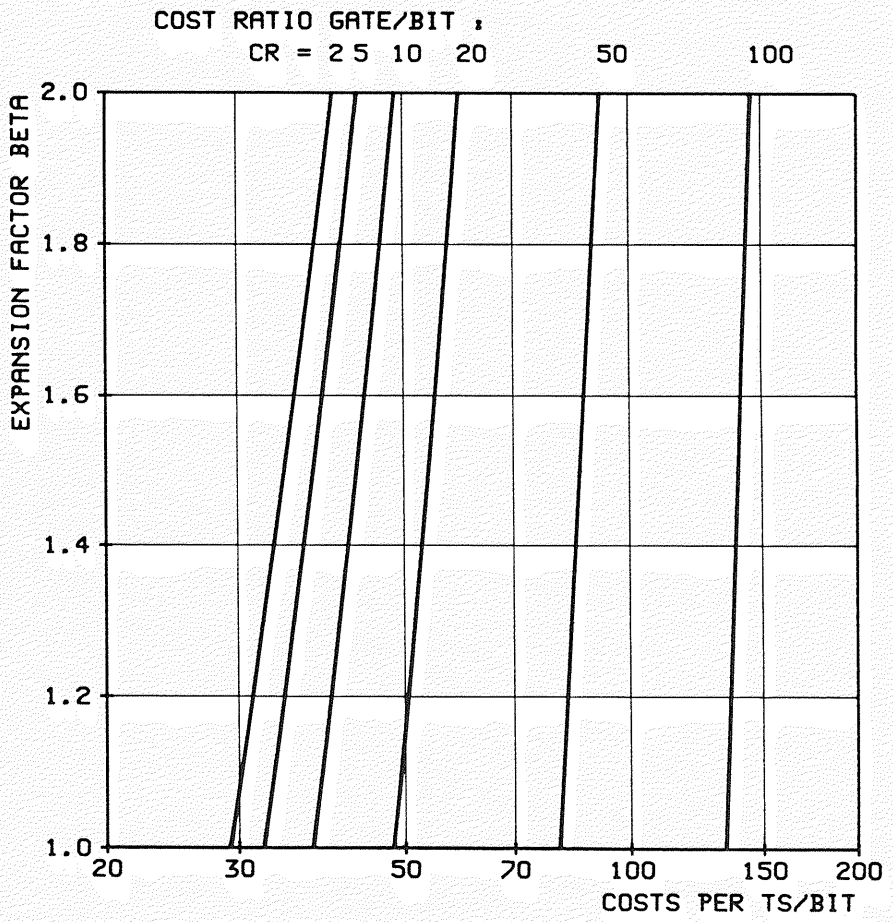




COMBINED SWITCHING	1 × 343 HW	H_2 = 7	——{ COMBINED SWITCHING
SEPARATED SWITCHING	2 × 343 HW	M = 30	{ SEPARATED SWITCHING

TSSSST



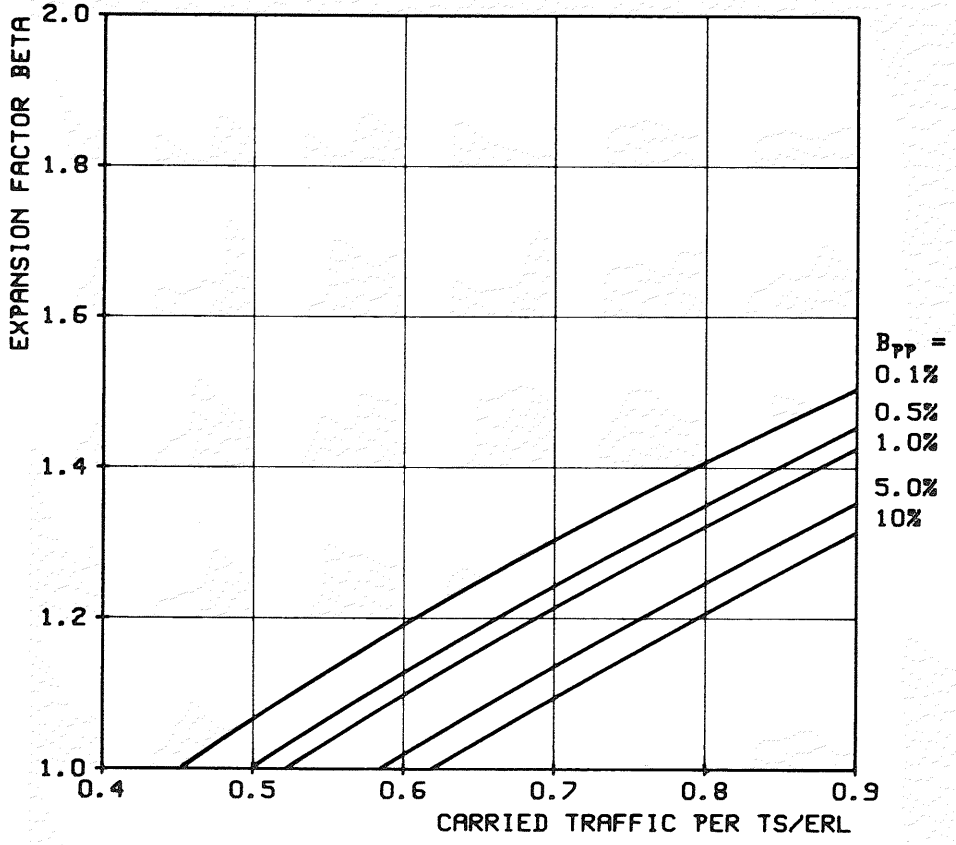


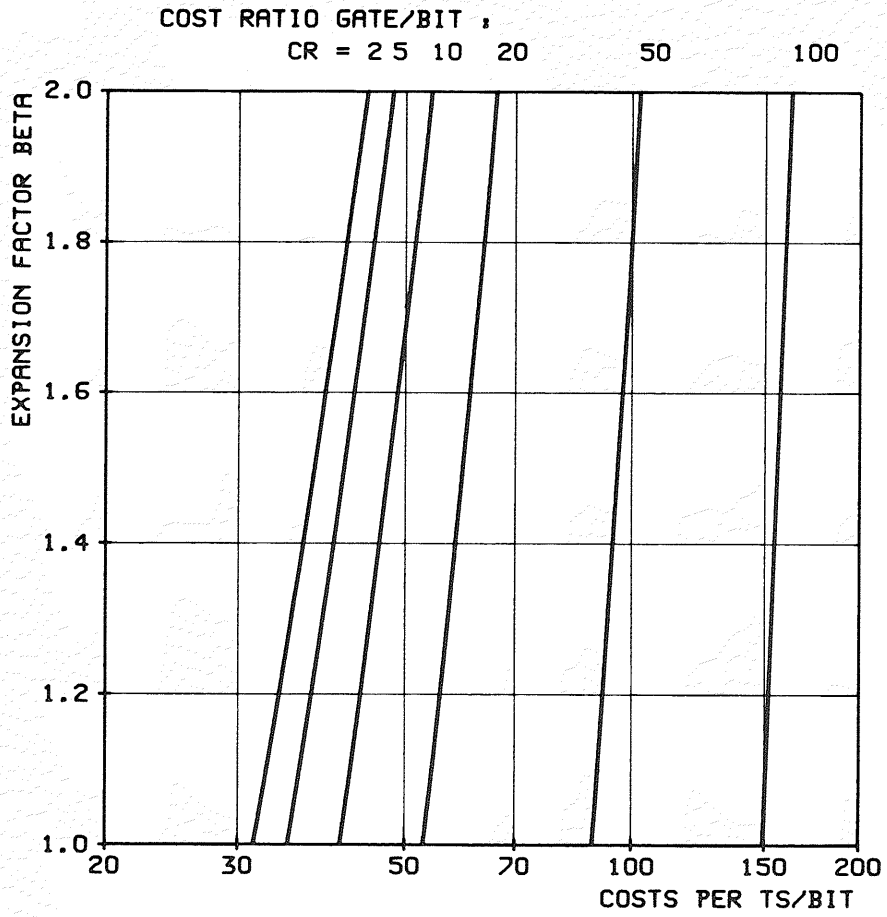
COMBINED SWITCHING 1 × 512 HW H_2 = 8
SEPARATED SWITCHING 2 × 512 HW M = 30

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

-CHART 64-

TSSSST



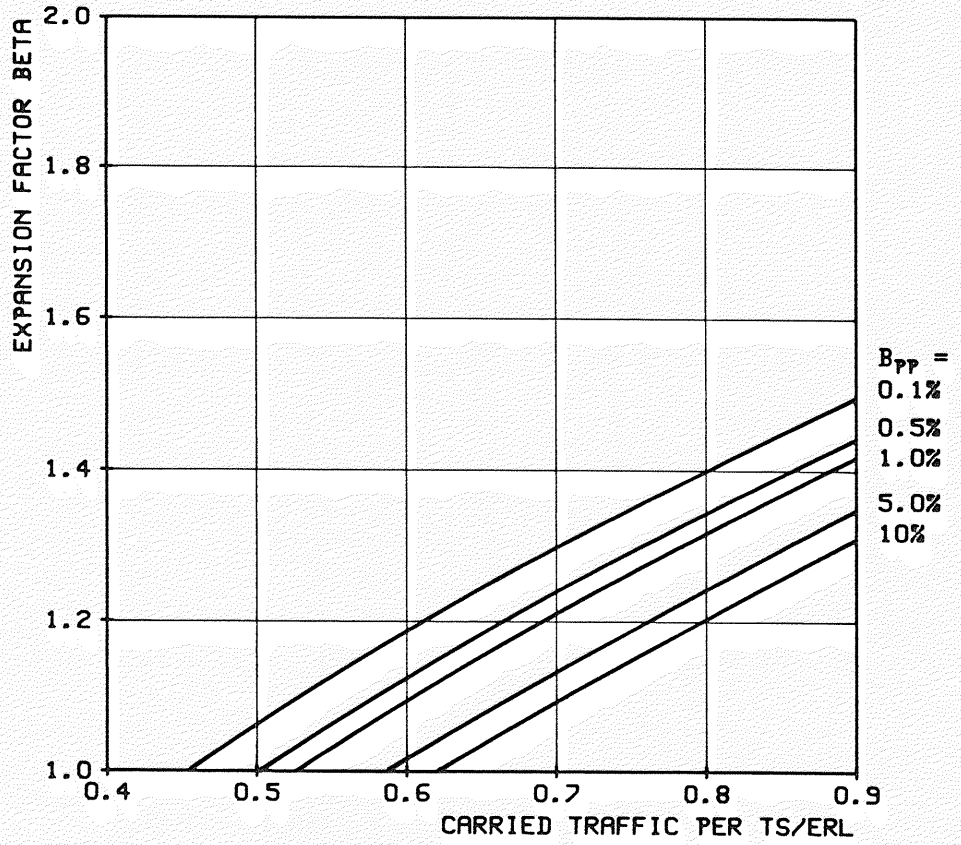


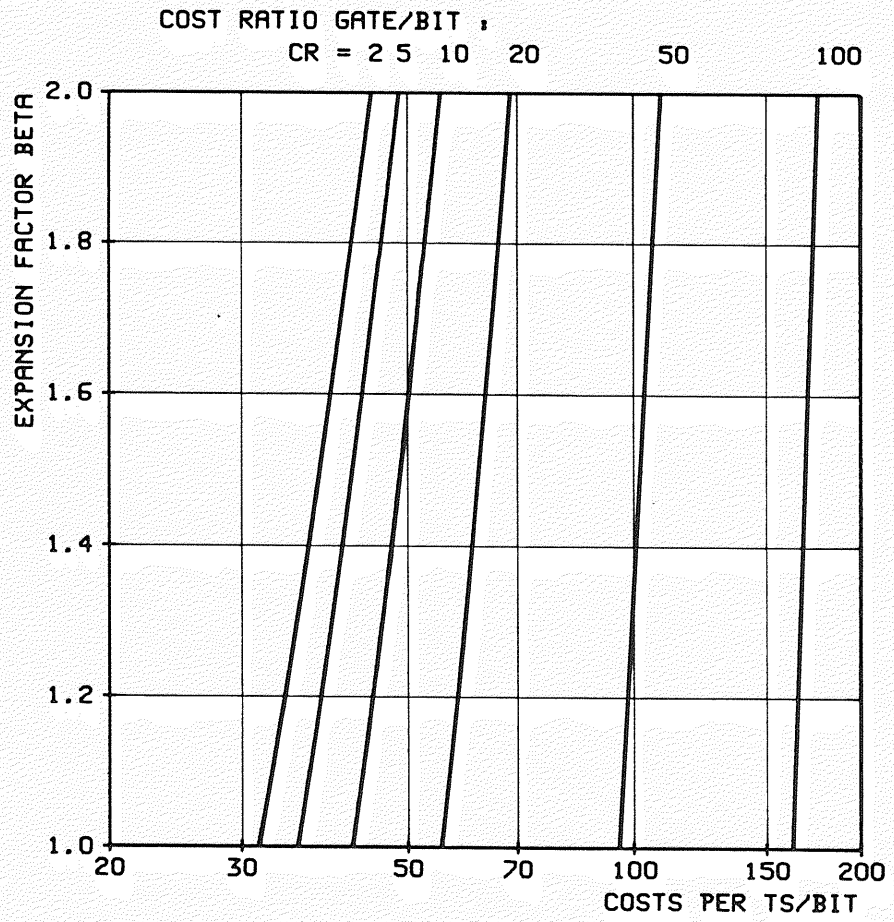
COMBINED SWITCHING 1 × 729 HW H_2 = 9

SEPARATED SWITCHING 2 × 729 HW M = 30

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

TSSSST



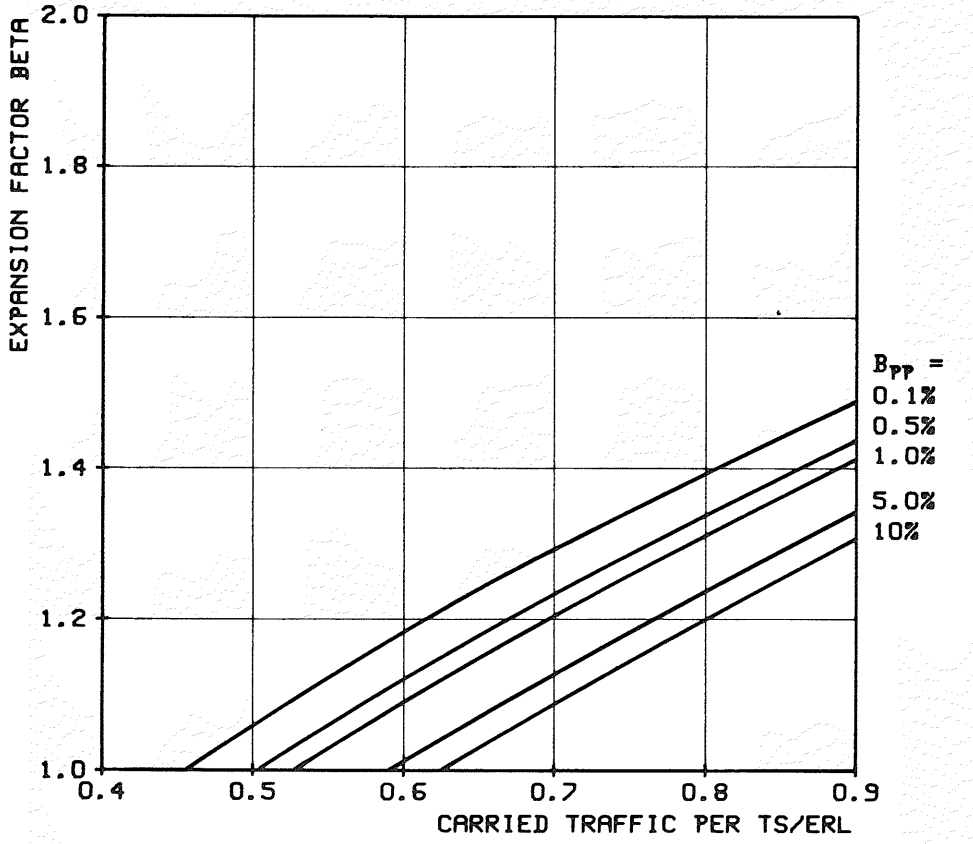


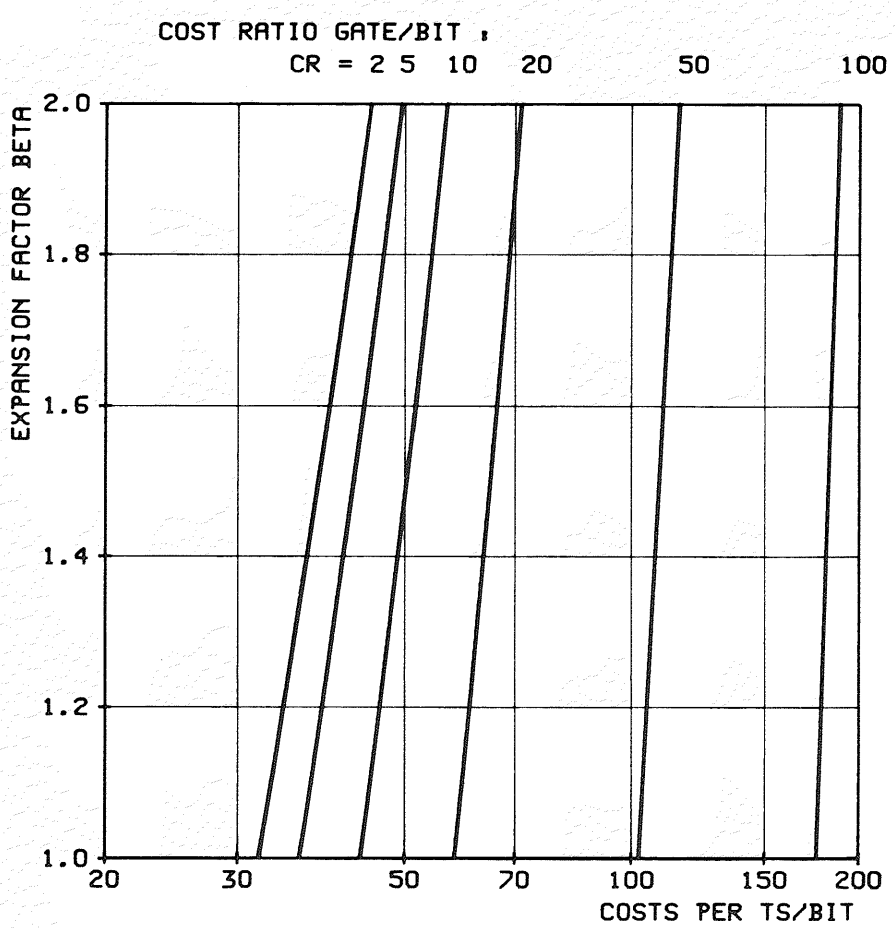
COMBINED SWITCHING 1 × 1000 HW H_2 = 10
SEPARATED SWITCHING 2 × 1000 HW M = 30

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

-CHART 66-

TSSSST

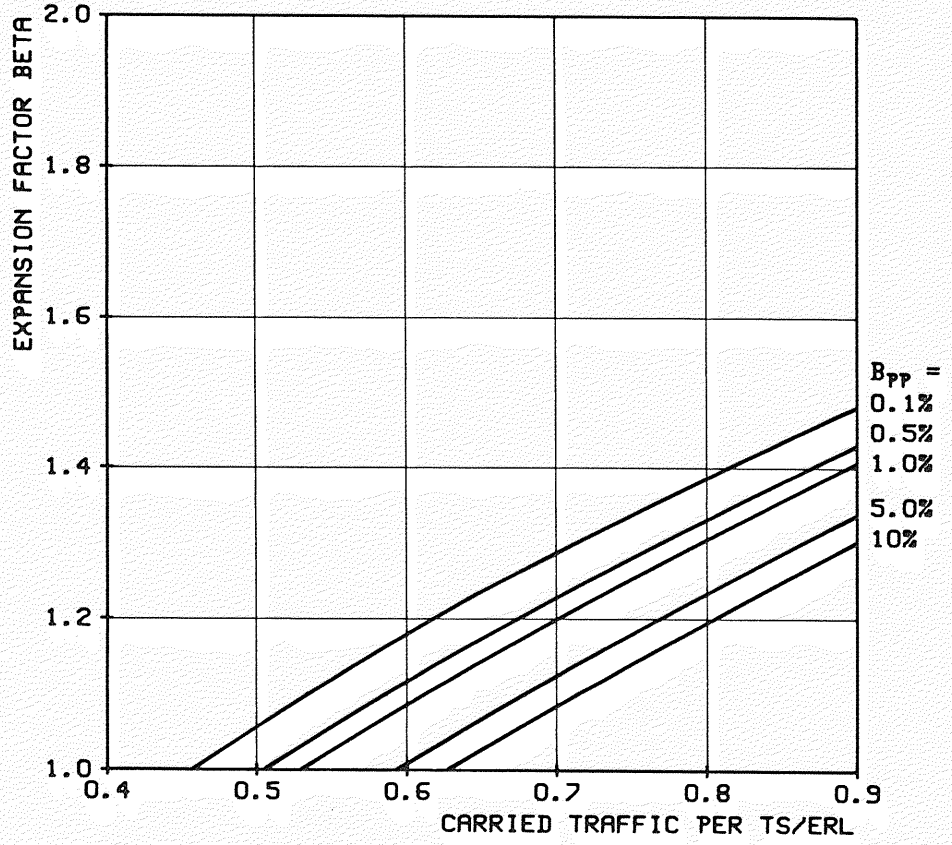


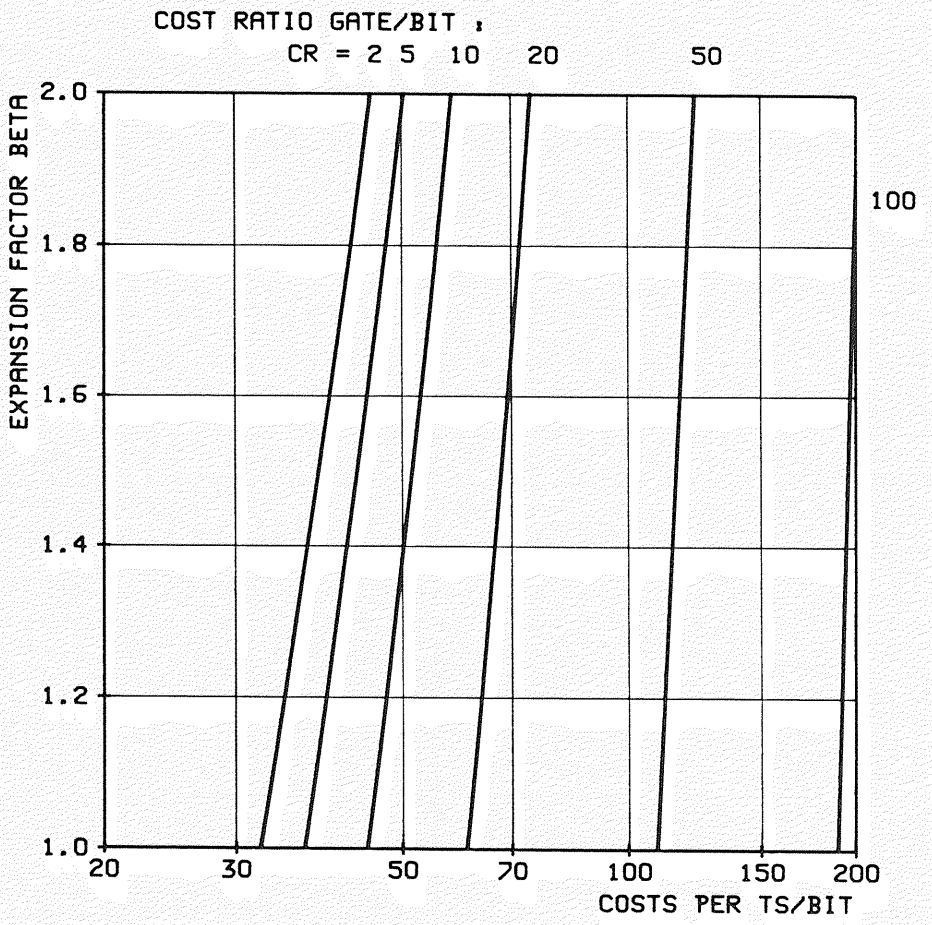


COMBINED SWITCHING 1 × 1331 HW H_2 = 11
SEPARATED SWITCHING 2 × 1331 HW M = 30

—— { COMBINED SWITCHING
SEPARATED SWITCHING

TSSSST

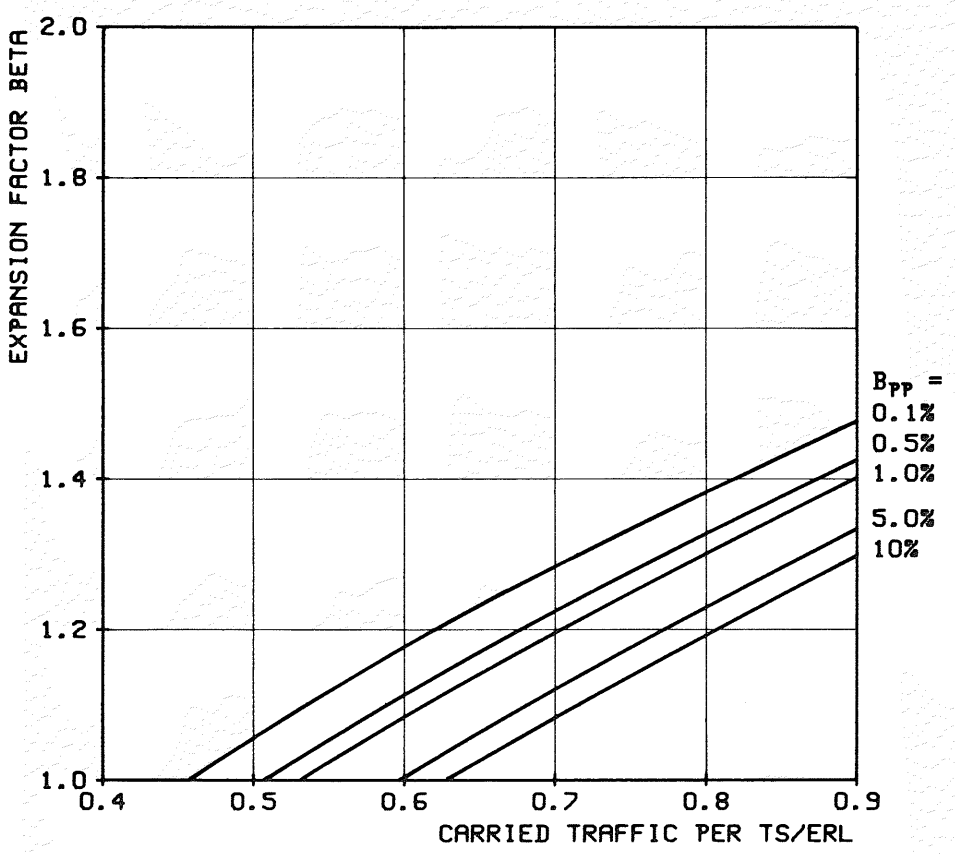


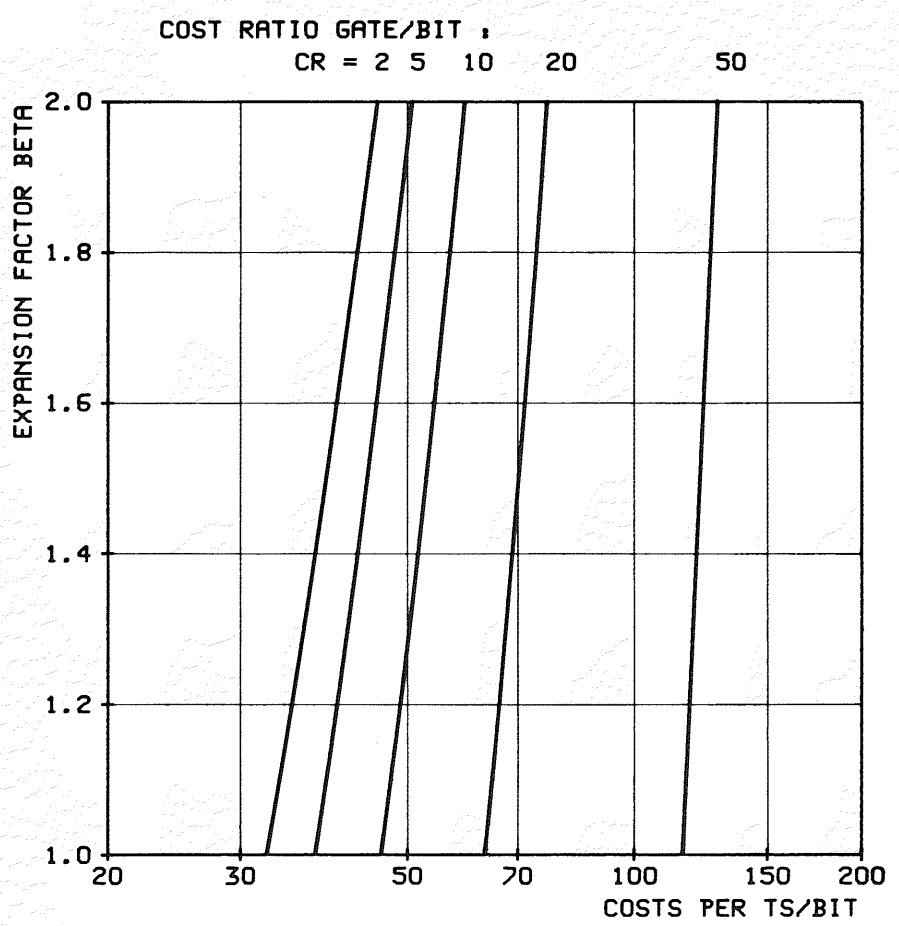


COMBINED SWITCHING 1 × 1728 HW H_2 = 12
SEPARATED SWITCHING 2 × 1728 HW M = 30

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

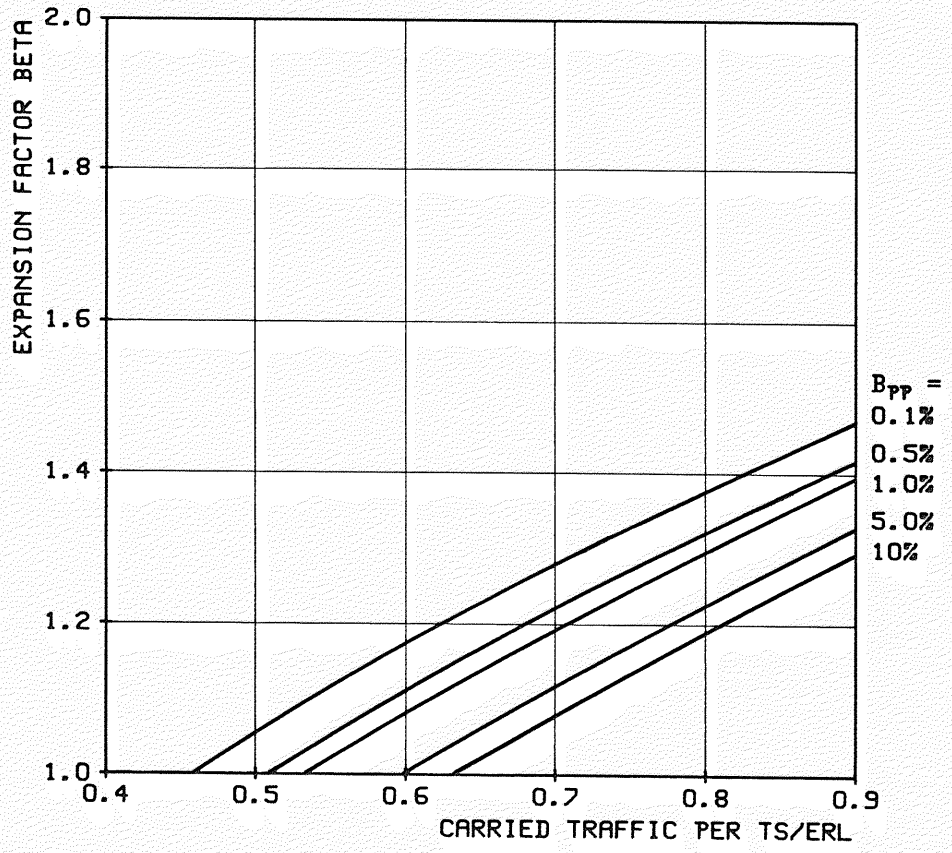
TSSSST

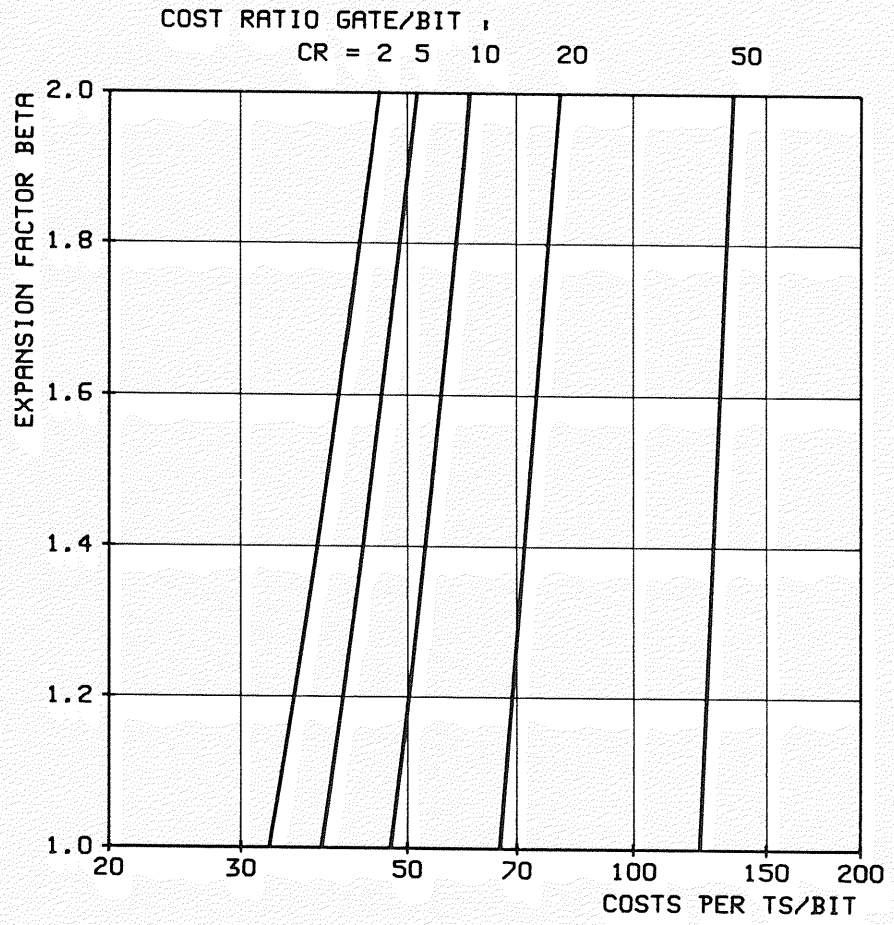




COMBINED SWITCHING	1 × 2197 HW	H_2 = 13	COMBINED SWITCHING
SEPARATED SWITCHING	2 × 2197 HW	M = 30	SEPARATED SWITCHING

TSSSST



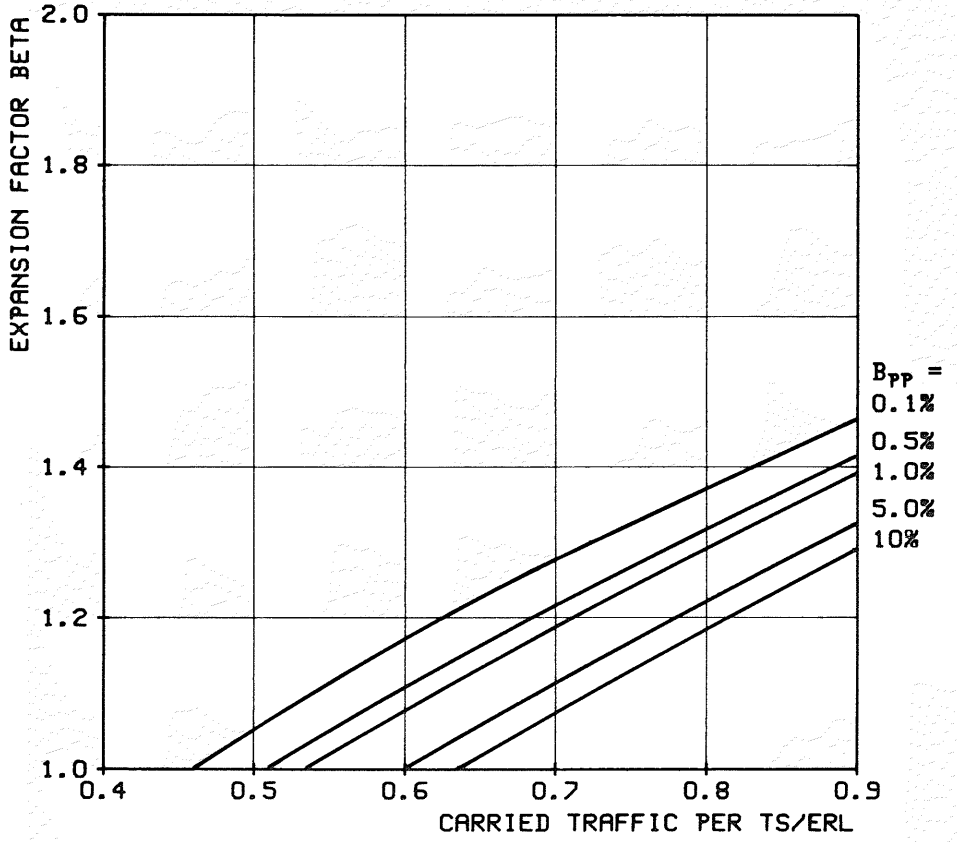


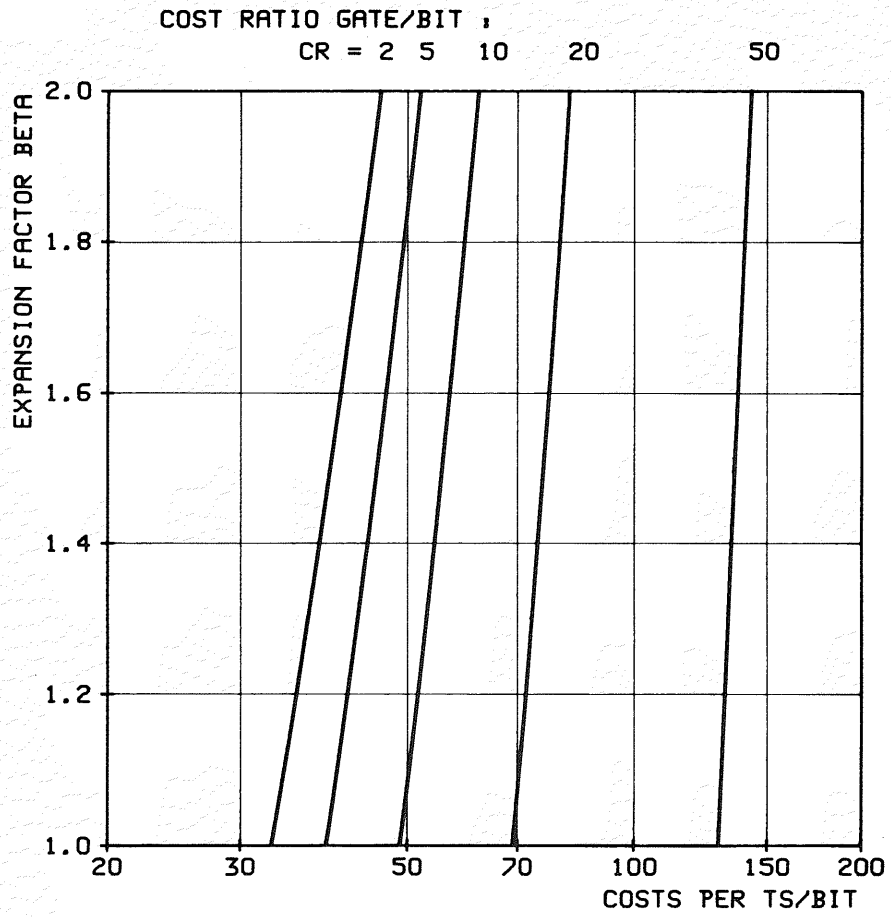
COMBINED SWITCHING 1 × 2744 HW H_2 = 14
SEPARATED SWITCHING 2 × 2744 HW M = 30

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

-CHART 70-

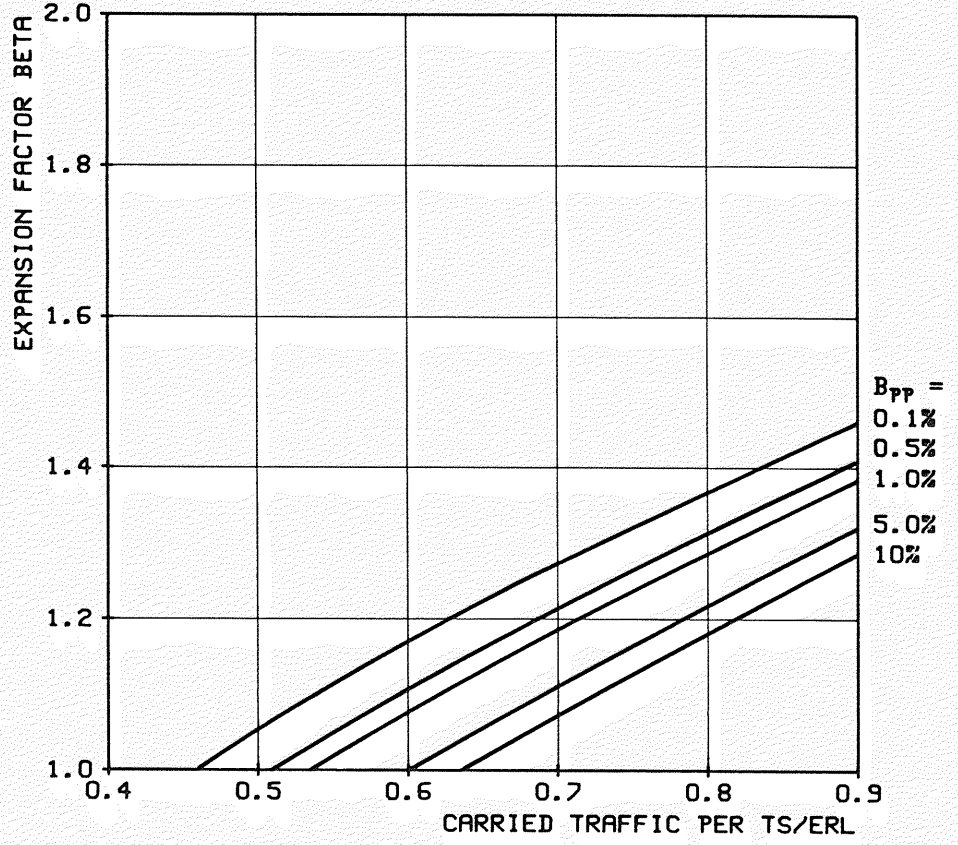
TSSSST

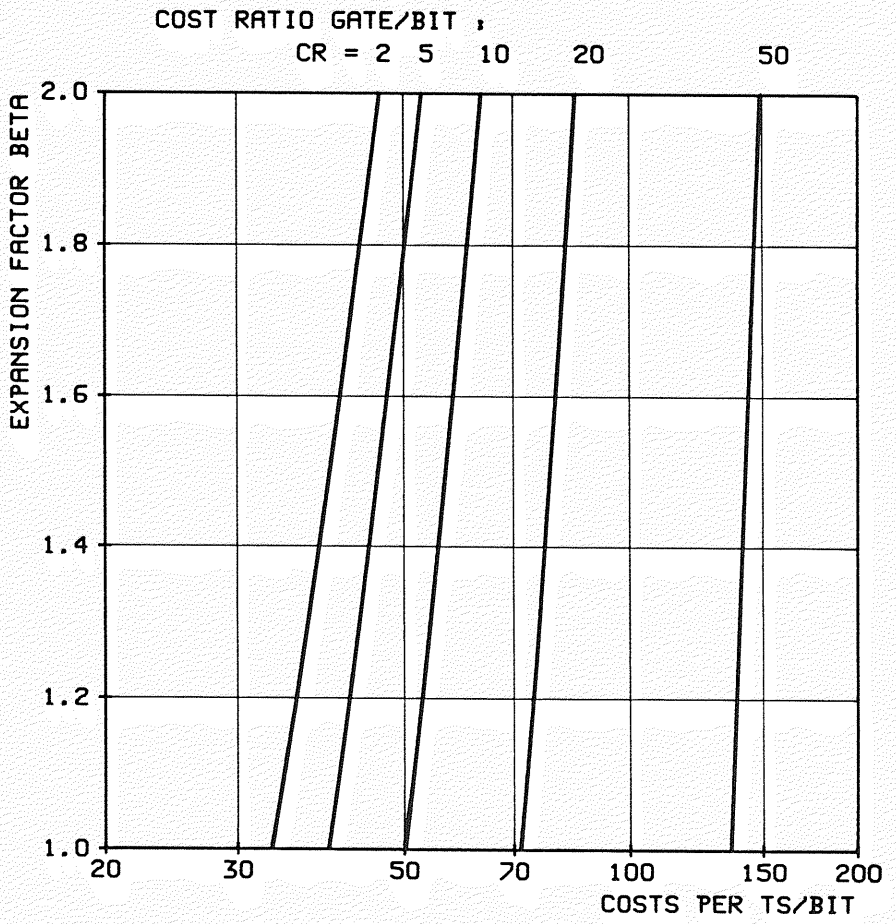




COMBINED SWITCHING	1 × 3375 HW	H_2 = 15	——{ COMBINED SWITCHING
SEPARATED SWITCHING	2 × 3375 HW	M = 30	{ SEPARATED SWITCHING

TSSSST





COMBINED SWITCHING 1 × 4096 HW H_2 = 16
SEPARATED SWITCHING 2 × 4096 HW M = 30

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

PCM SWITCHING ARRAY : TST

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 4, 9, 16, 25, 36, 49, 64,

SEPARATED SWITCHING : HW = 8, 18, 32, 50, 72, 98, 128,

TIME-SLOTS (TS) PER HW : M = 120 TS

POINT-TO-POINT LOSS, PCT1 : B_{PP} = 0.1, 0.5, 1.0, 5.0, 10.0%

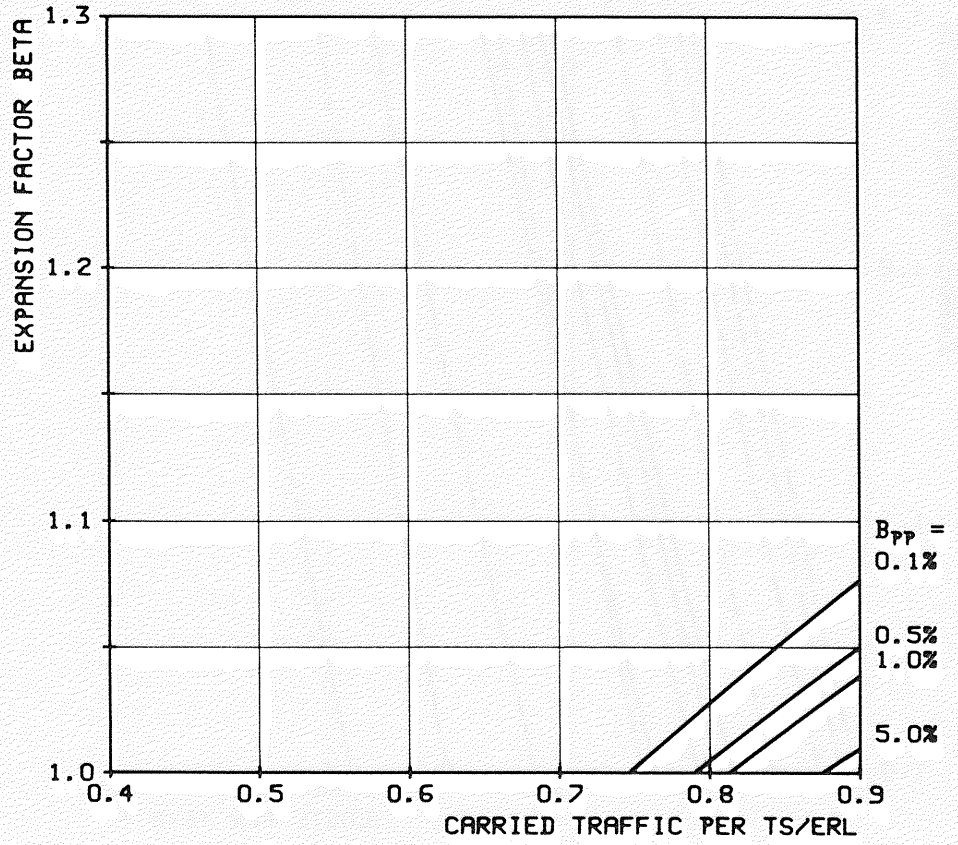
COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

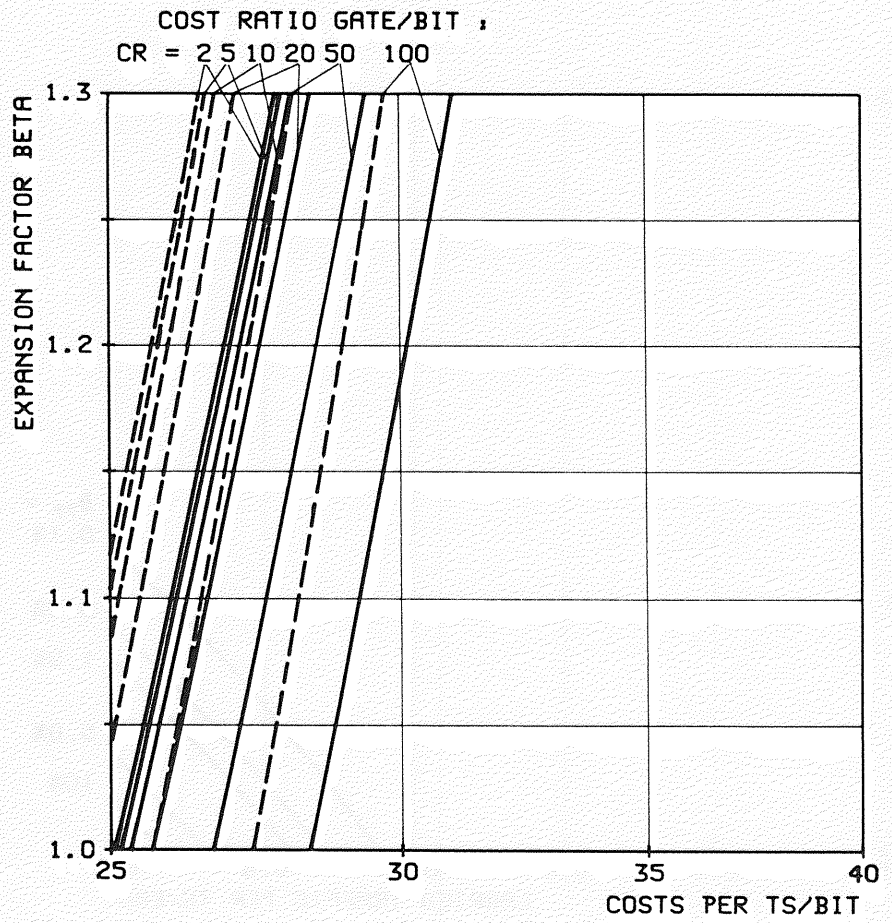
BLOCK SIZE

COMBINED SWITCHING : H_2 = HW

SEPARATED SWITCHING : H_2 = HW/2

TST





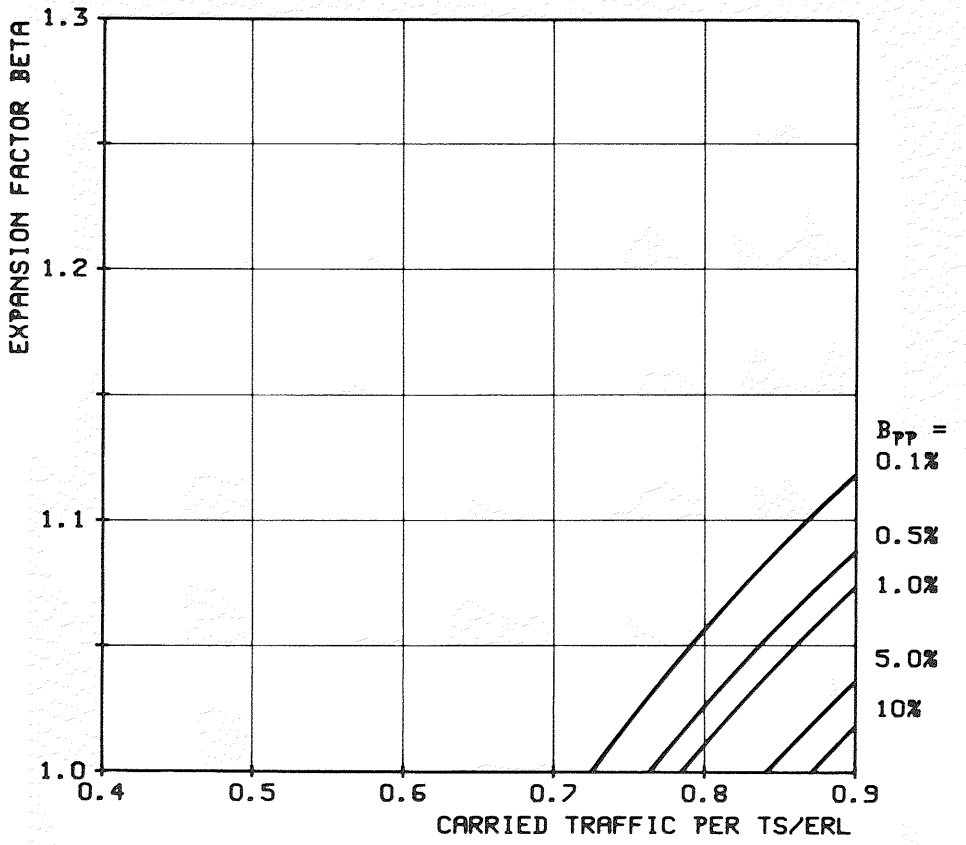
COMBINED SWITCHING 1 × 4 HW H_2 = 4

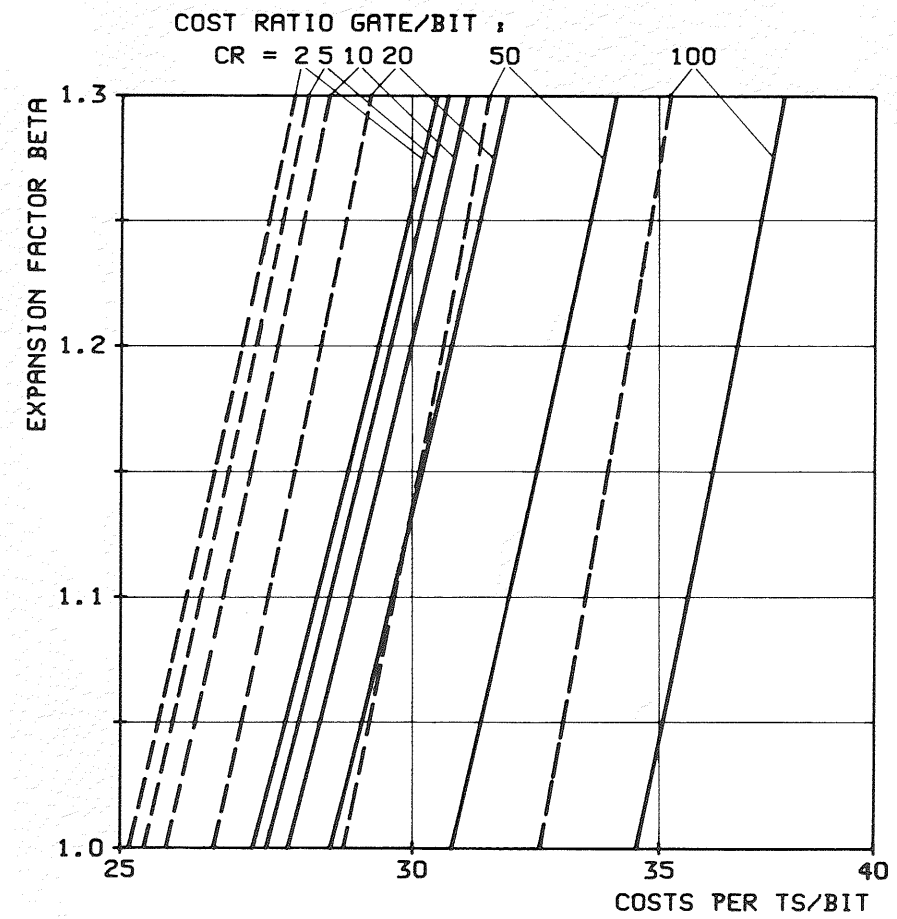
SEPARATED SWITCHING 2 × 4 HW M = 120

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

TST

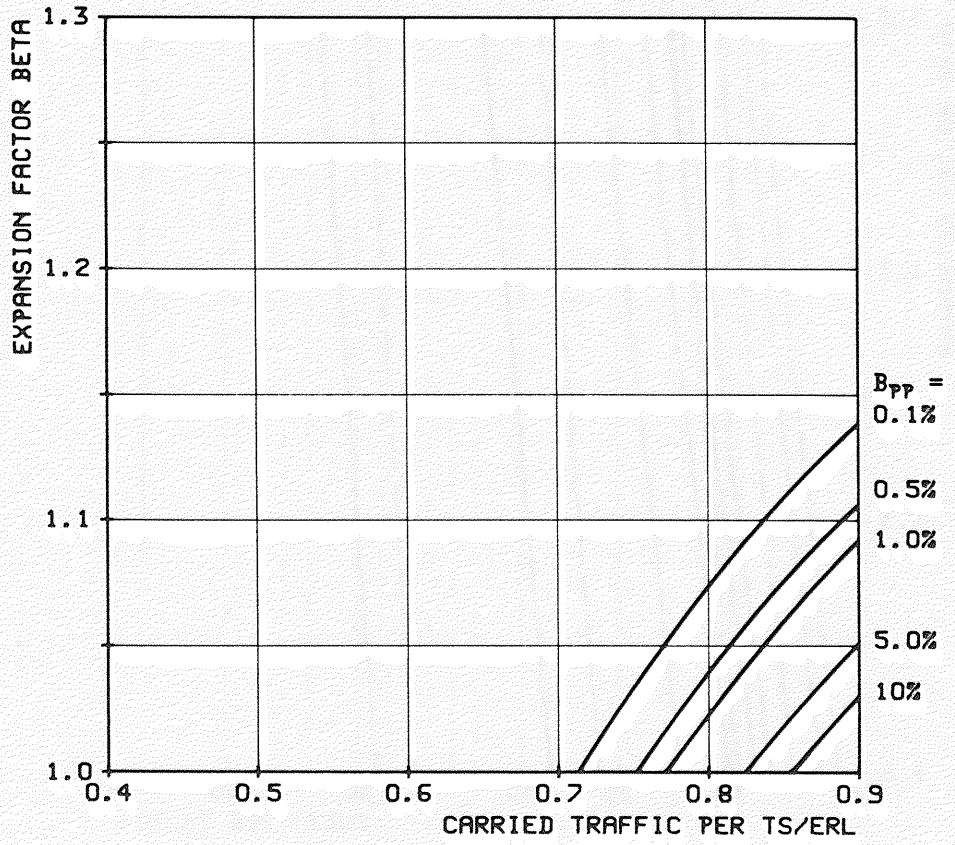


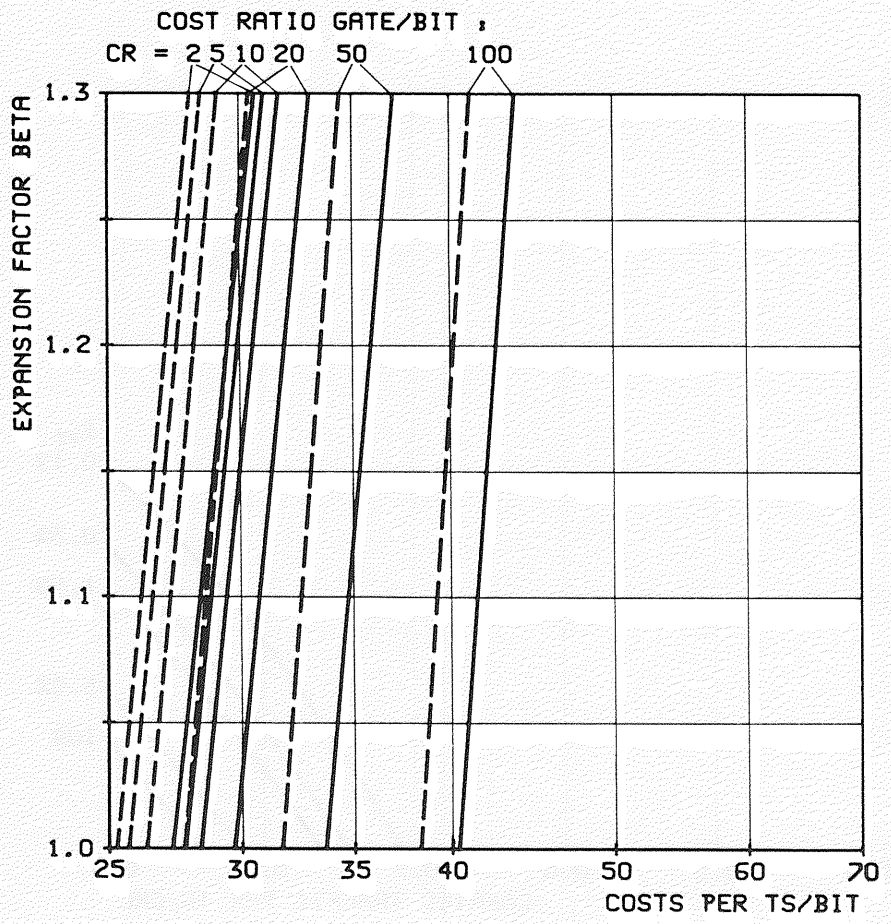


COMBINED SWITCHING 1 × 9 HW H_2 = 9 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 9 HW M = 120 --- SEPARATED SWITCHING

TST

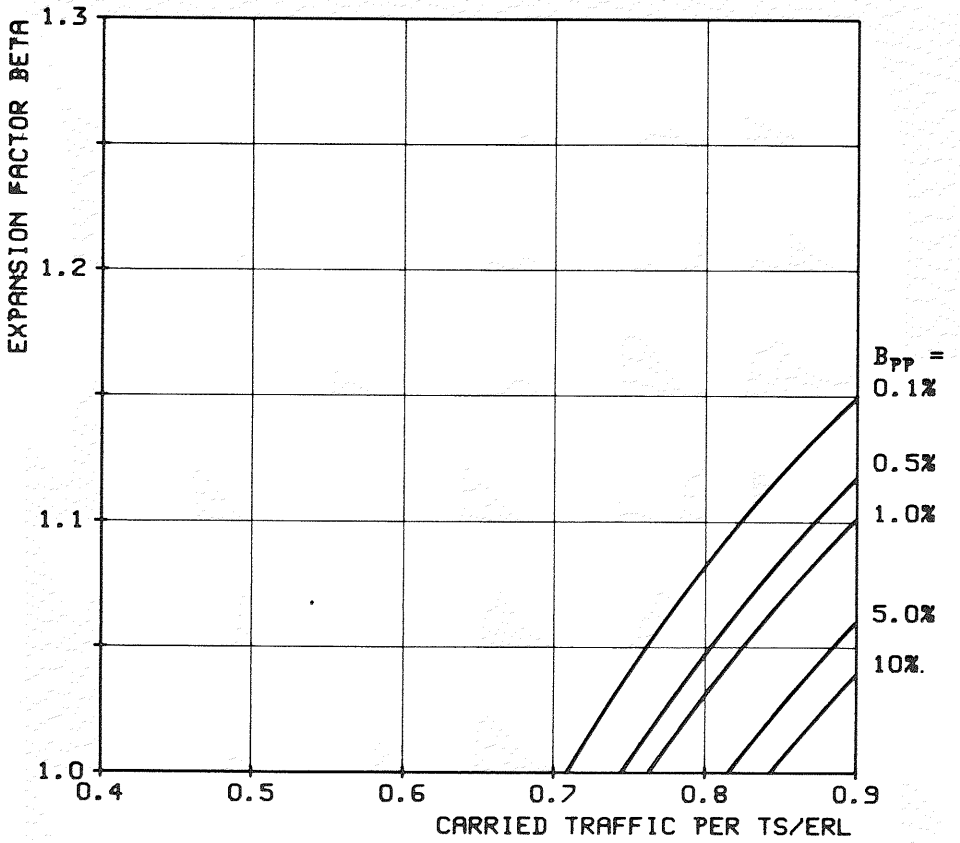


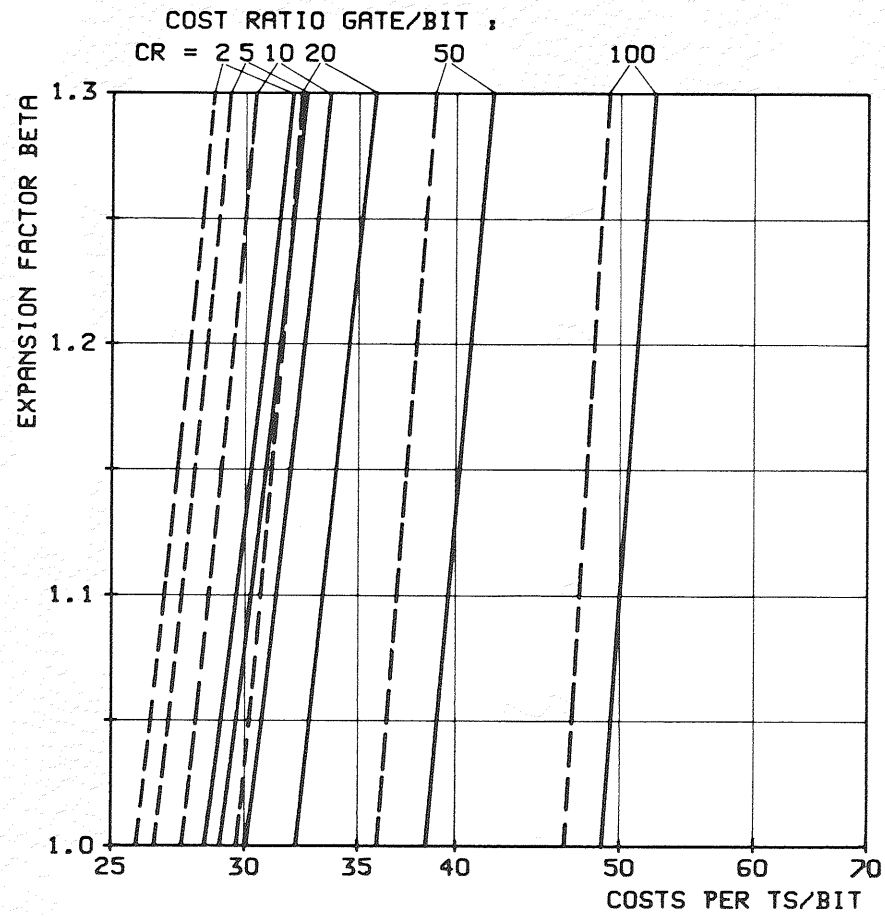


COMBINED SWITCHING 1 × 16 HW H_2 = 16 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 16 HW M = 120 --- SEPARATED SWITCHING

TST

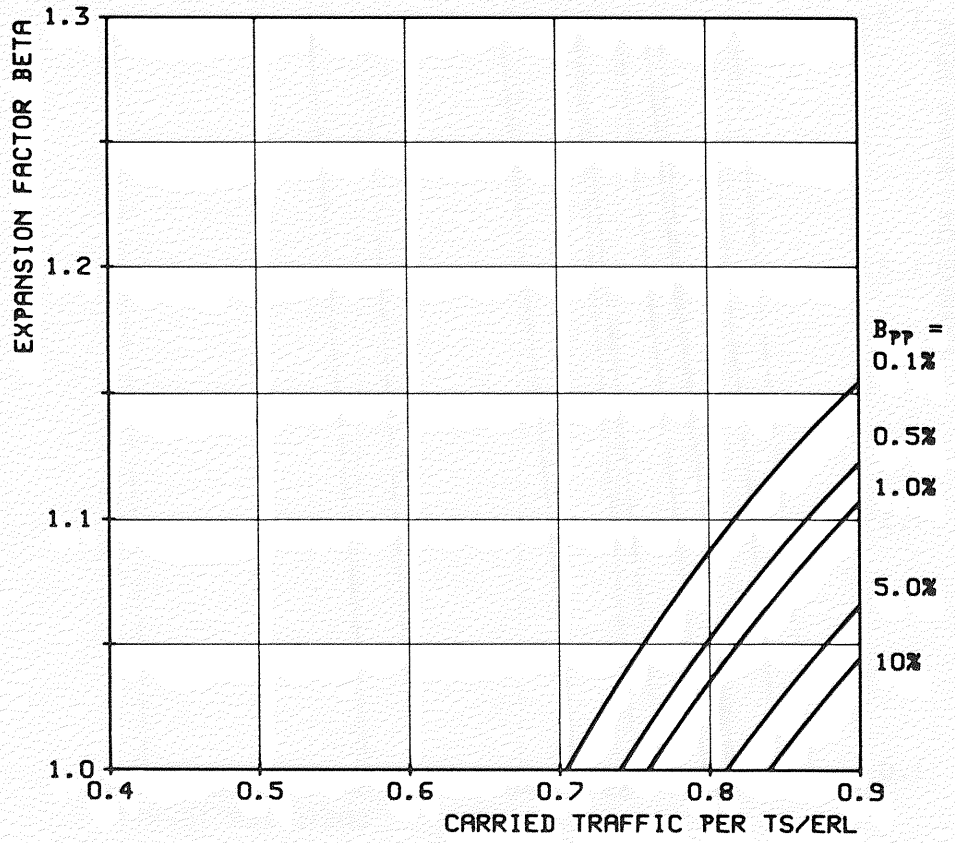


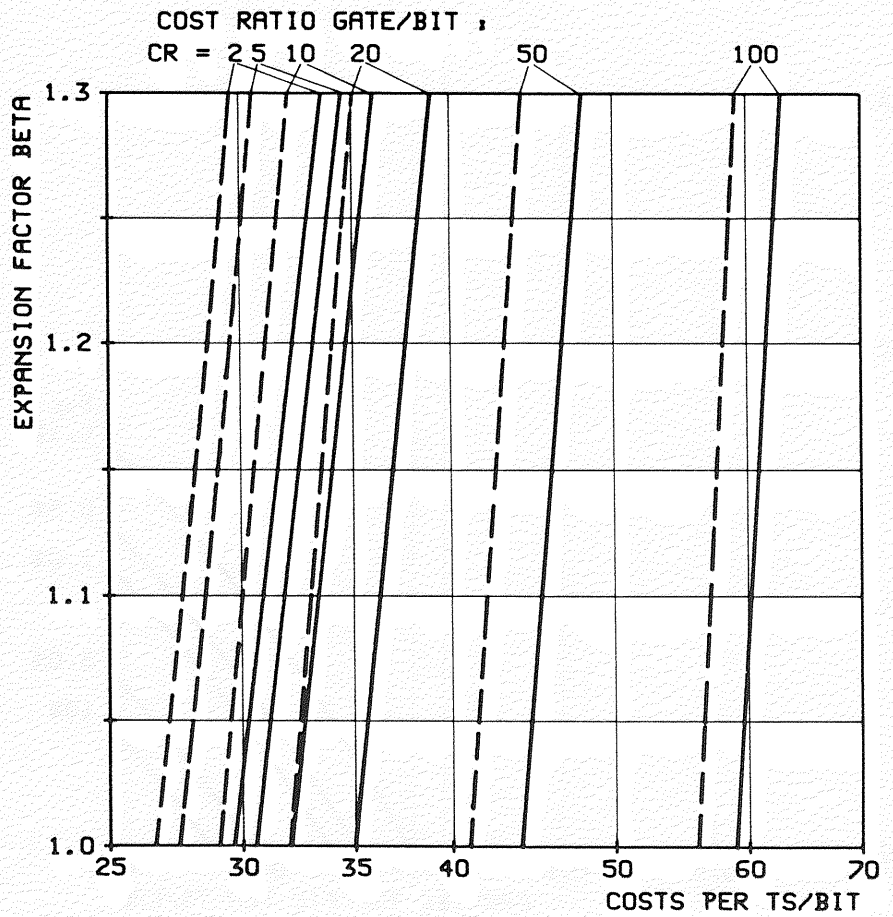


COMBINED SWITCHING 1 × 25 HW H_2 = 25 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 25 HW M = 120 --- SEPARATED SWITCHING

TST

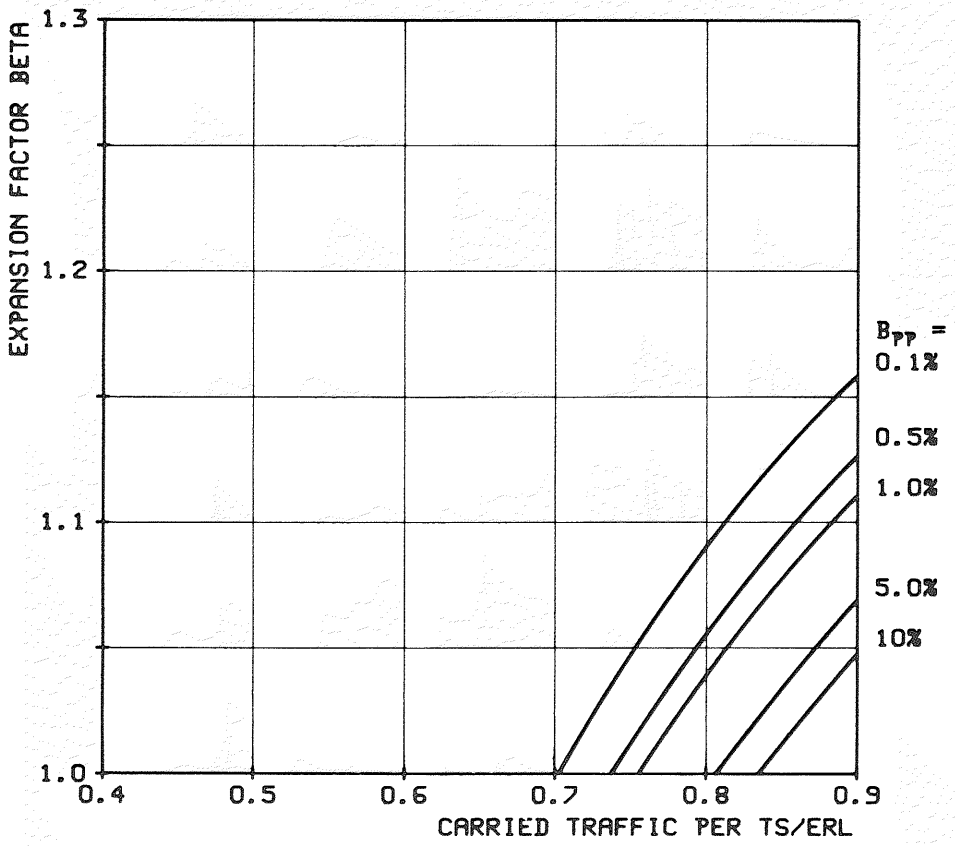


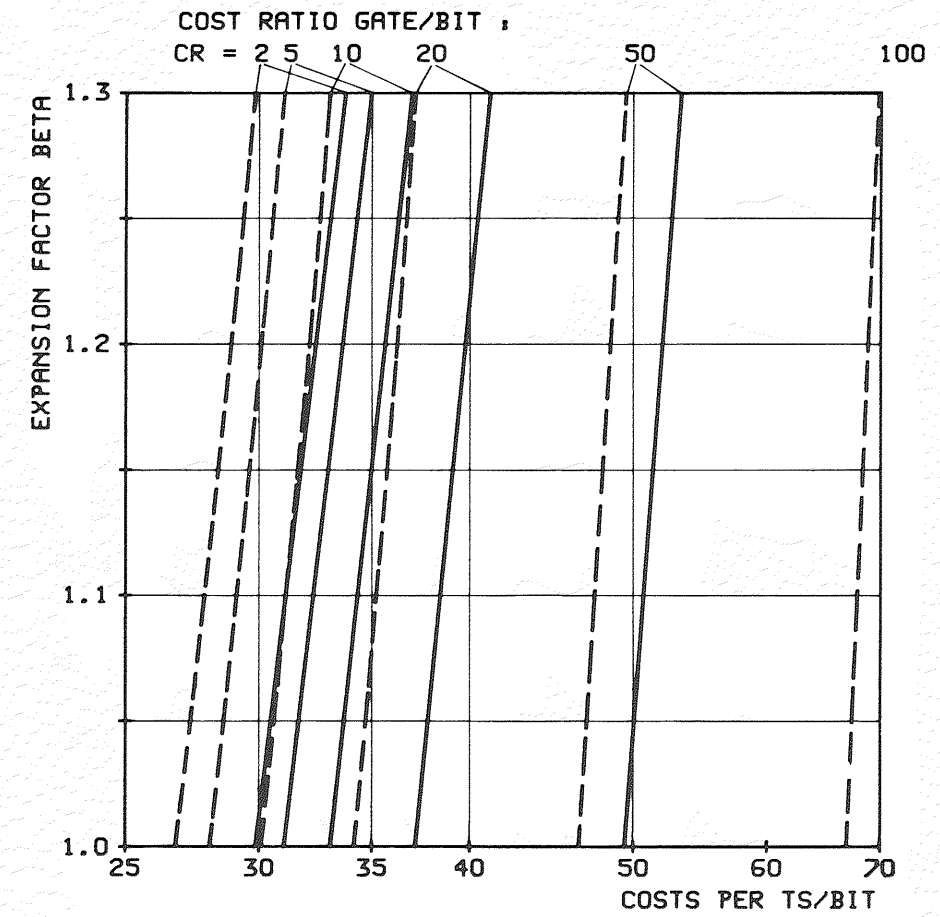


COMBINED SWITCHING 1 × 36 HW H_2 = 36 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 36 HW M = 120 --- SEPARATED SWITCHING

TST

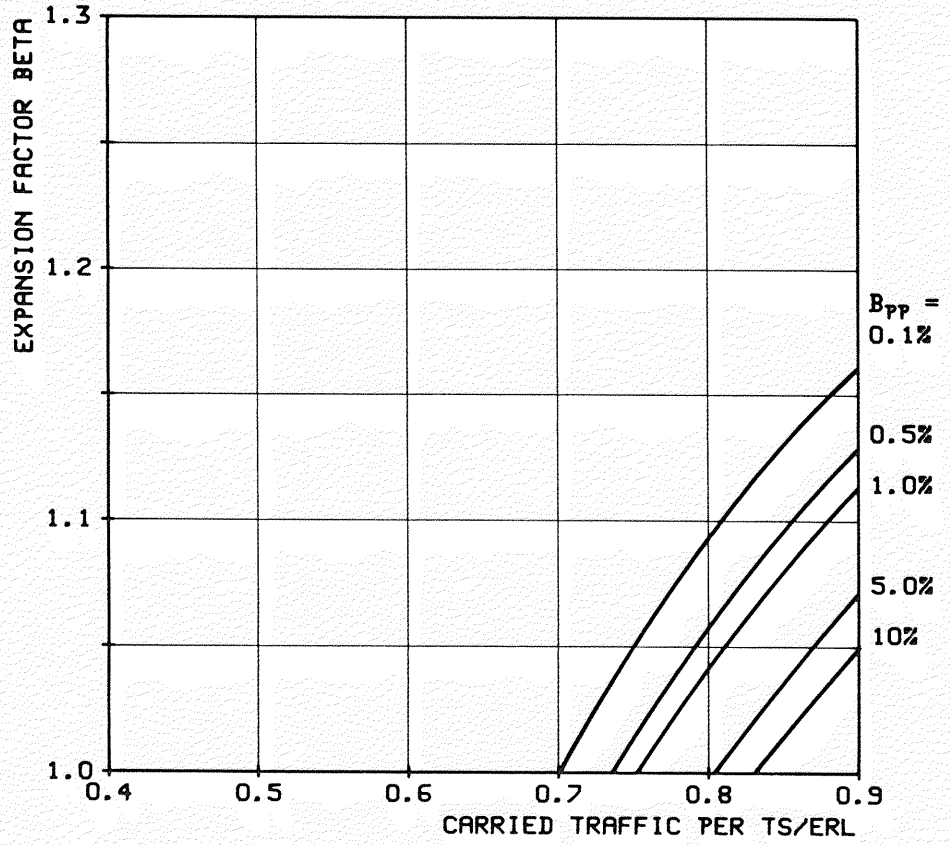


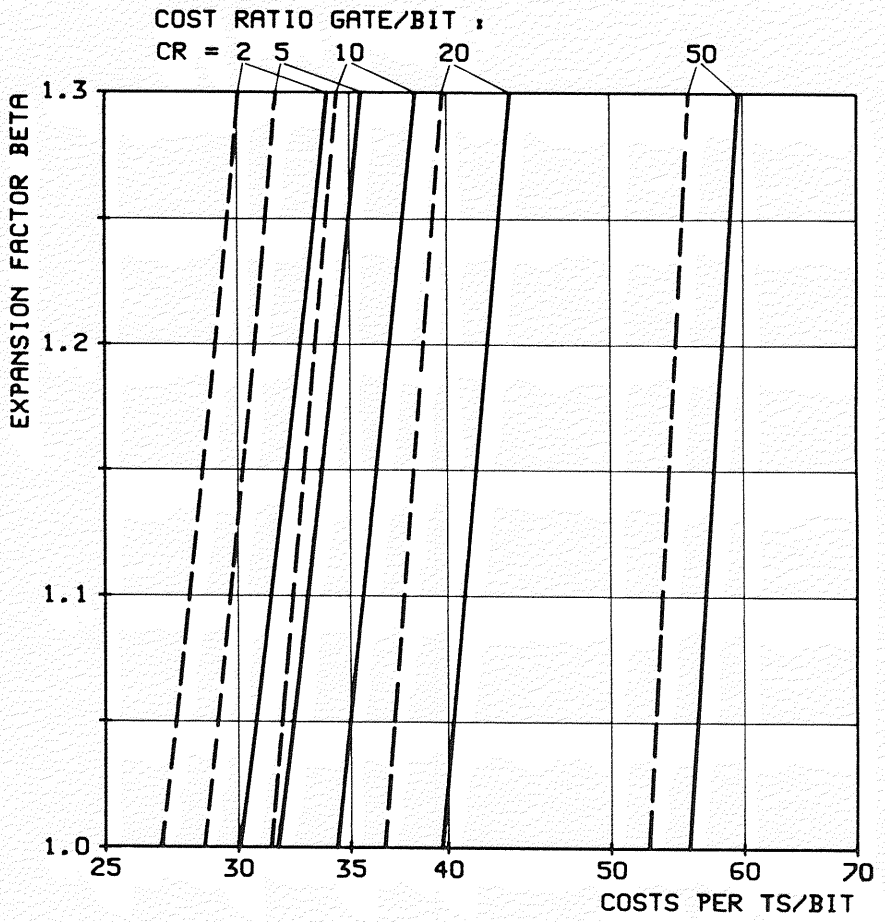


COMBINED SWITCHING 1 × 49 HW H_2 = 49 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 49 HW M = 120 --- SEPARATED SWITCHING

TST





COMBINED SWITCHING 1 × 64 HW H_2 = 64 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 64 HW M = 120 --- SEPARATED SWITCHING

PCM SWITCHING ARRAY : STS

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 9, 16, 25, 36, 49, 64,

SEPARATED SWITCHING : HW = 18, 32, 50, 72, 98, 128,

TIME-SLOTS (TS) PER HW : M = 120 TS

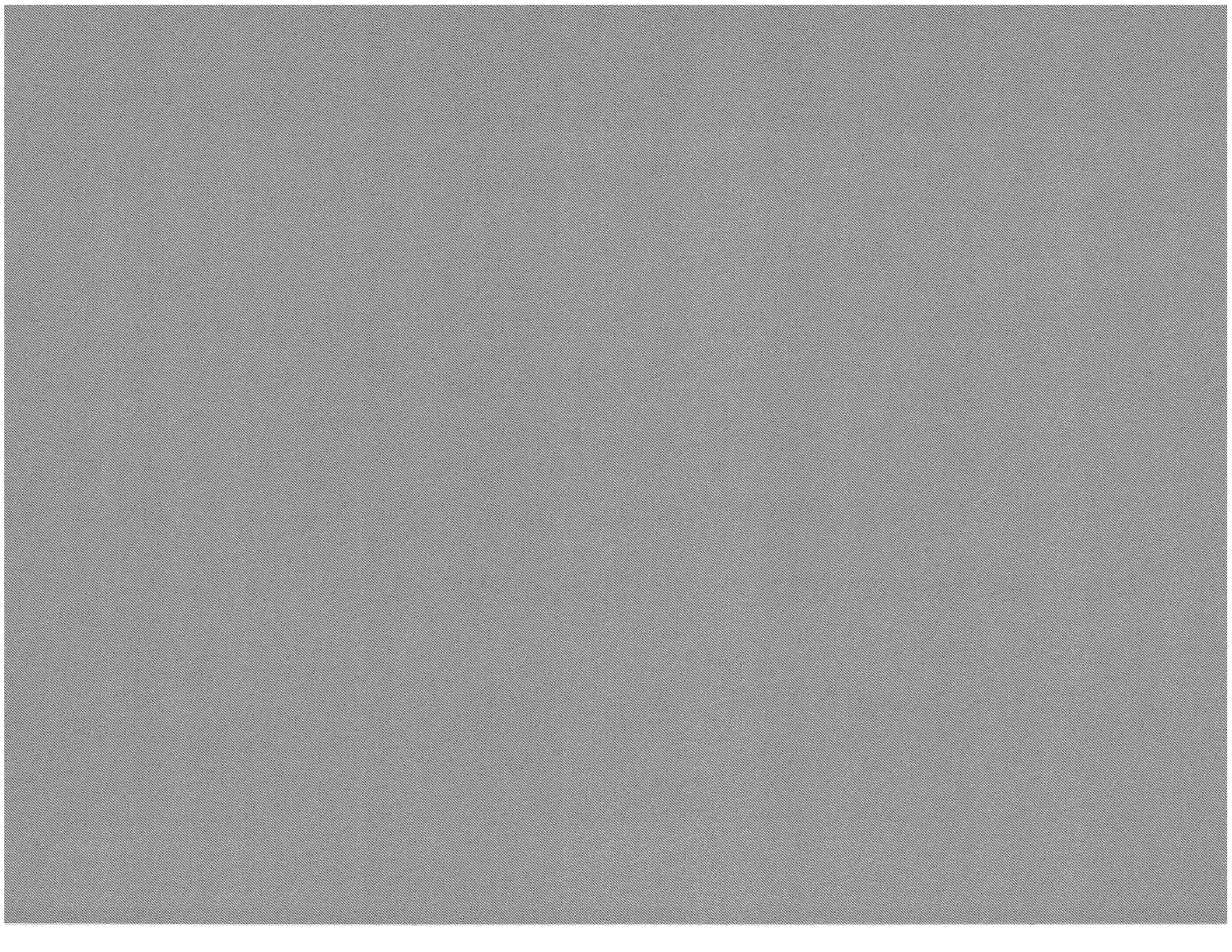
POINT-TO-POINT LOSS, PCT1 : B_{PP} = 0.1, 0.5, 1.0, 5.0, 10.0%

COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

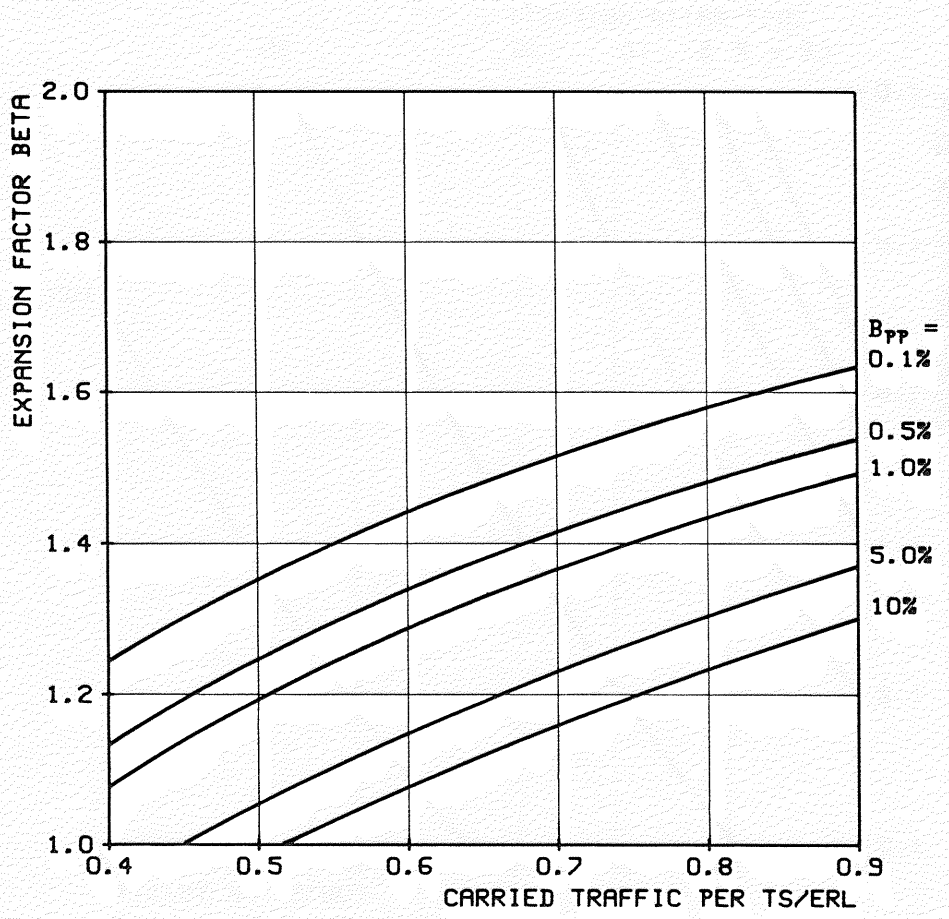
BLOCK SIZE

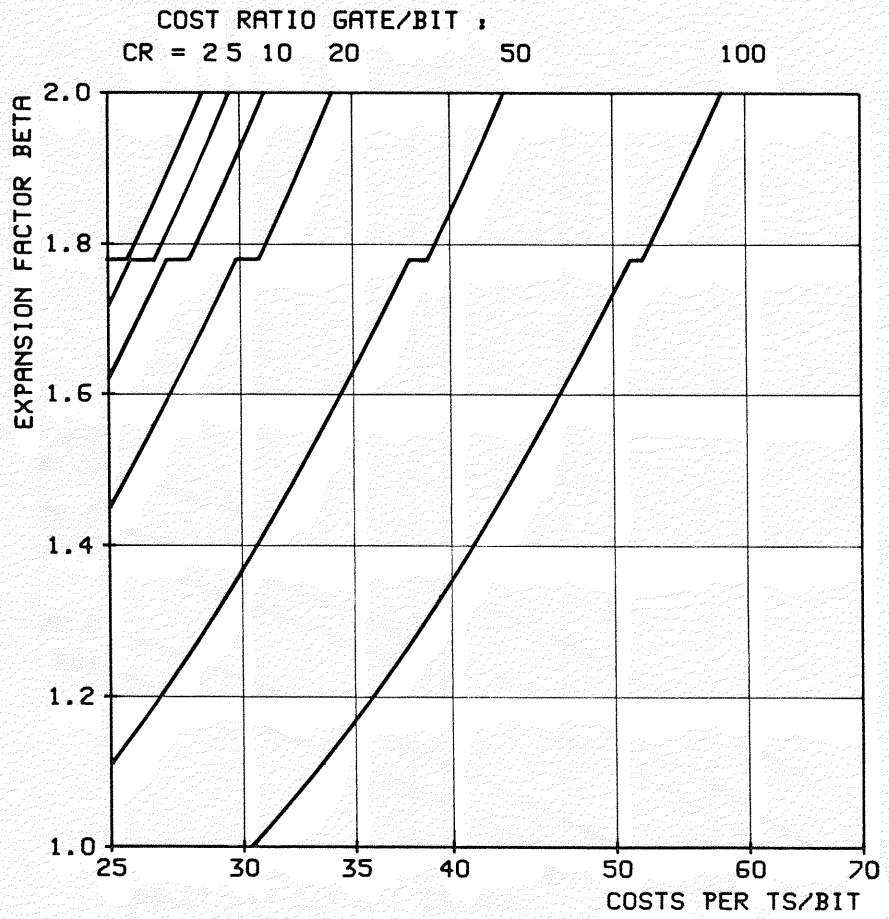
COMBINED SWITCHING : H_1 = HW

SEPARATED SWITCHING : H_1 = HW/2



STS



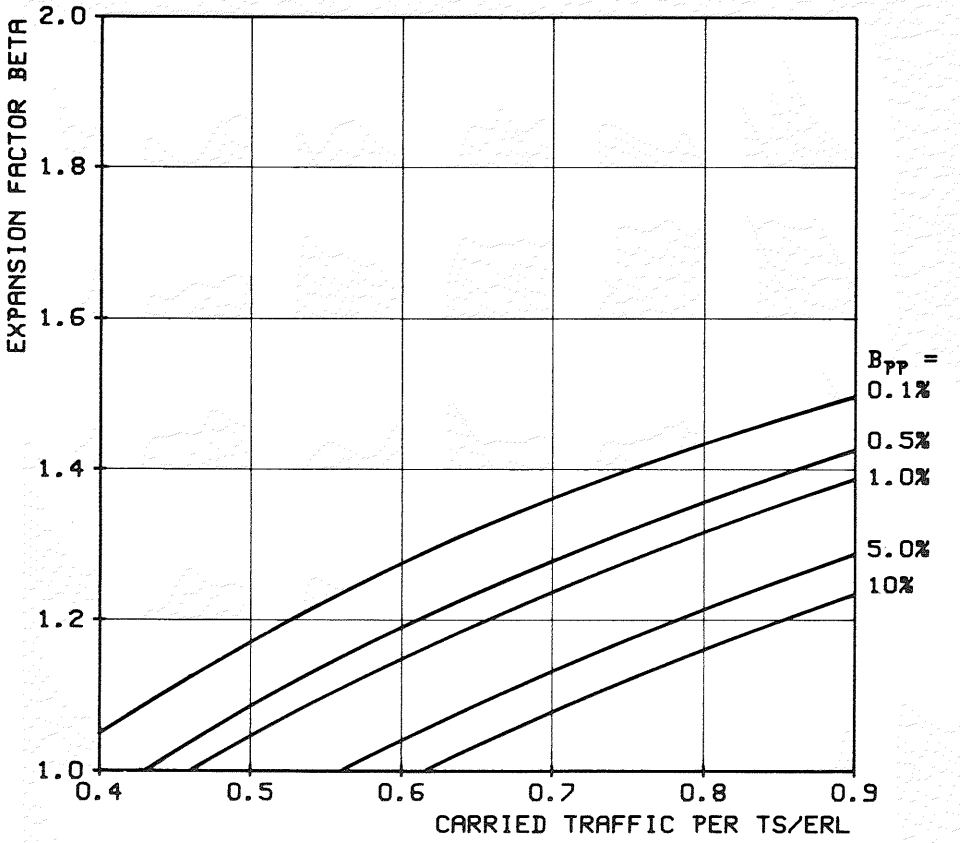


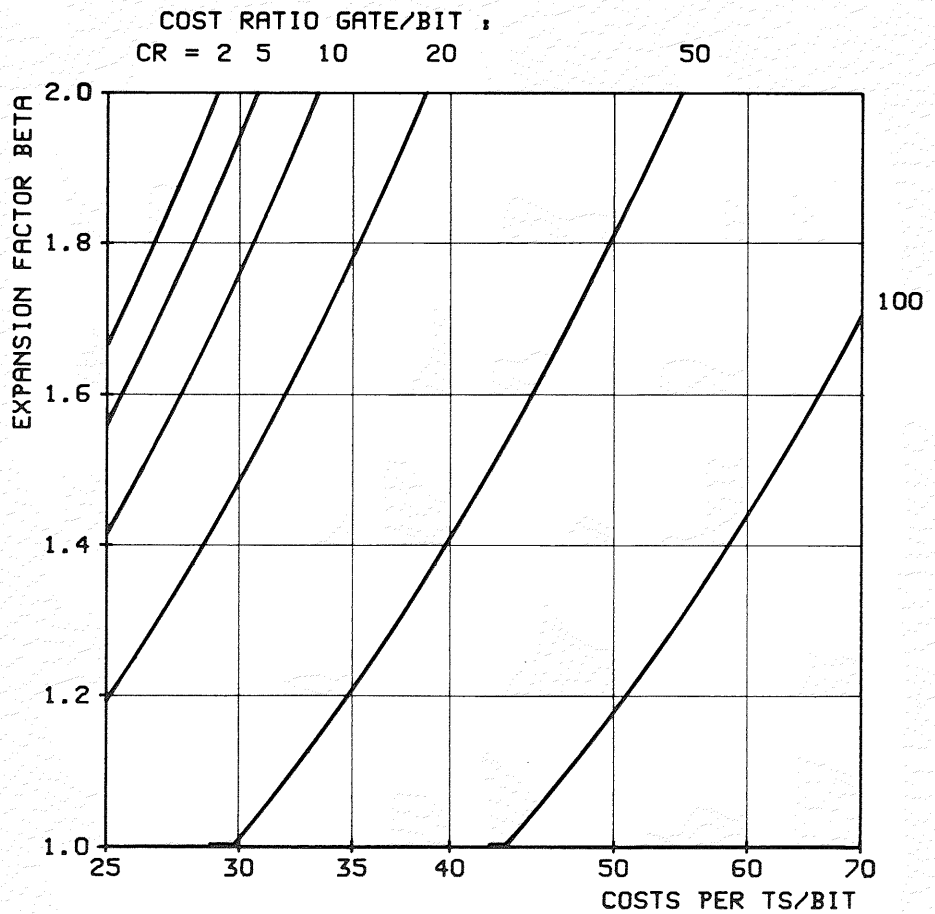
COMBINED SWITCHING 1 × 9 HW H_1 = 9

SEPARATED SWITCHING 2 × 9 HW M = 120

——{ COMBINED SWITCHING
{ SEPRRATED SWITCHING

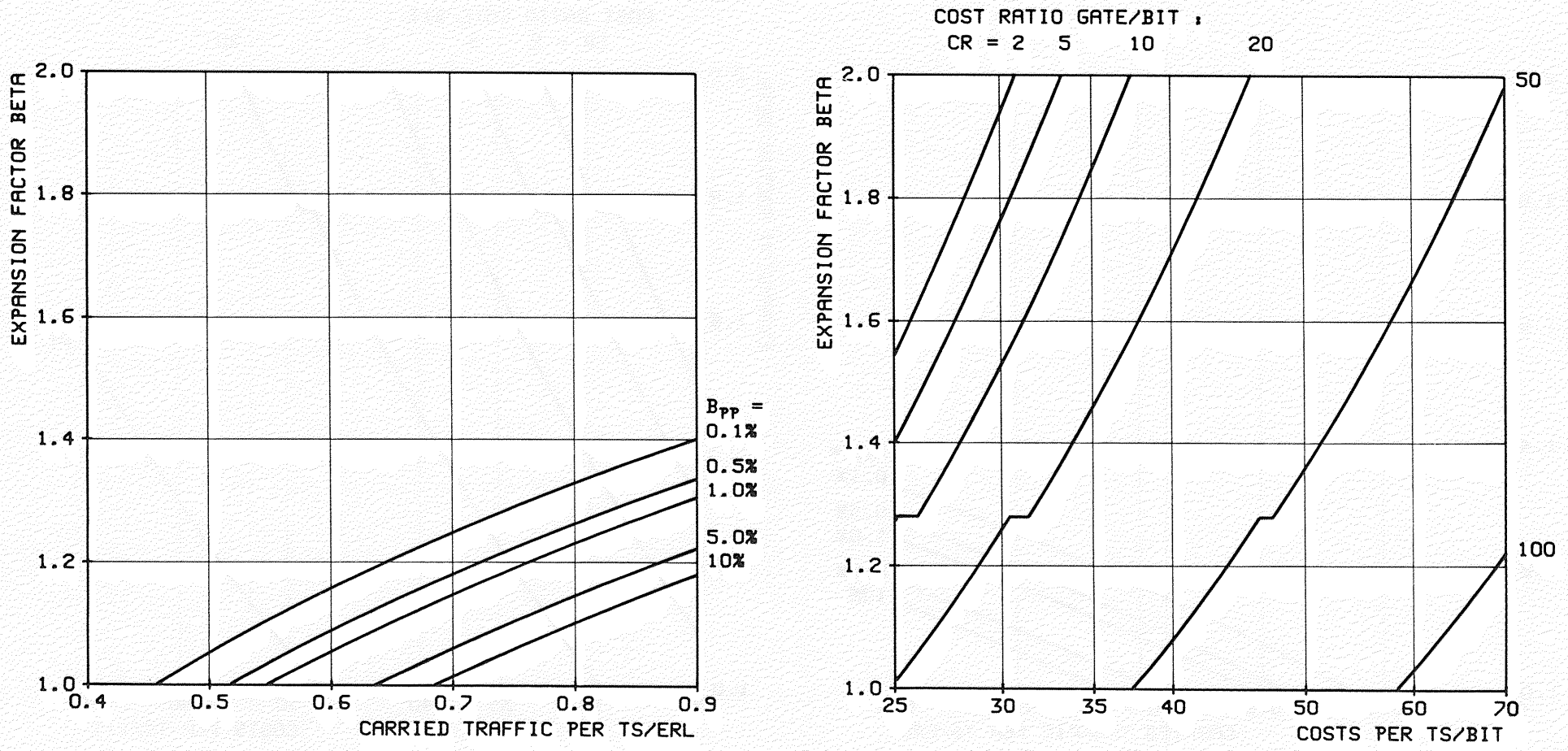
STS





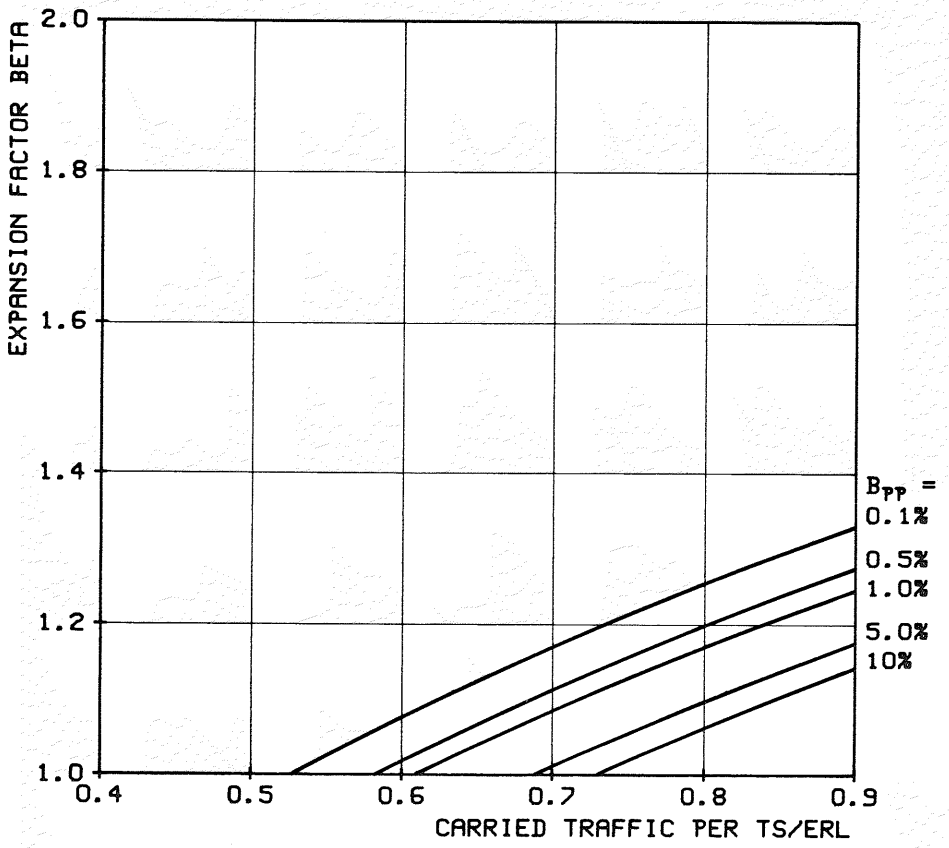
COMBINED SWITCHING	1 × 16 HW	H_1 = 16	—— {COMBINED SWITCHING
SEPARATED SWITCHING	2 × 16 HW	M = 120	{SEPARATED SWITCHING

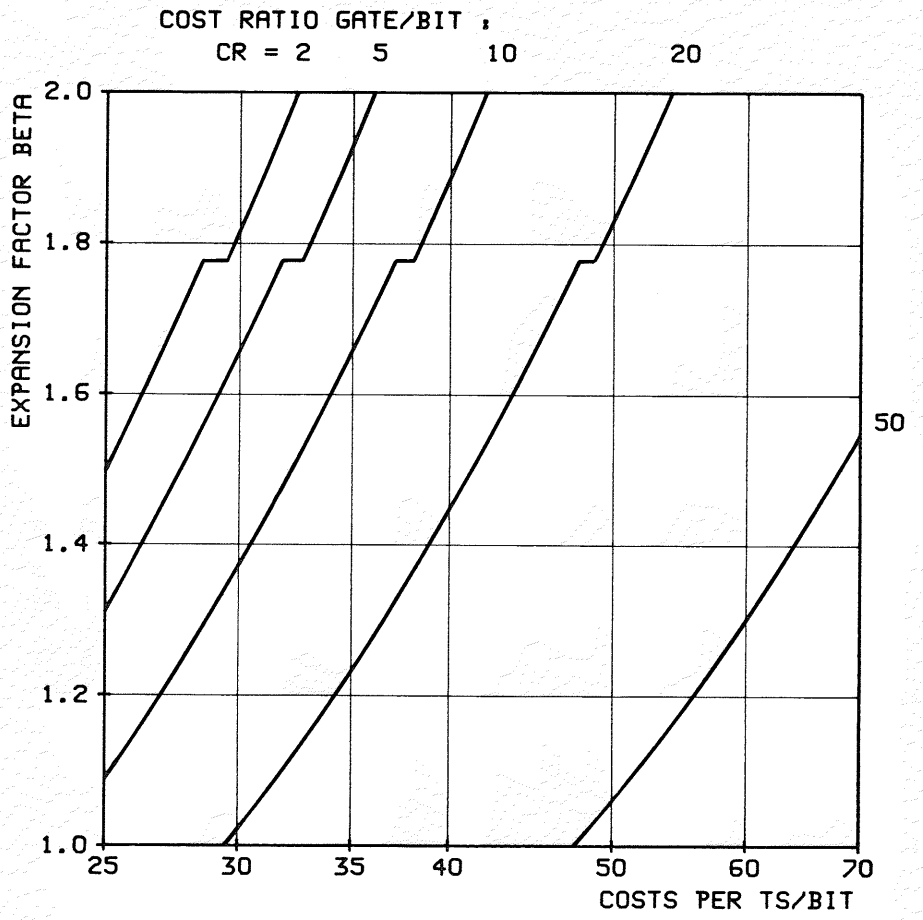
STS



COMBINED SWITCHING	1 × 25 HW	H_1 = 25	{ COMBINED SWITCHING
SEPARATED SWITCHING	2 × 25 HW	M = 120	{ SEPARATED SWITCHING

STS

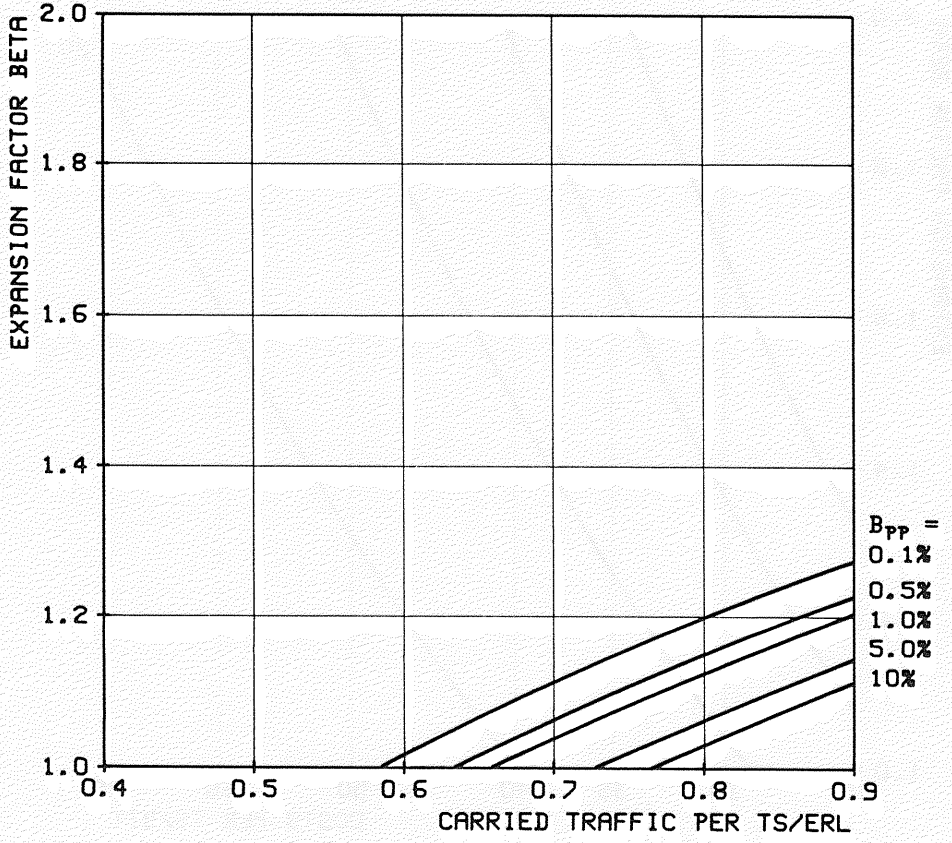


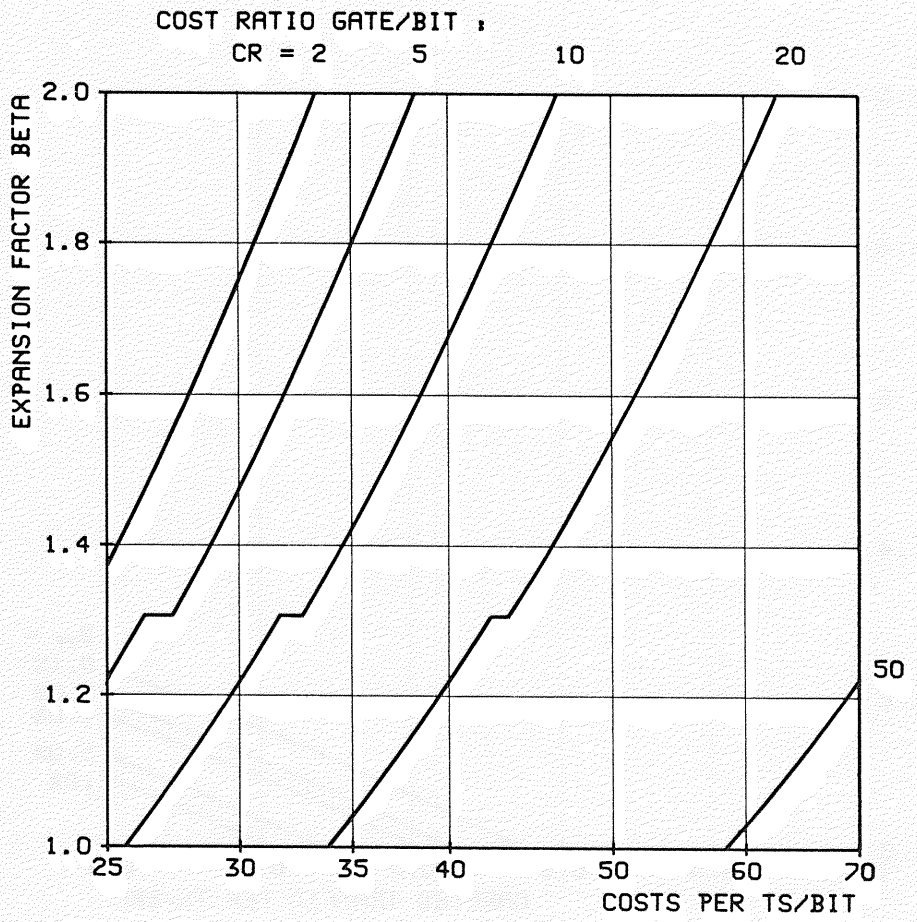


COMBINED SWITCHING 1 × 36 HW H_1 = 36
SEPARATED SWITCHING 2 × 36 HW M = 120

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

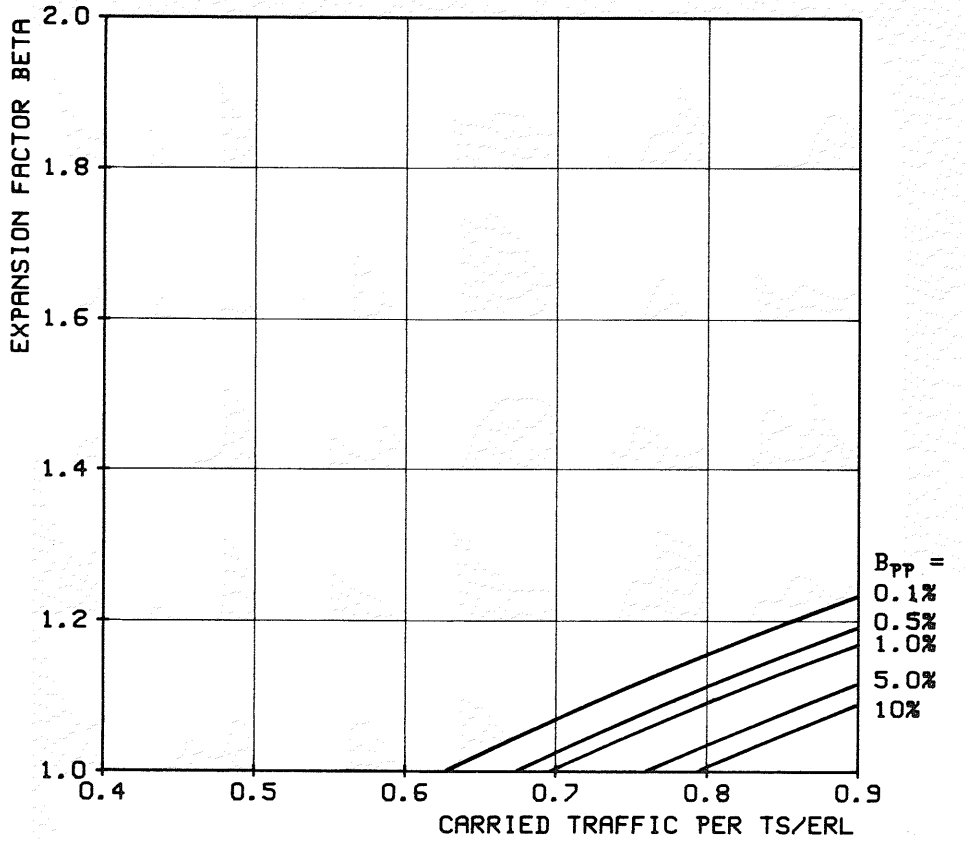
STS

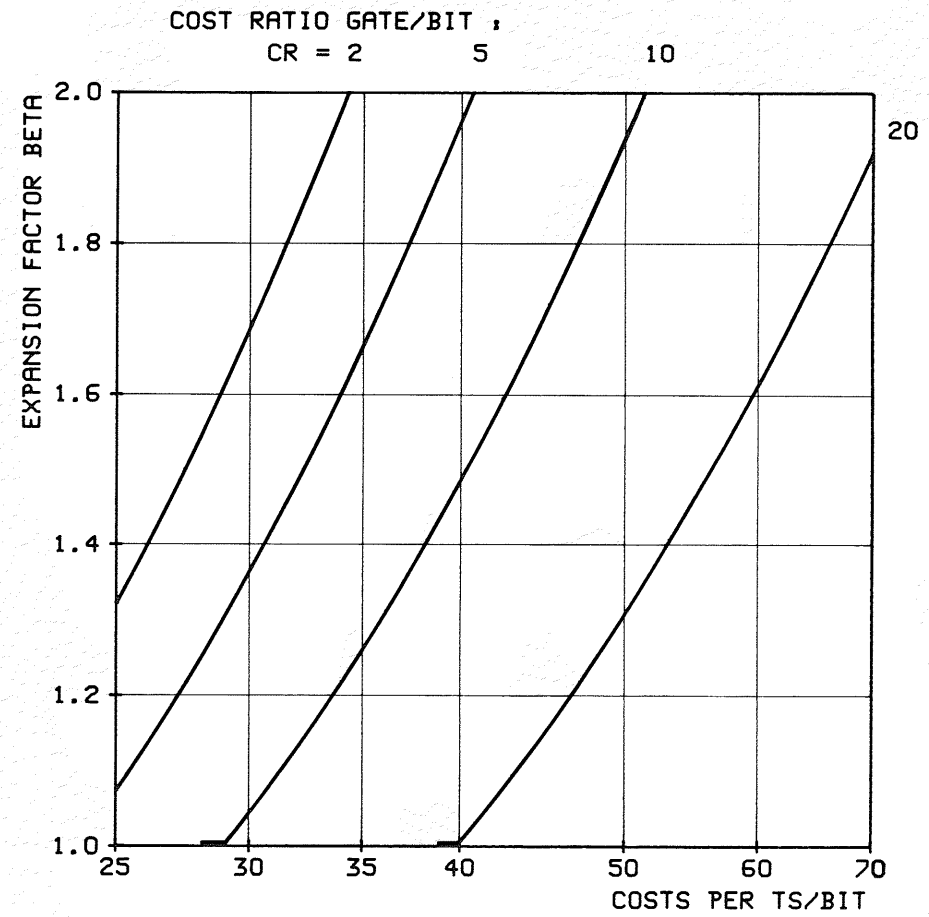




COMBINED SWITCHING	1 × 49 HW	H_1 = 49	—— { COMBINED SWITCHING
SEPARATED SWITCHING	2 × 49 HW	M = 120	{ SEPARATED SWITCHING

STS





COMBINED SWITCHING 1 × 64 HW H_1 = 64

SEPARATED SWITCHING 2 × 64 HW M = 120

—— { COMBINED SWITCHING
SEPARATED SWITCHING

PCM SWITCHING ARRAY : TSST

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 4, 9, 16, 25, 36, 64, 100, 144, 196, 256, 324, 400, 484, 625, 784, 1024,

SEPARATED SWITCHING : HW = 8, 18, 32, 50, 72, 128, 200, 288, 392, 512, 648, 800, 968, 1250, 1568, 2048,

TIME-SLOTS (TS) PER HW : M = 120 TS

POINT-TO-POINT LOSS, PCT1 : B_{PP} = 0.1, 0.5, 1.0, 5.0, 10.0%

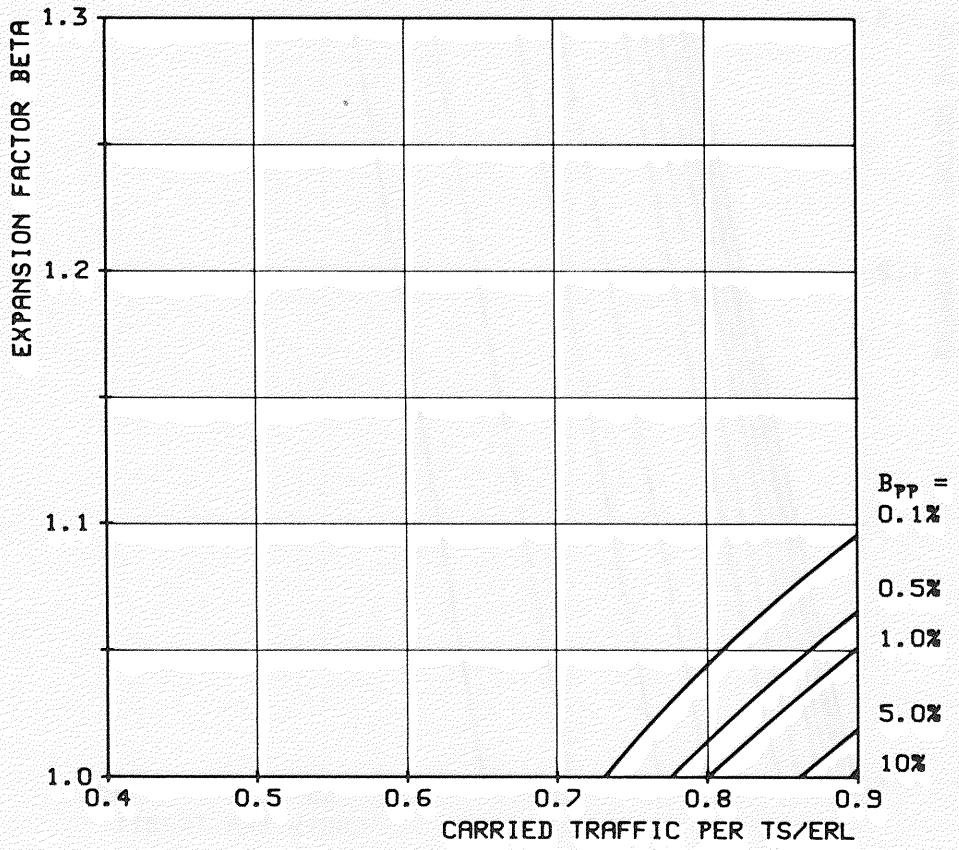
COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

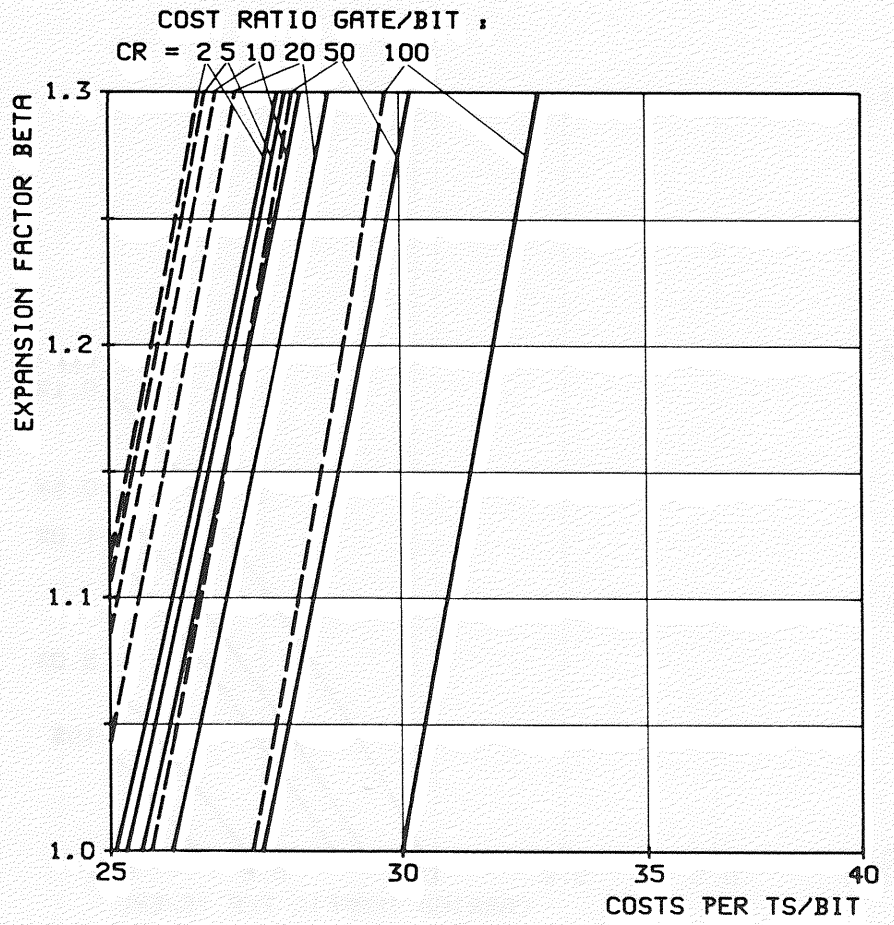
BLOCK SIZE

COMBINED SWITCHING : $H_2 = \sqrt{HW}$

SEPARATED SWITCHING : $H_2 = \sqrt{HW/2}$

TSST

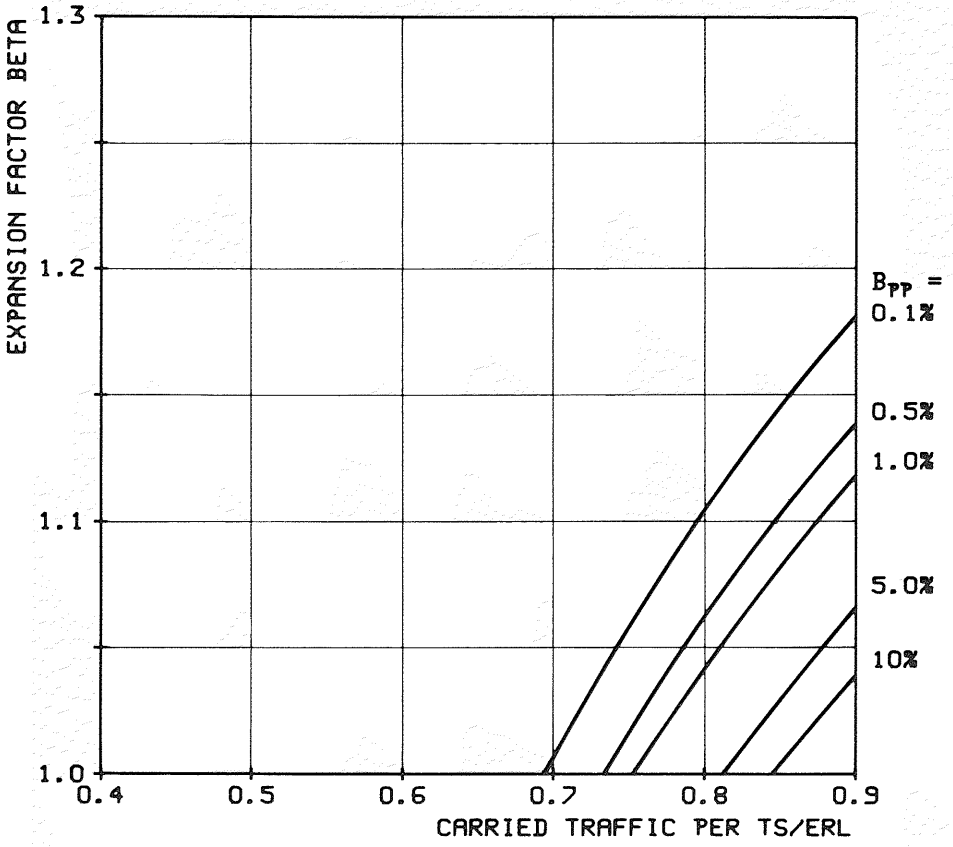


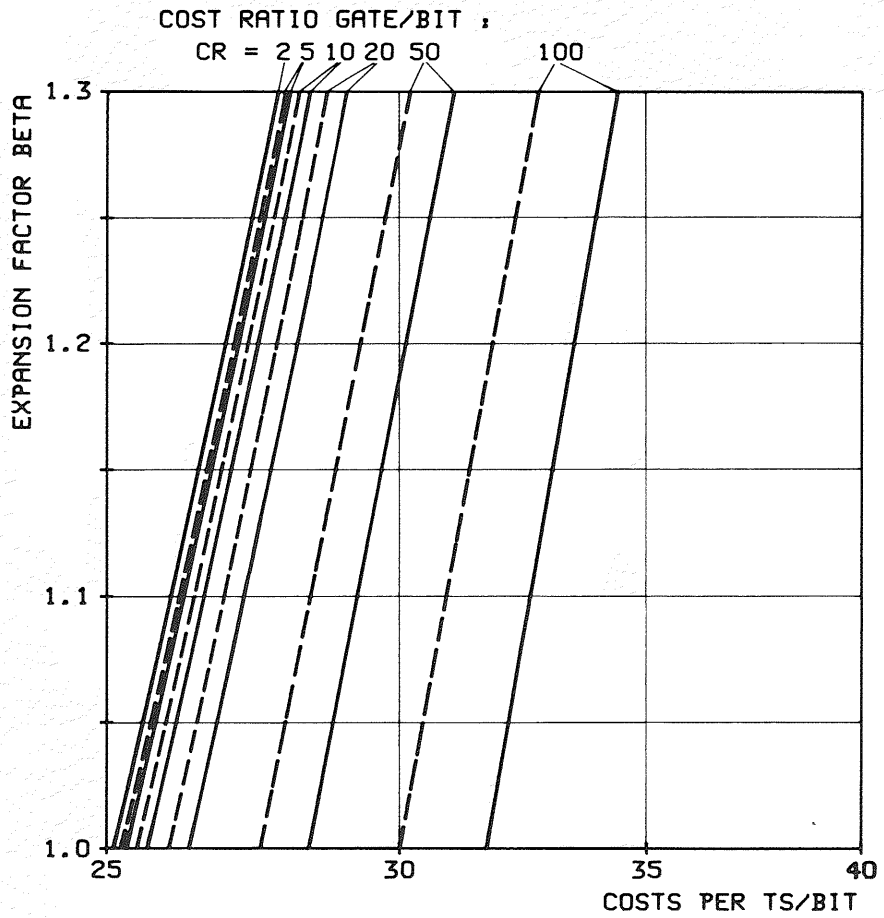


COMBINED SWITCHING 1 × 4 HW H_2 = 2 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 4 HW M = 120 --- SEPARATED SWITCHING

TSST

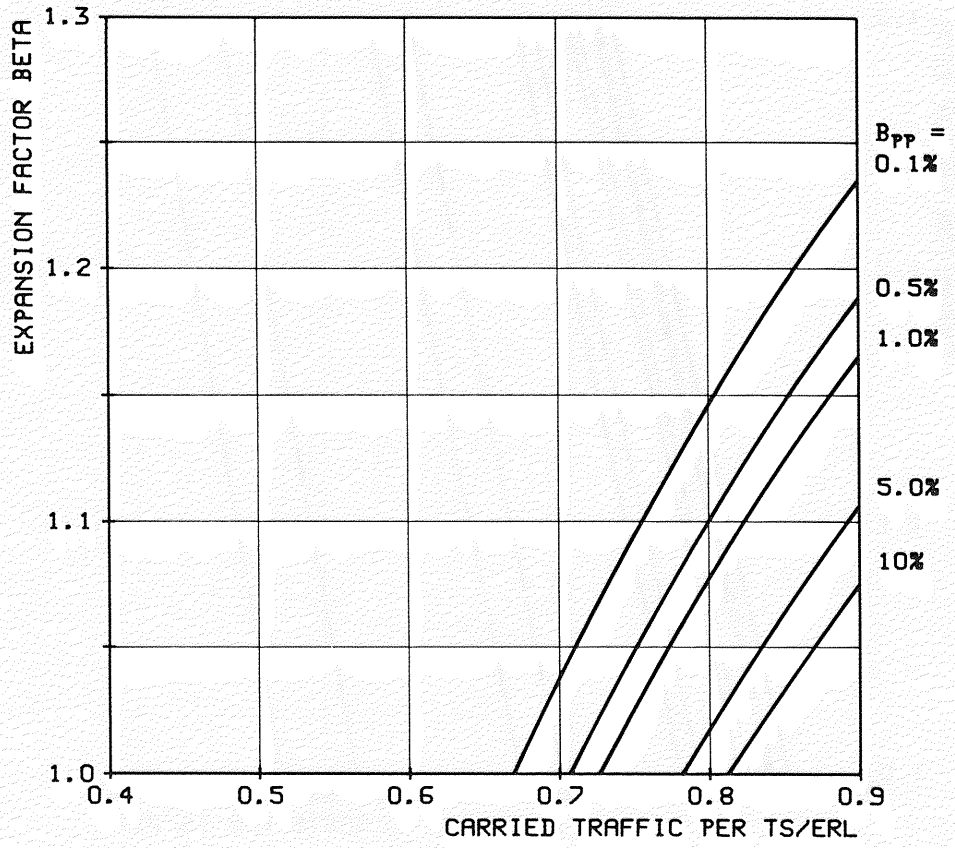


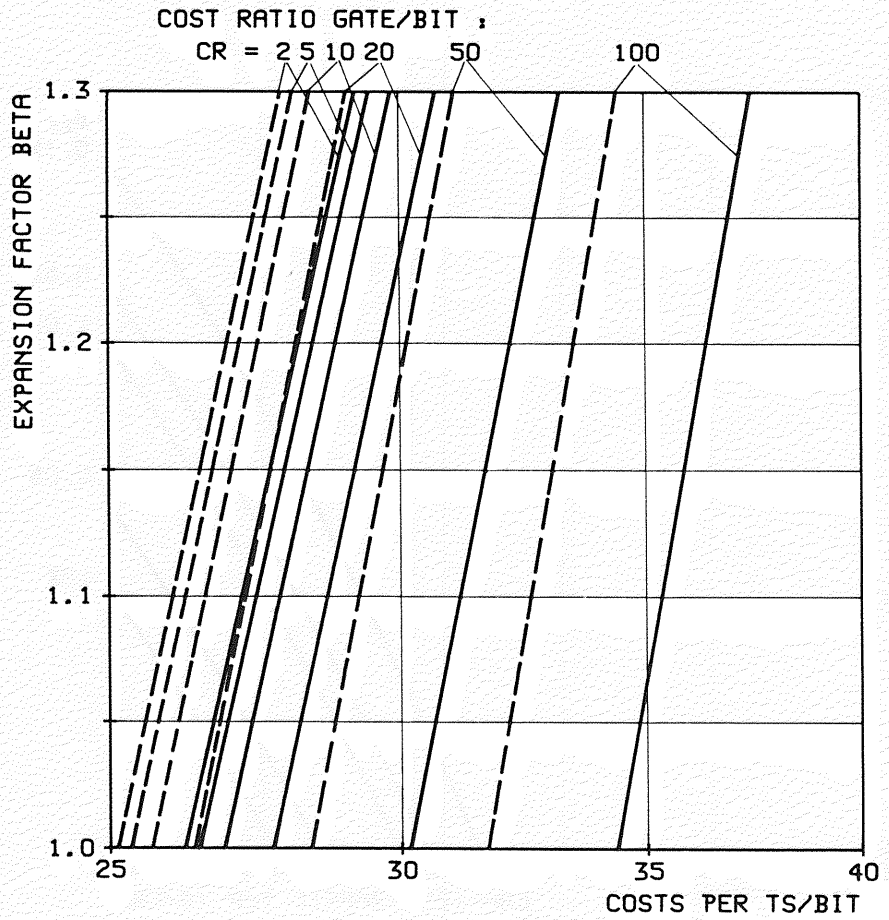


COMBINED SWITCHING 1 × 9 HW H_2 = 3
SEPARATED SWITCHING 2 × 9 HW M = 120

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

TSST

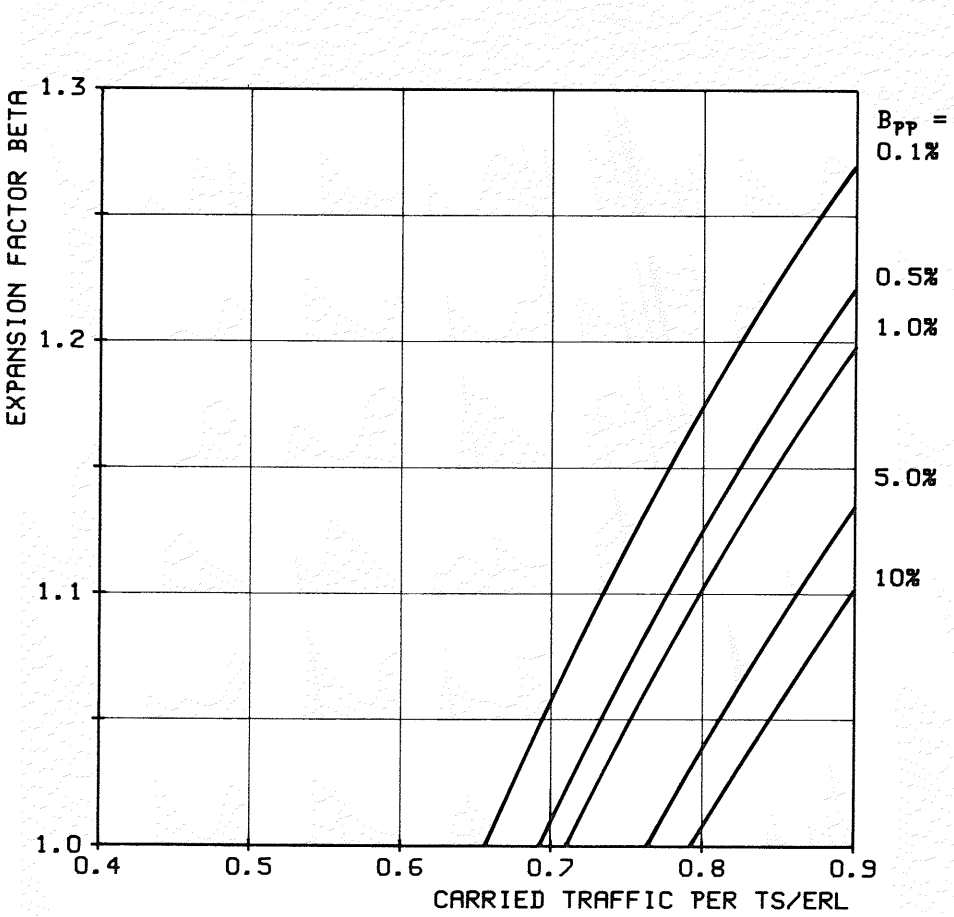


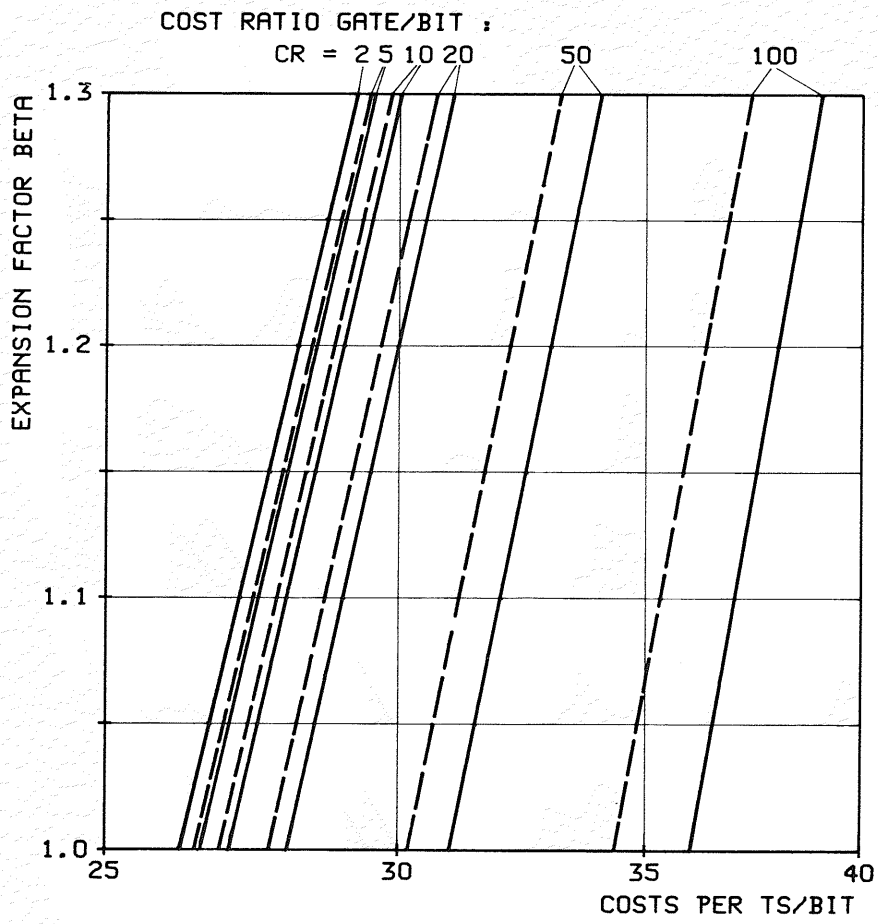


COMBINED SWITCHING 1 × 16 HW H_2 = 4 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 16 HW M = 120 --- SEPARATED SWITCHING

TSST

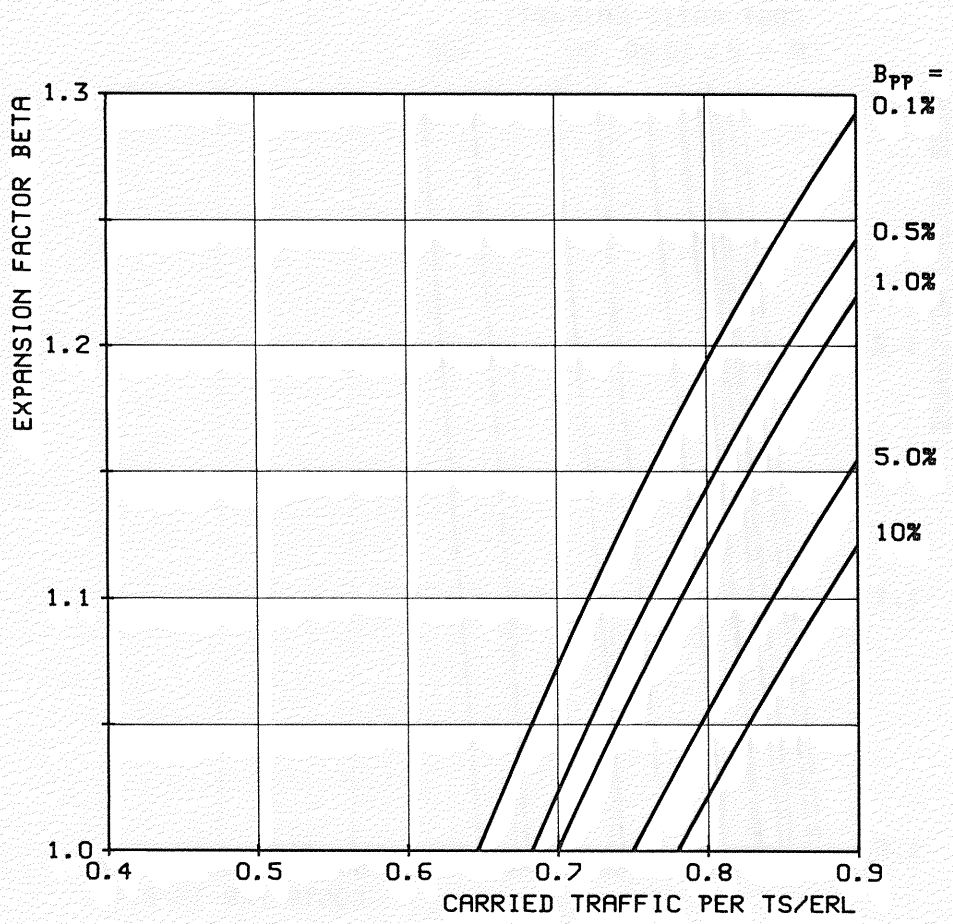


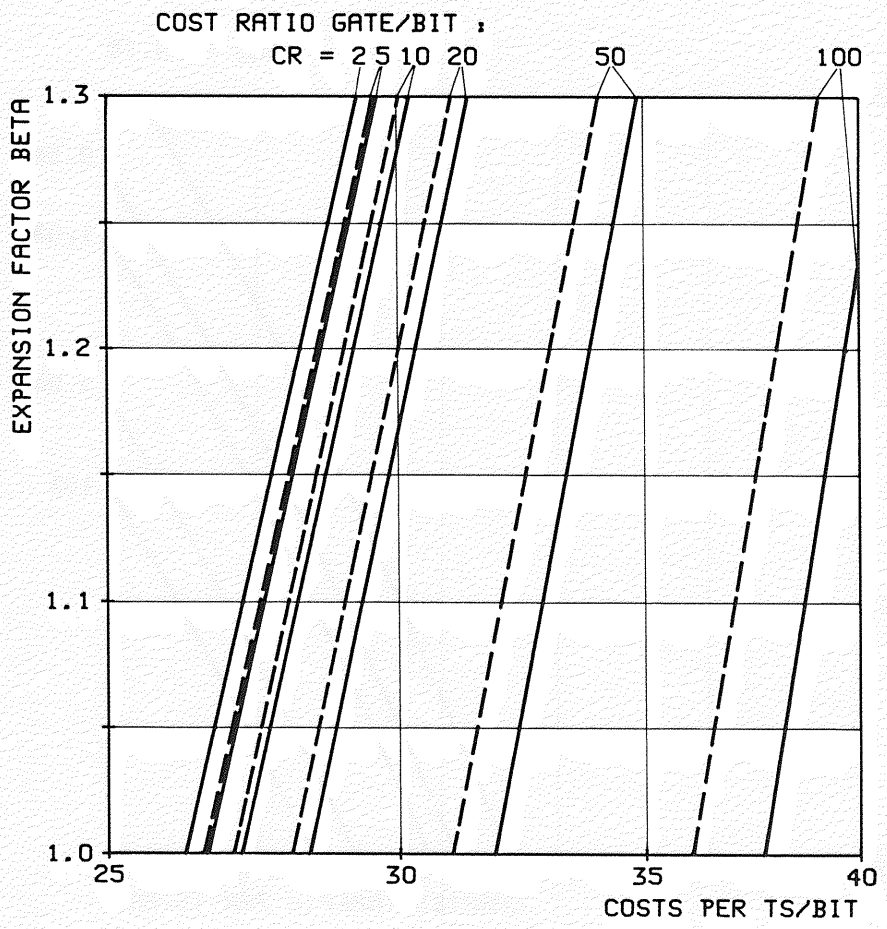


COMBINED SWITCHING 1 × 25 HW H_2 = 5 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 25 HW M = 120 --- SEPARATED SWITCHING

TSST

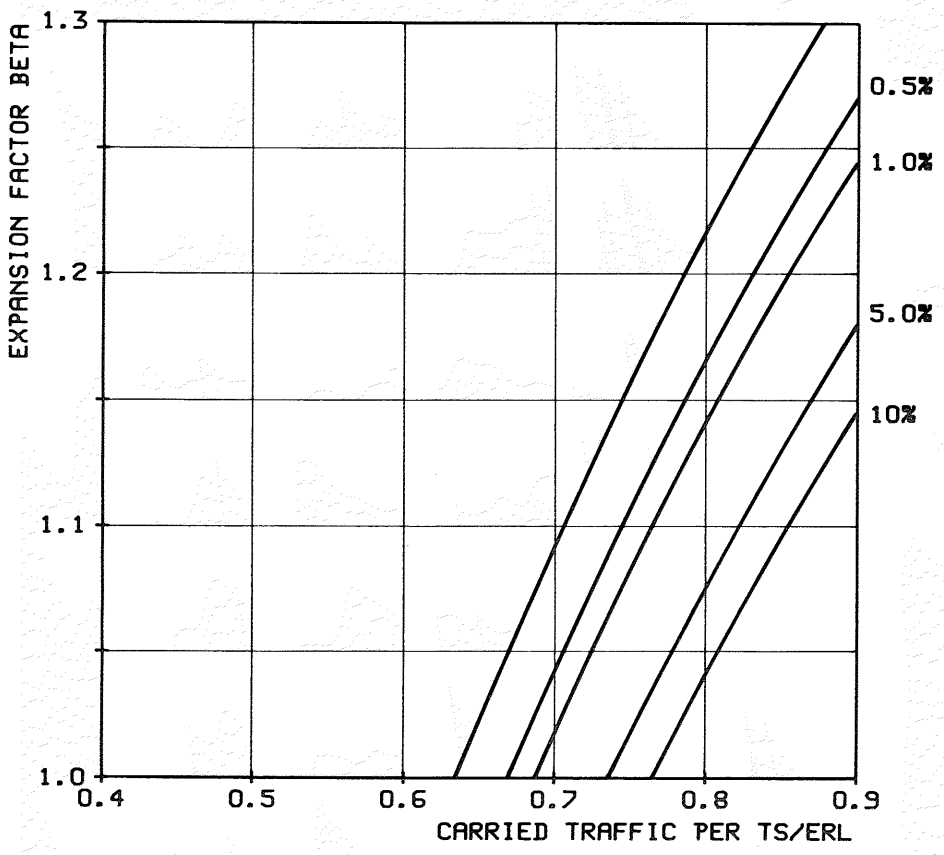


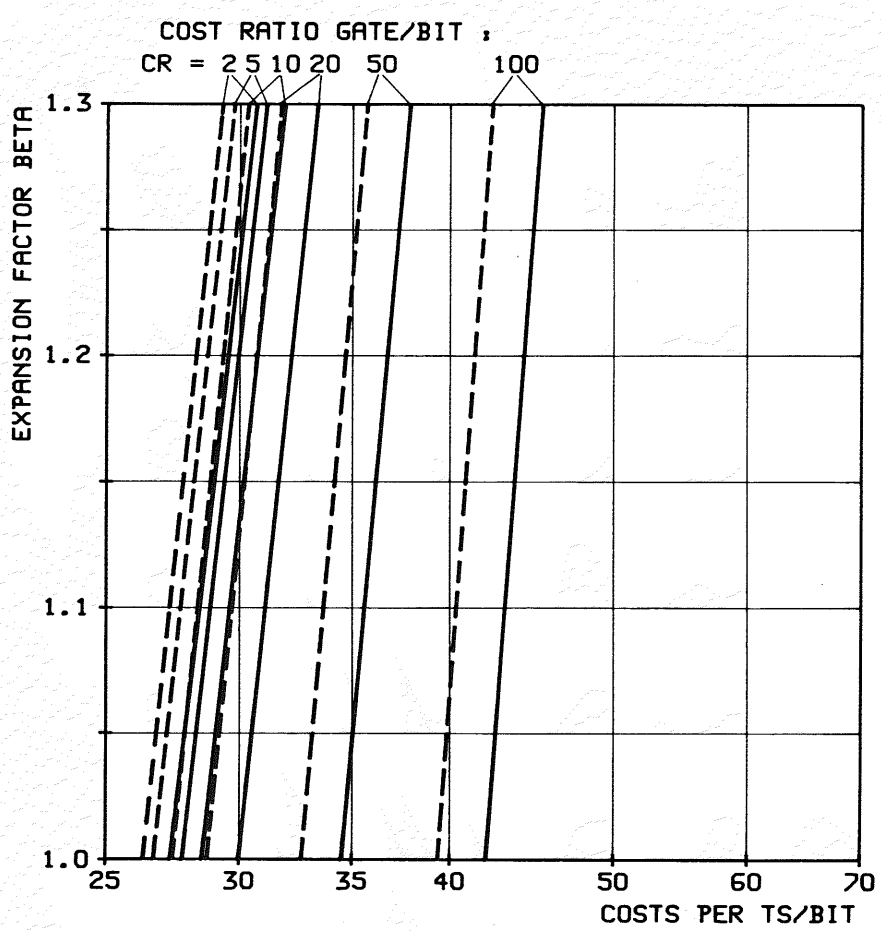


COMBINED SWITCHING 1 × 36 HW H_2 = 6 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 36 HW M = 120 --- SEPARATED SWITCHING

TSST

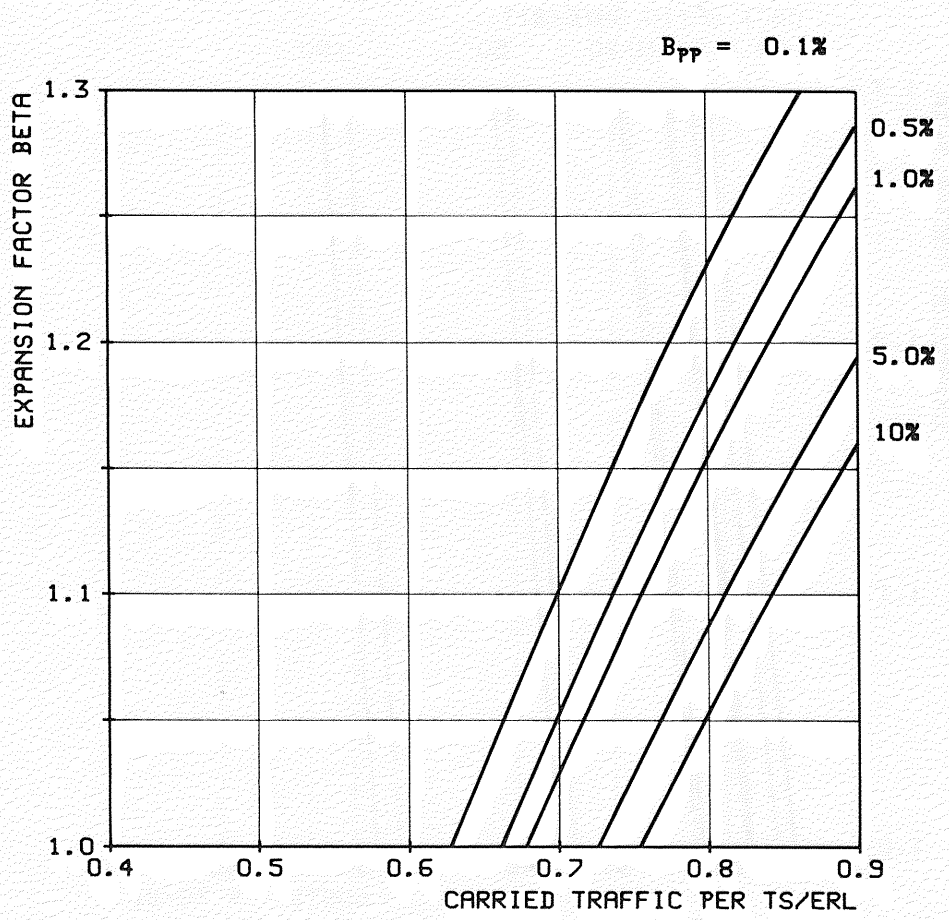


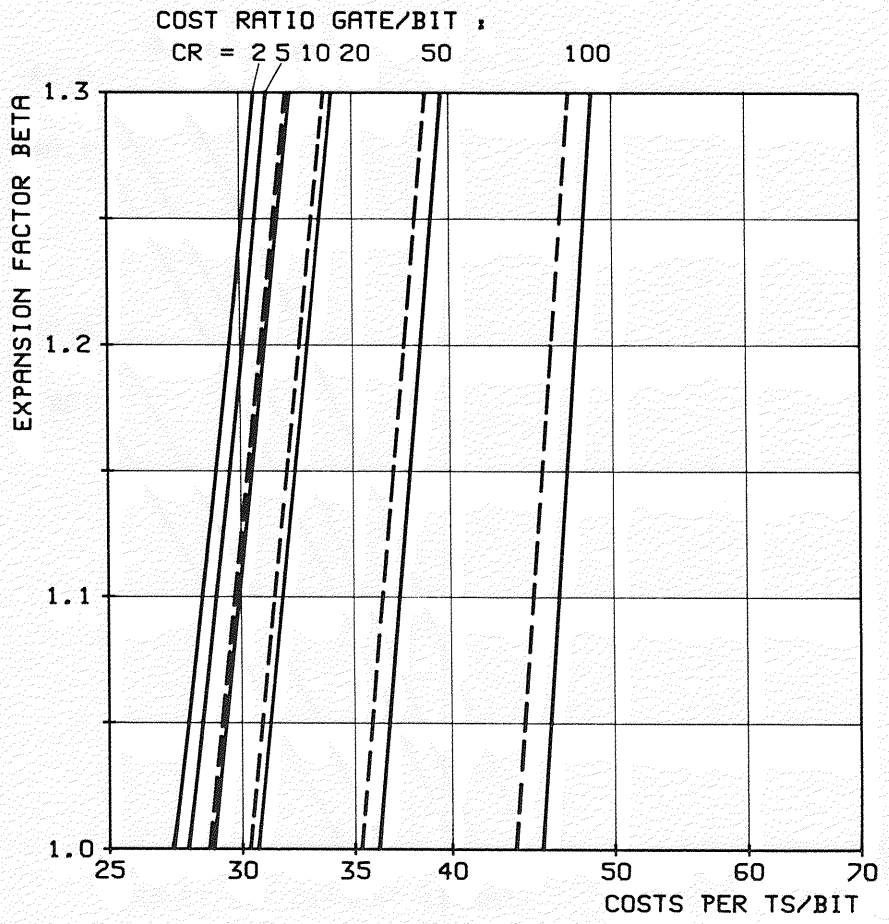


COMBINED SWITCHING 1 × 64 HW H_2 = 8 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 64 HW M = 120 --- SEPARATED SWITCHING

TSST

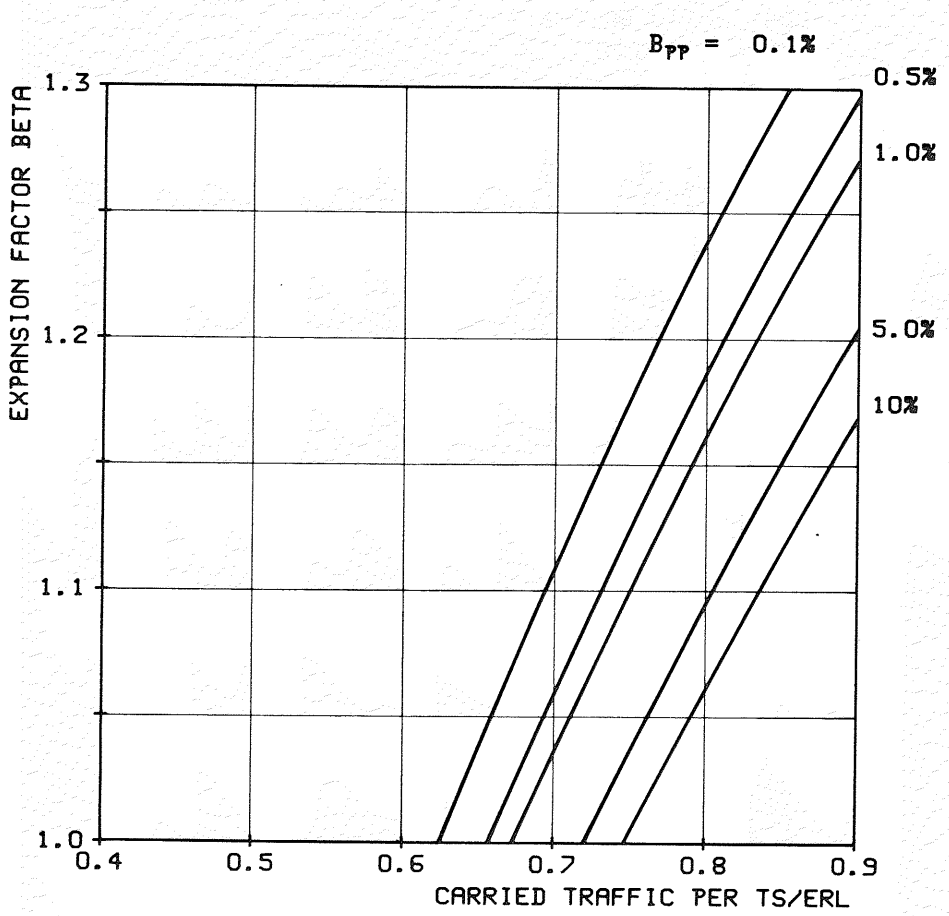


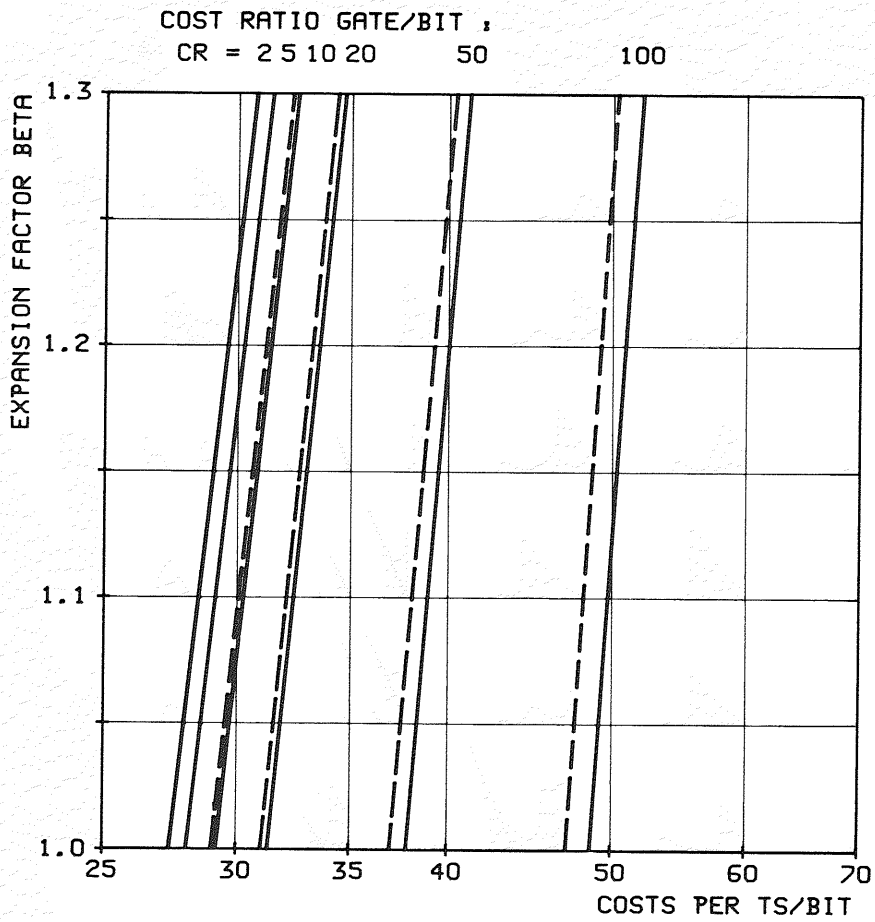


COMBINED SWITCHING 1 × 100 HW H_2 = 10 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 100 HW M = 120 --- SEPARATED SWITCHING

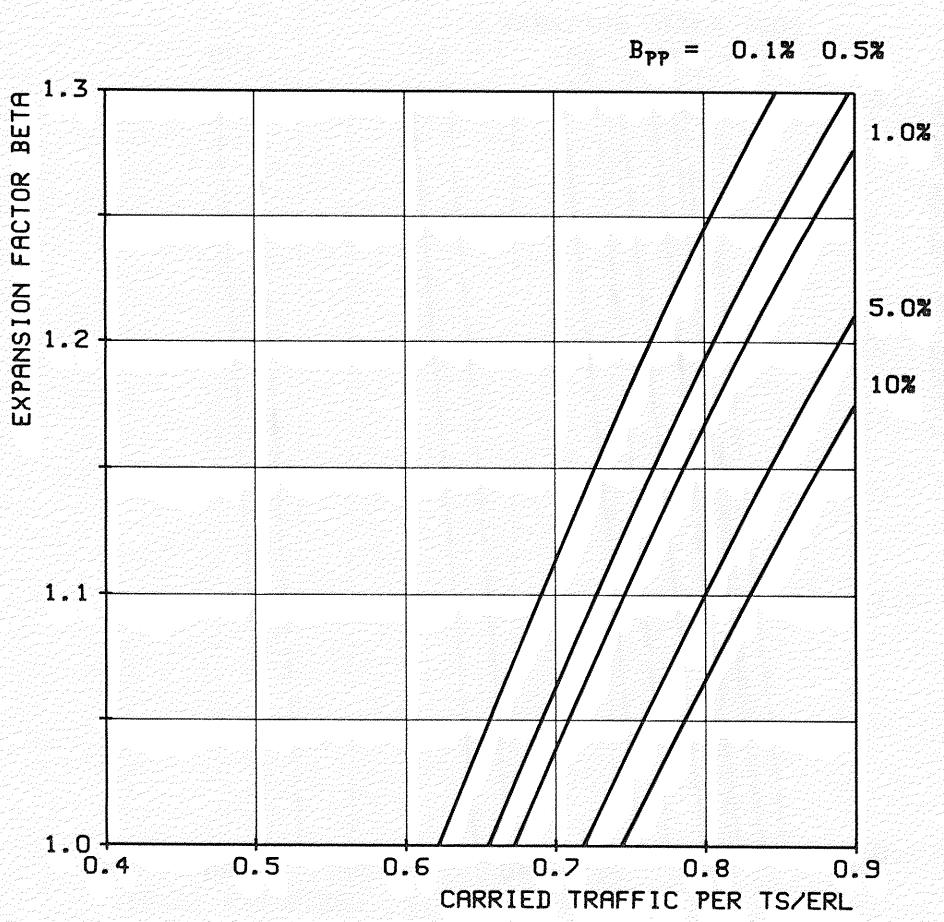
TSST

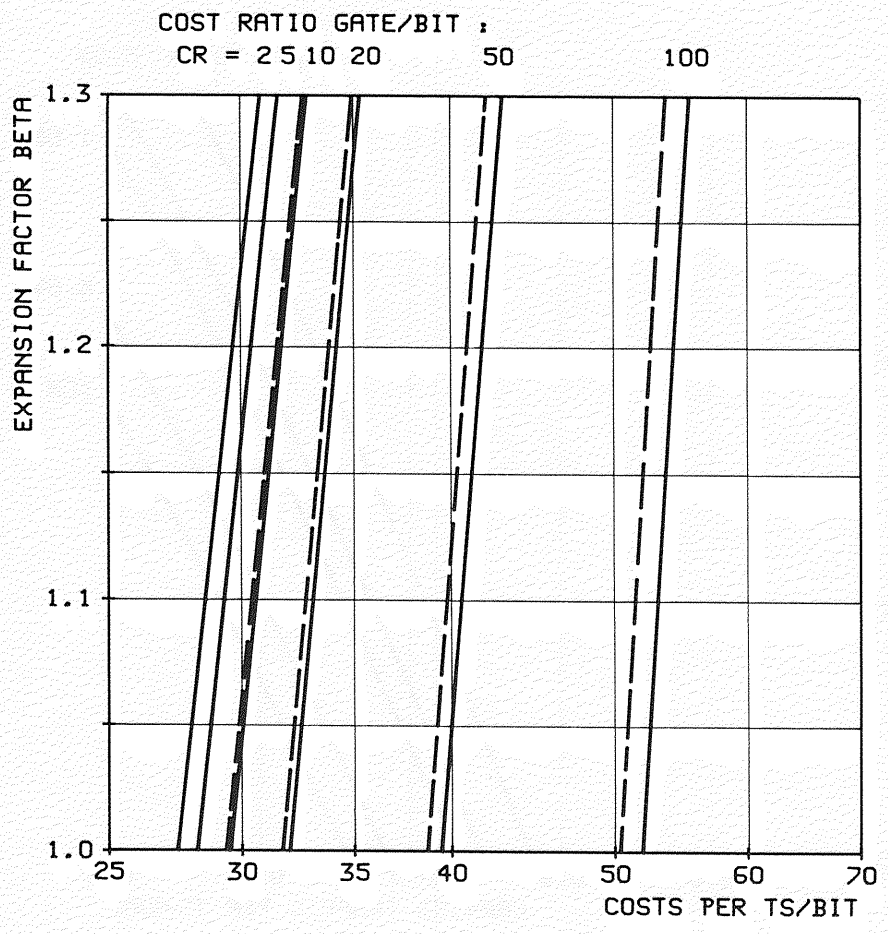




COMBINED SWITCHING 1 × 144 HW H_2 = 12 —— COMBINED SWITCHING
SEPARATED SWITCHING 2 × 144 HW M = 120 --- SEPARATED SWITCHING

TSST

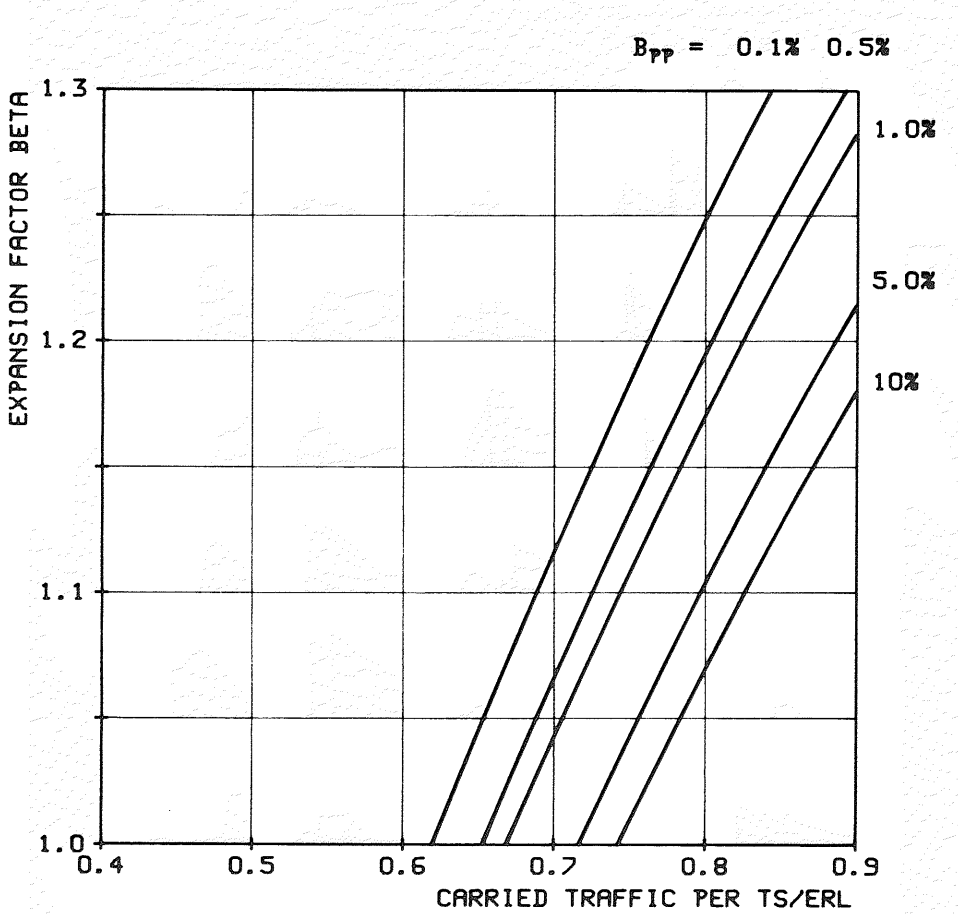


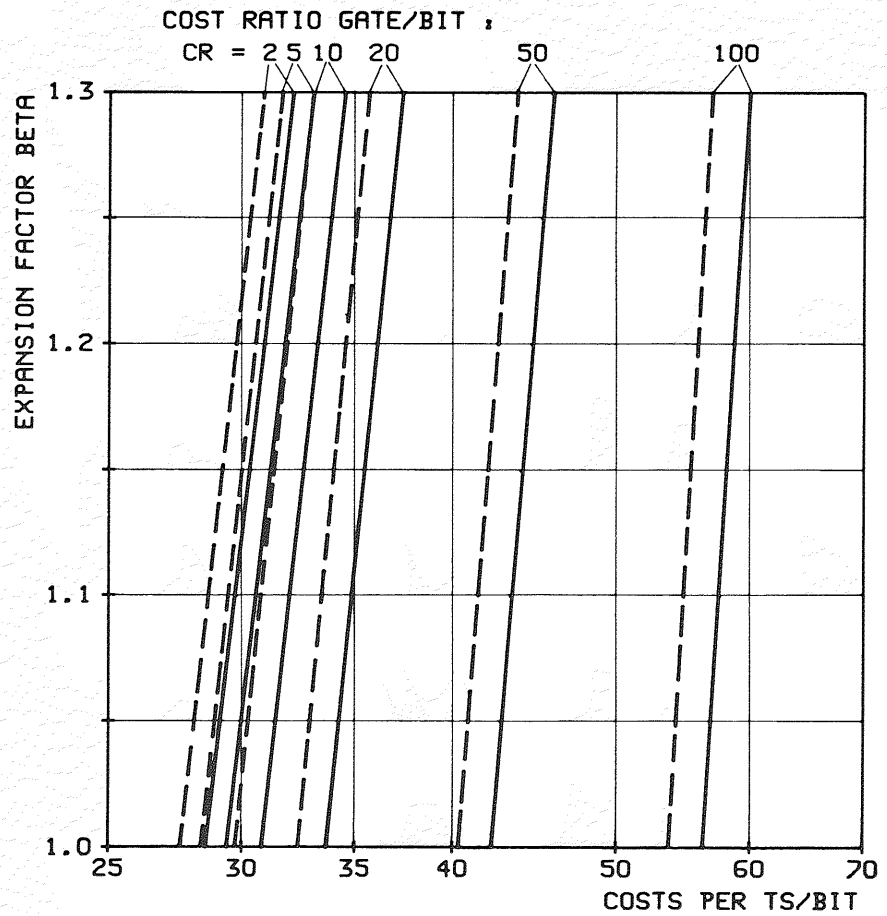


COMBINED SWITCHING 1 × 196 HW H_2 = 14 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 196 HW M = 120 --- SEPARATED SWITCHING

TSST

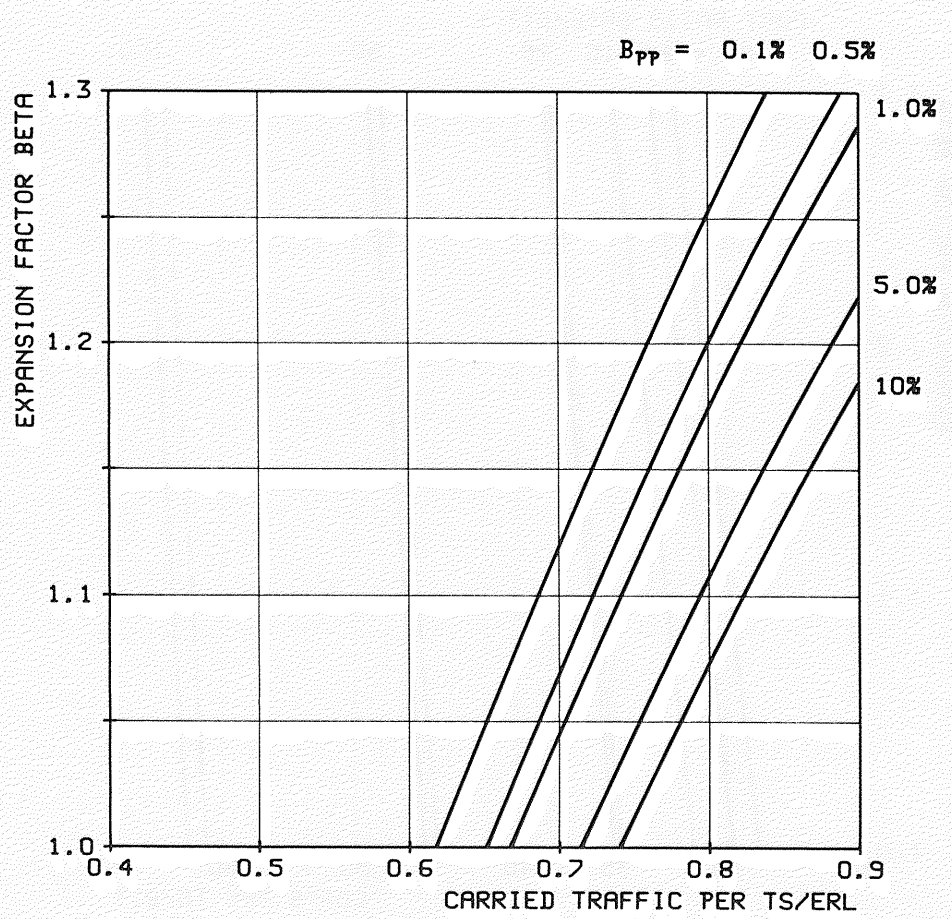


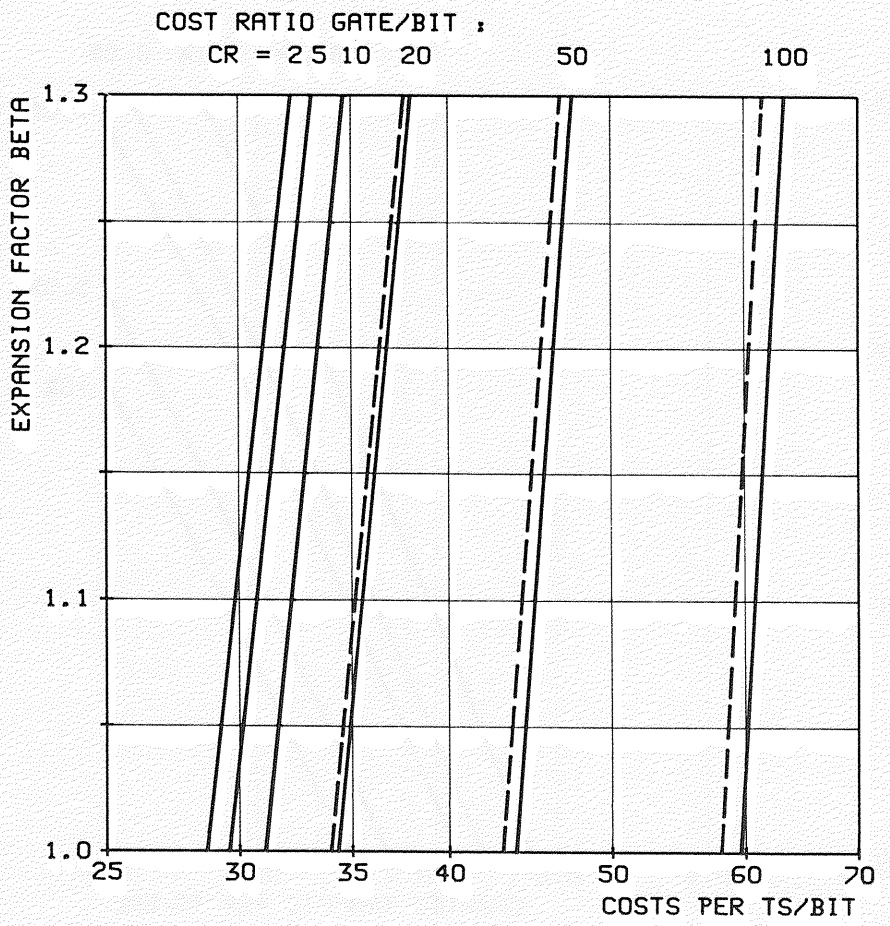


COMBINED SWITCHING 1 × 256 HW H_2 = 16 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 256 HW M = 120 --- SEPARATED SWITCHING

TSST

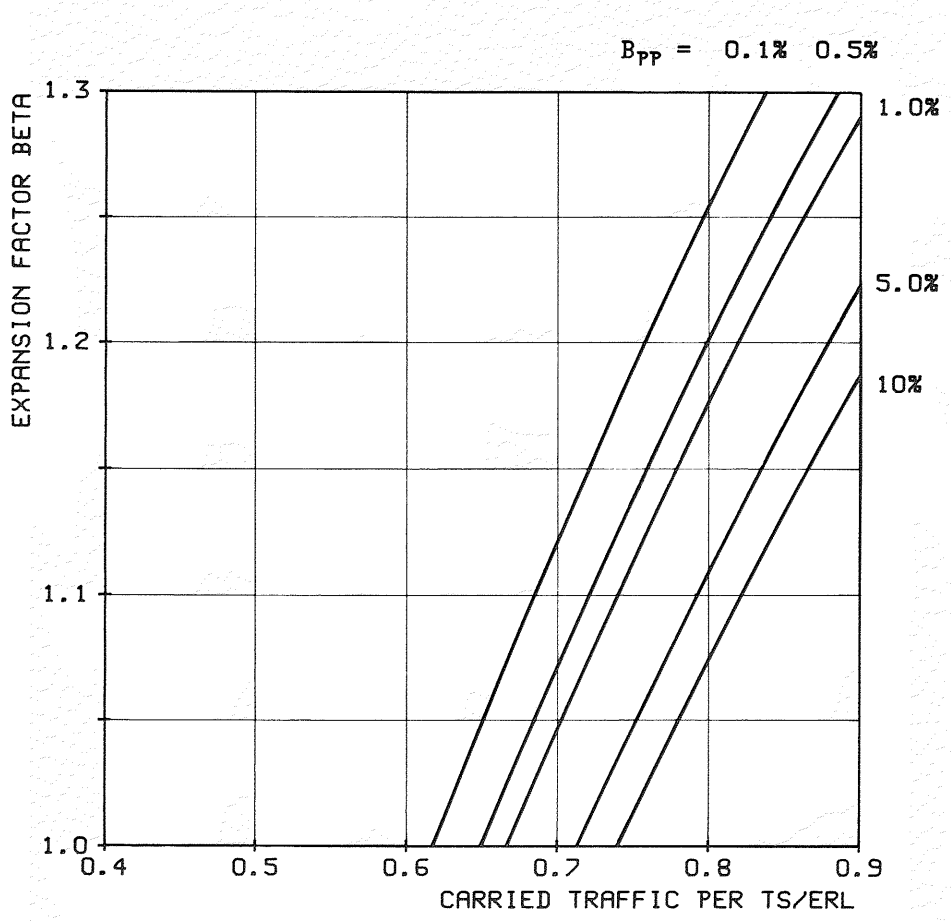


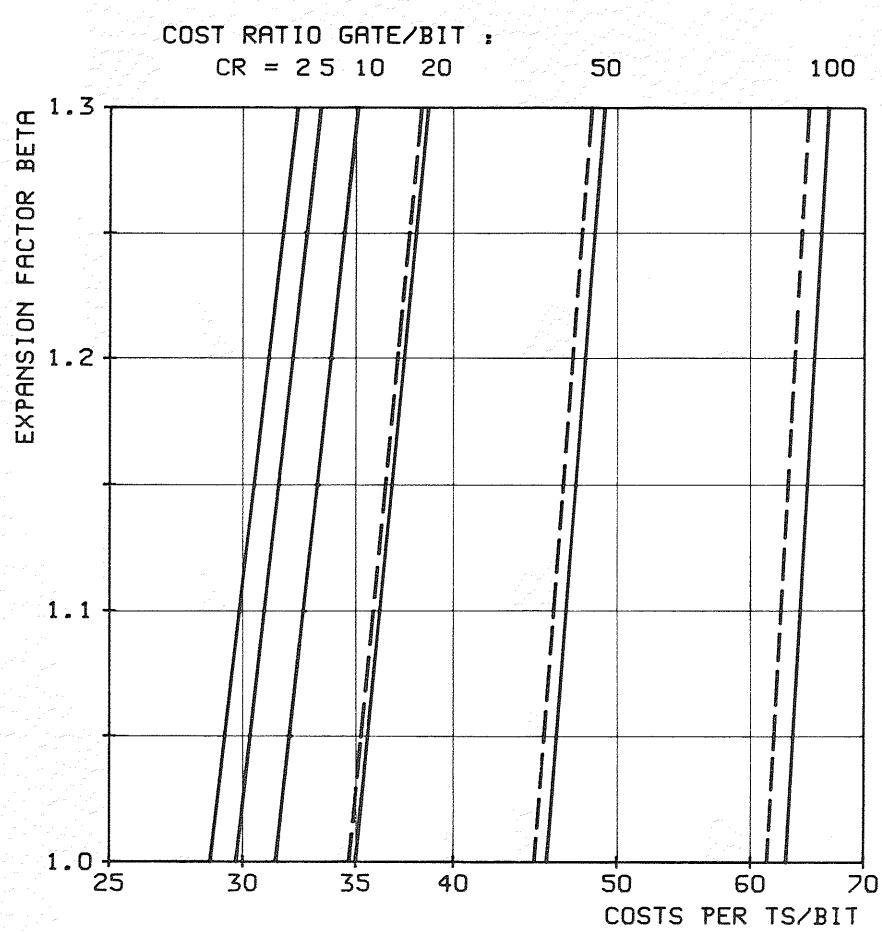


COMBINED SWITCHING 1 × 324 HW H_2 = 18 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 324 HW M = 120 --- SEPARATED SWITCHING

TSST

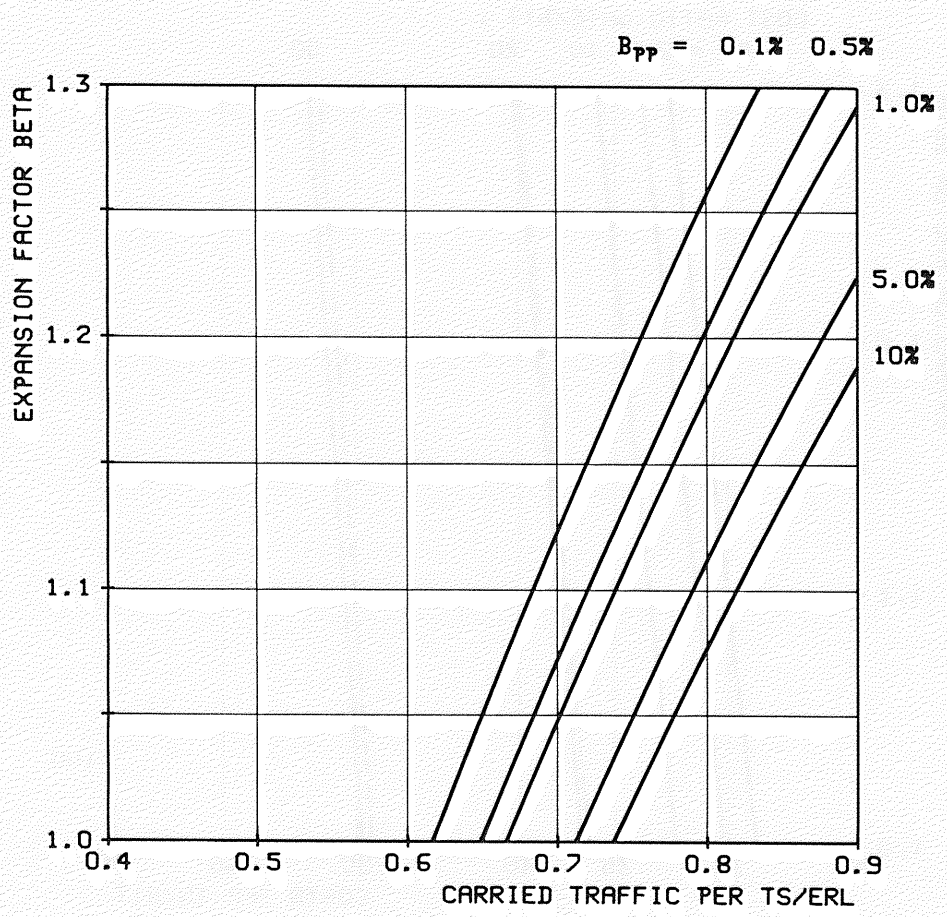


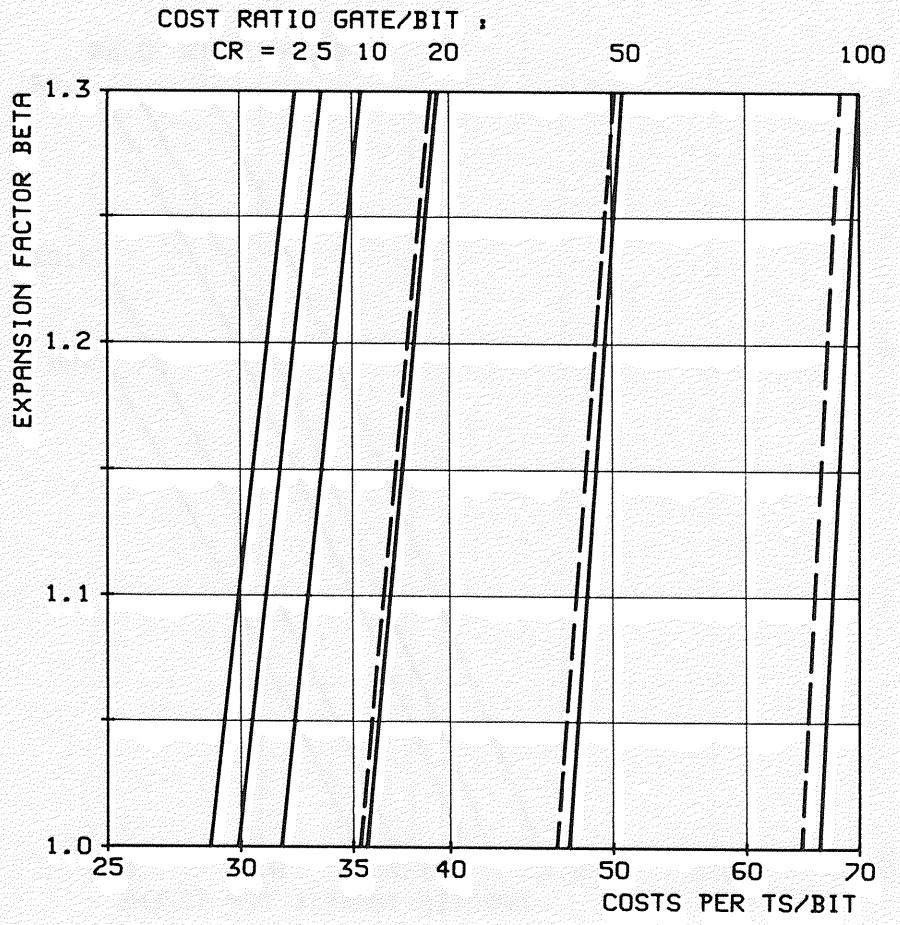


COMBINED SWITCHING 1 × 400 HW H_2 = 20 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 400 HW M = 120 --- SEPARATED SWITCHING

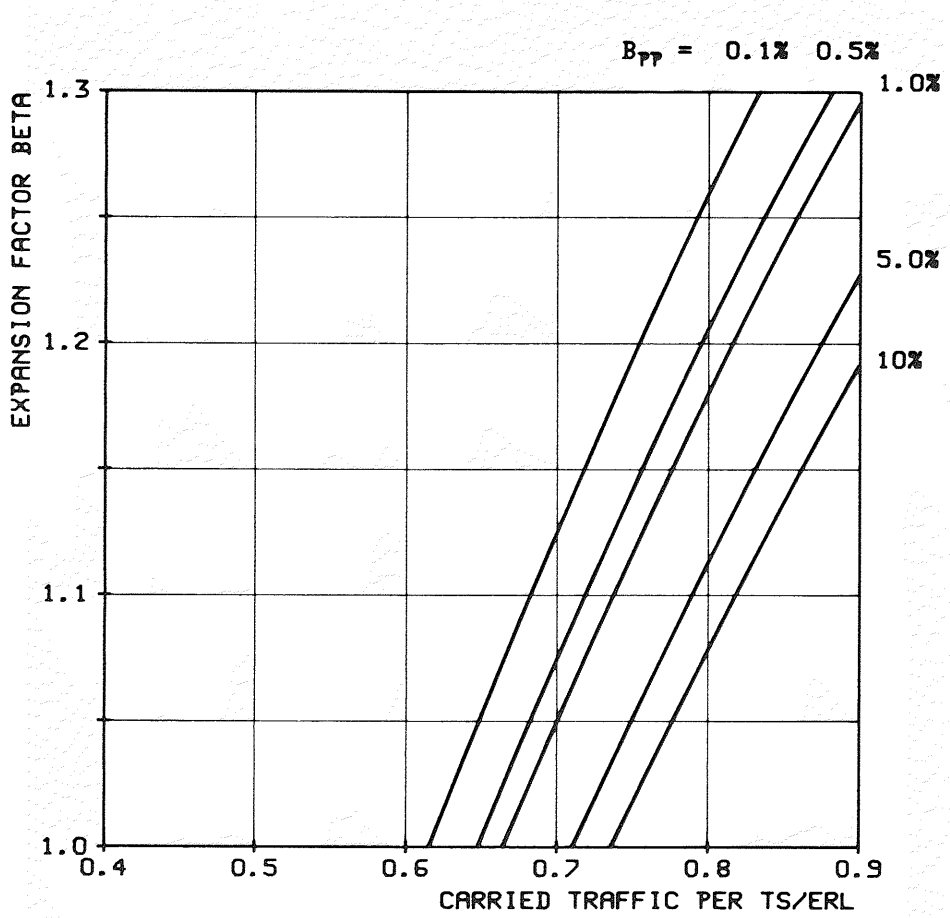
TSST

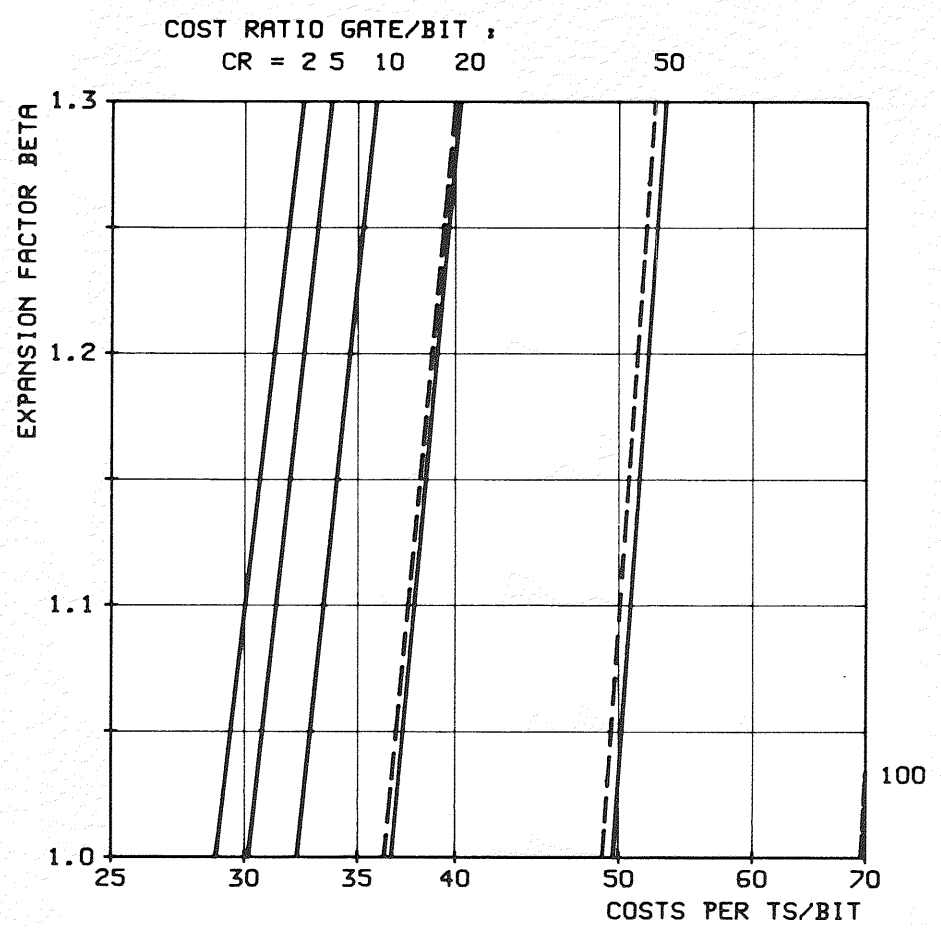




COMBINED SWITCHING	1 × 484 HW	H_2 = 22	—— COMBINED SWITCHING
SEPARATED SWITCHING	2 × 484 HW	M = 120	--- SEPARATED SWITCHING

TSST

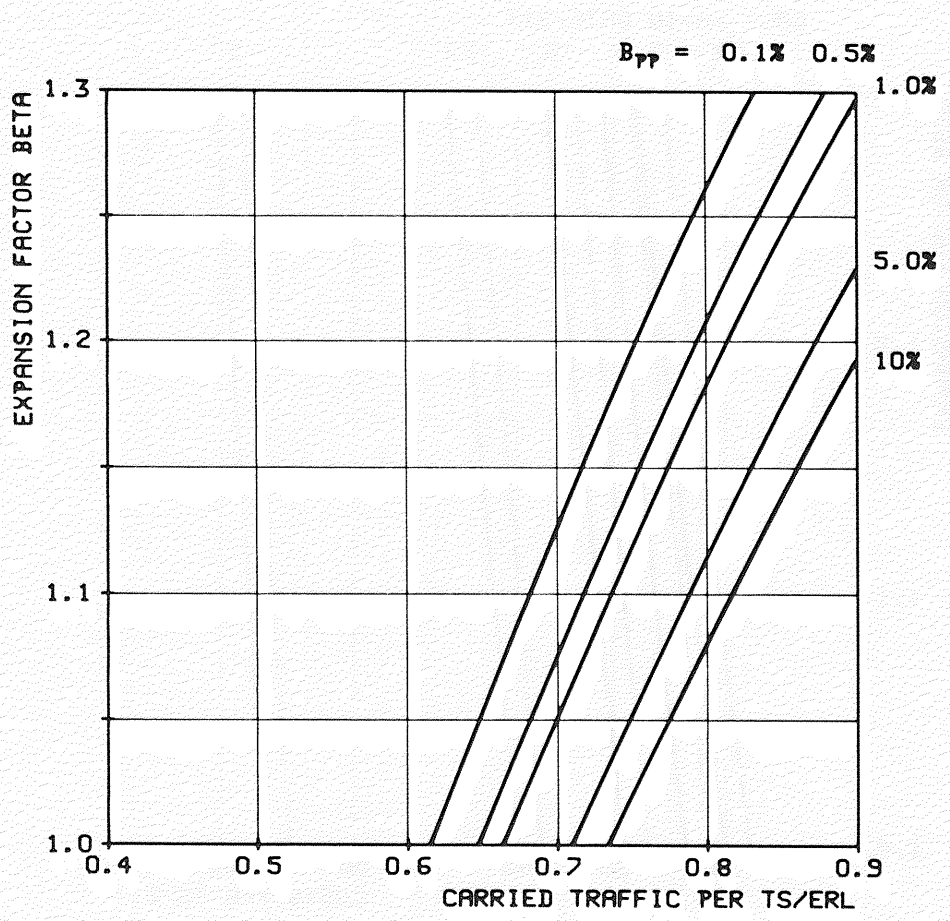


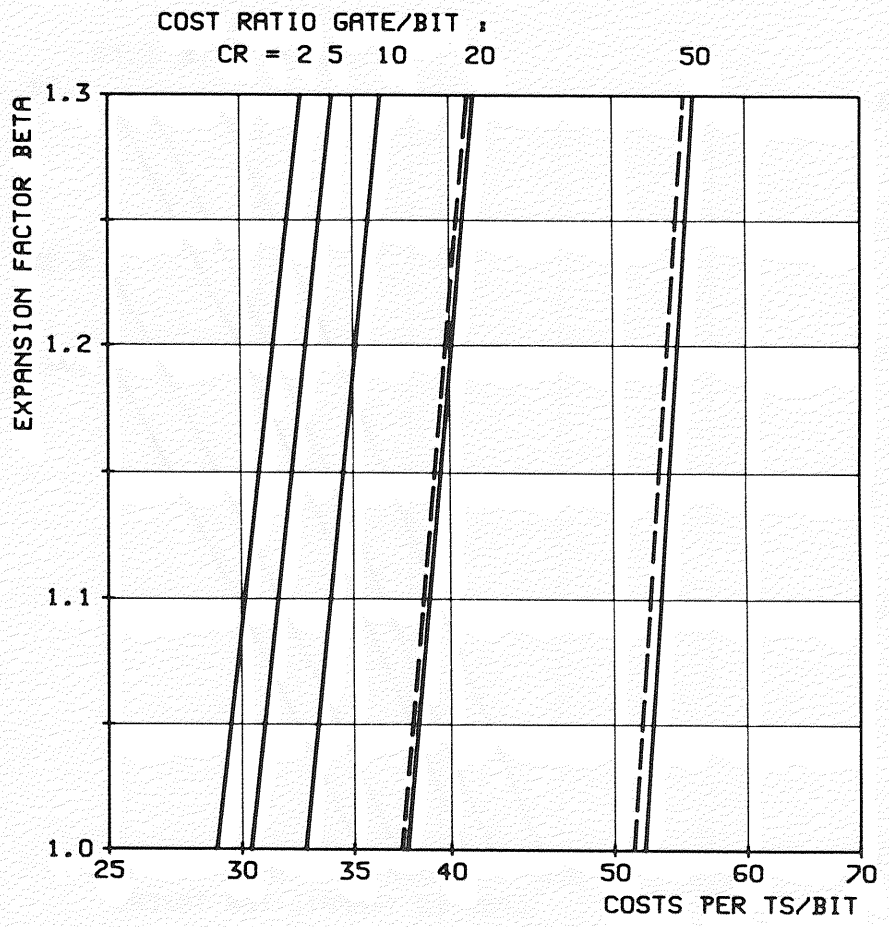


COMBINED SWITCHING 1 × 625 HW H_2 = 25 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 625 HW M = 120 --- SEPARATED SWITCHING

TSST

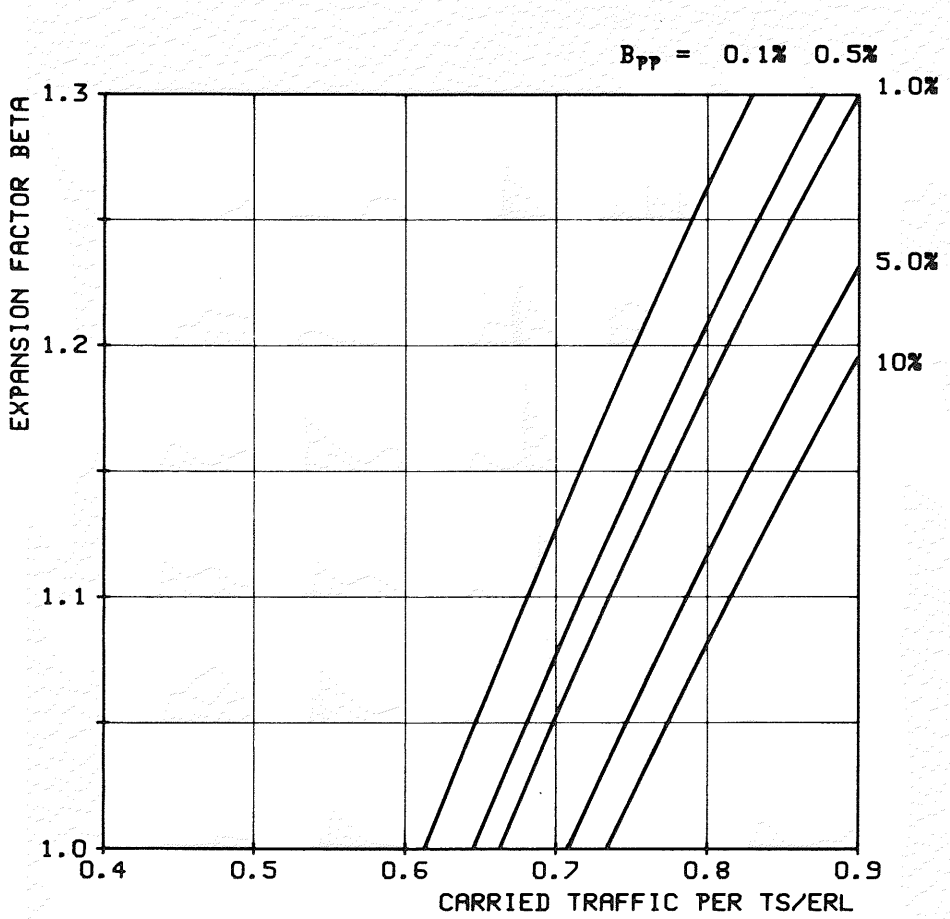


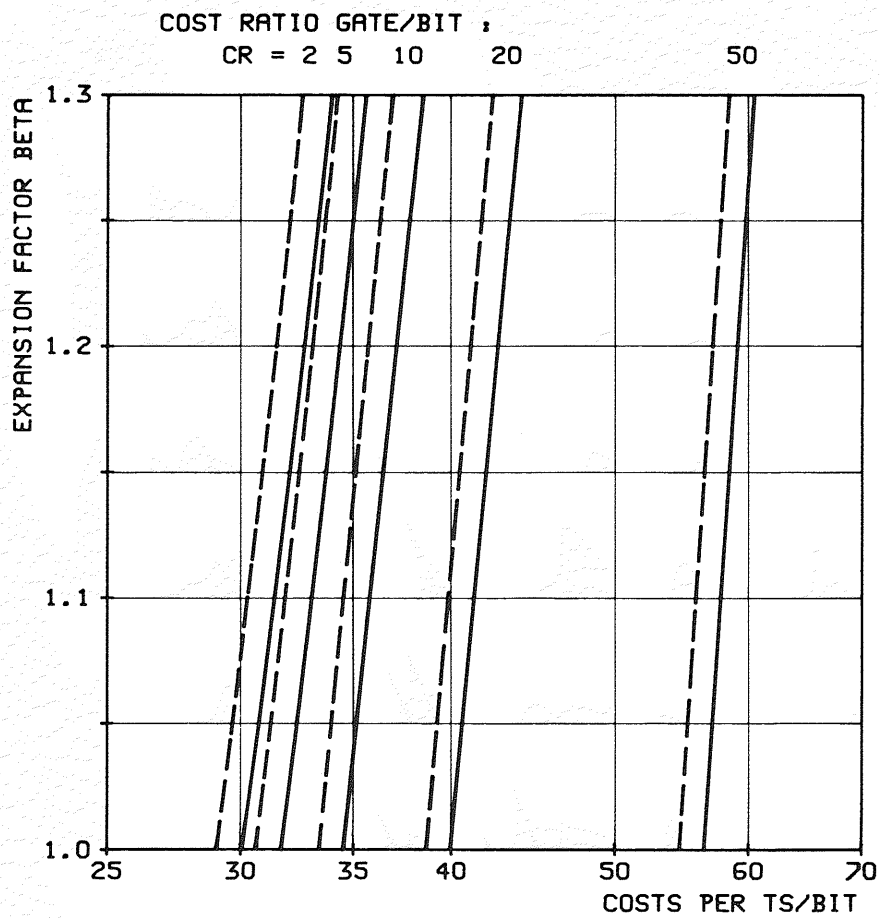


COMBINED SWITCHING	1 × 784 HW	H_2 = 28	—— COMBINED SWITCHING
SEPARATED SWITCHING	2 × 784 HW	M = 120	--- SEPARATED SWITCHING

-CHART 100-

TSST





COMBINED SWITCHING 1 × 1024 HW H_2 = 32 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 1024 HW M = 120 --- SEPARATED SWITCHING

PCM SWITCHING ARRAY : TSSST

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 4, 9, 16, 25, 36, 64, 100, 144, 196, 256, 324, 400, 484, 625, 784, 1024,

SEPARATED SWITCHING : HW = 8, 18, 32, 50, 72, 128, 200, 288, 392, 512, 648, 800, 968, 1250, 1568, 2048,

TIME-SLOTS (TS) PER HW : M = 120 TS

POINT-TO-POINT LOSS, PCT1 : B_{PP} = 0.1, 0.5, 1.0, 5.0, 10.0%

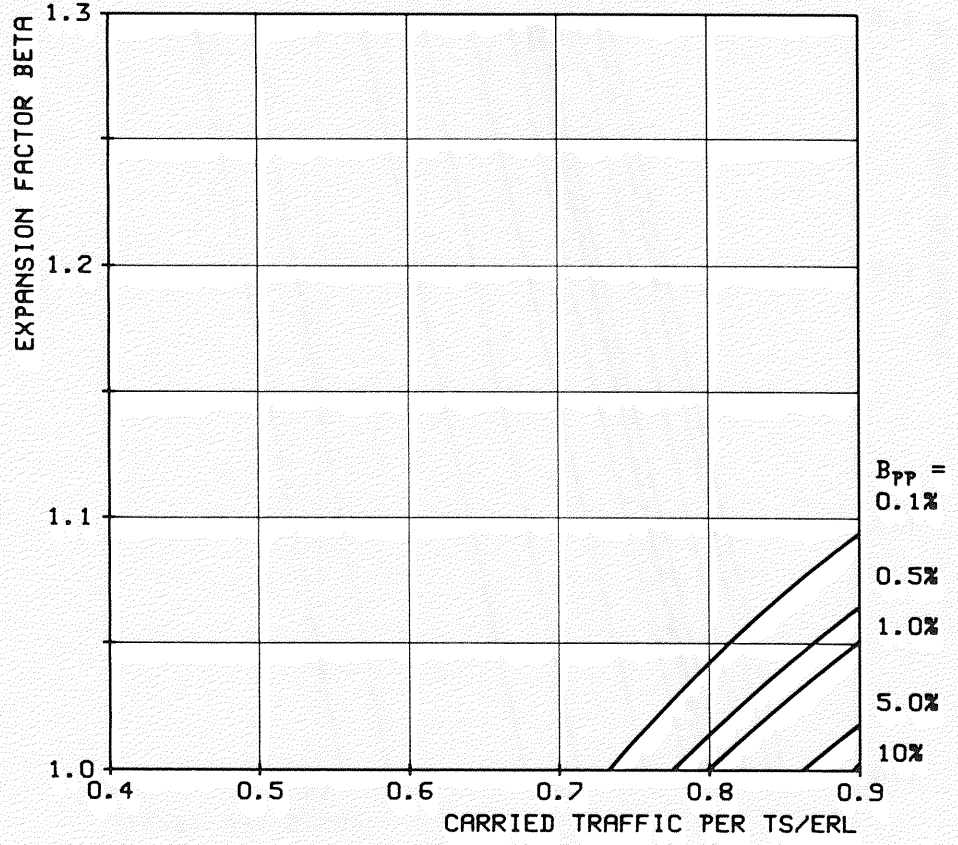
COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

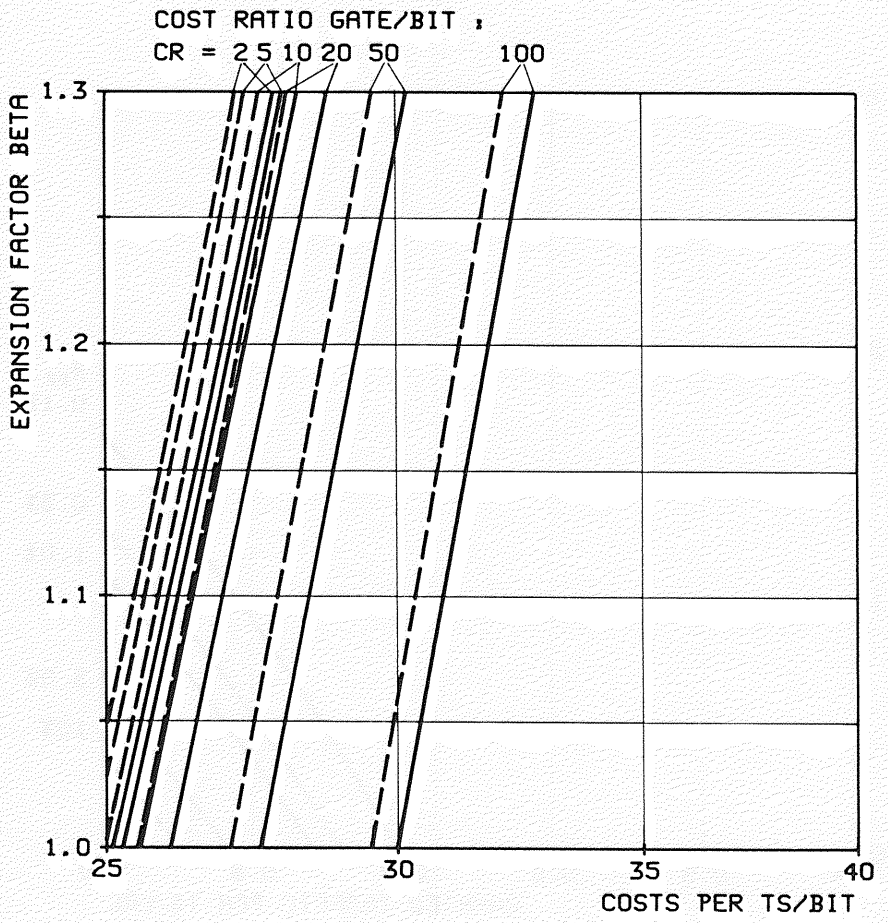
BLOCK SIZE

COMBINED SWITCHING : $H_2 = \sqrt{HW}$

SEPARATED SWITCHING : $H_2 = \sqrt{HW/2}$

TSSST



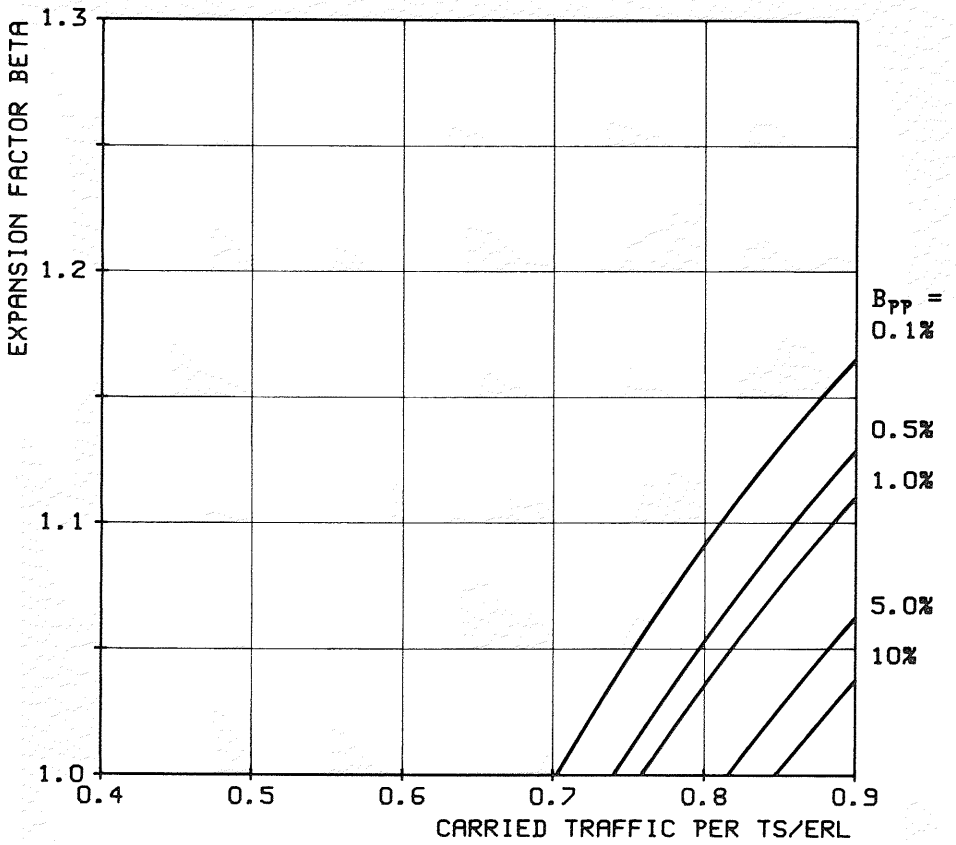


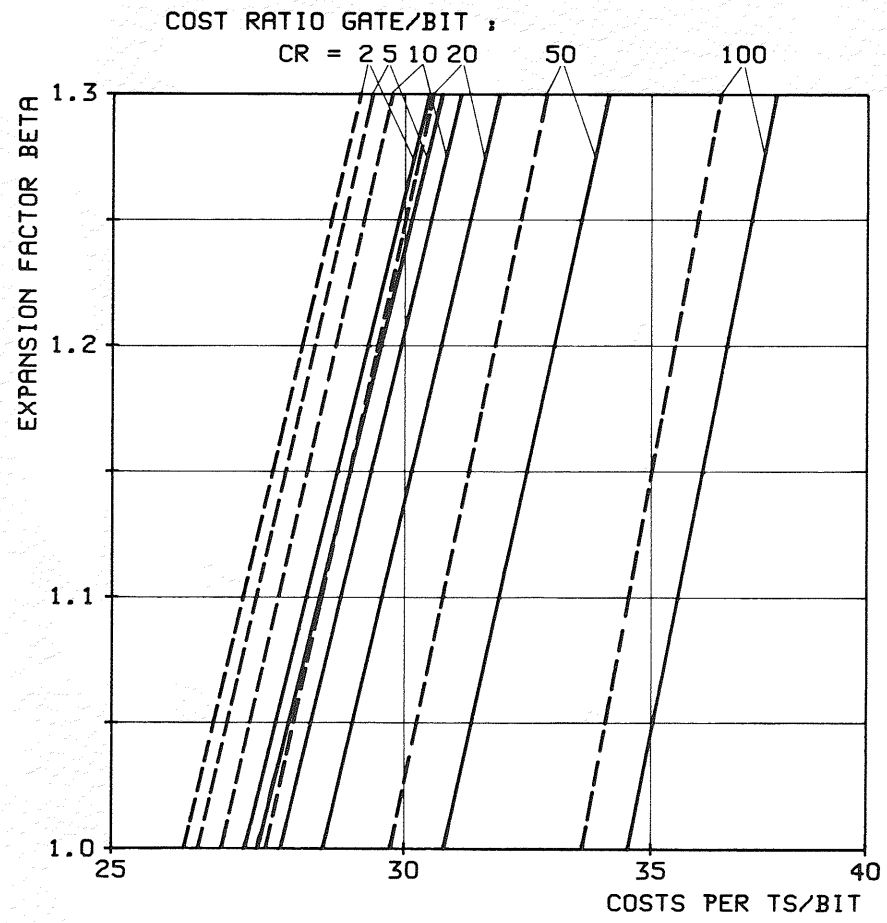
COMBINED SWITCHING 1 × 4 HW H_2 = 2
SEPARATED SWITCHING 2 × 4 HW M = 120

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

-CHART 102-

TSSST

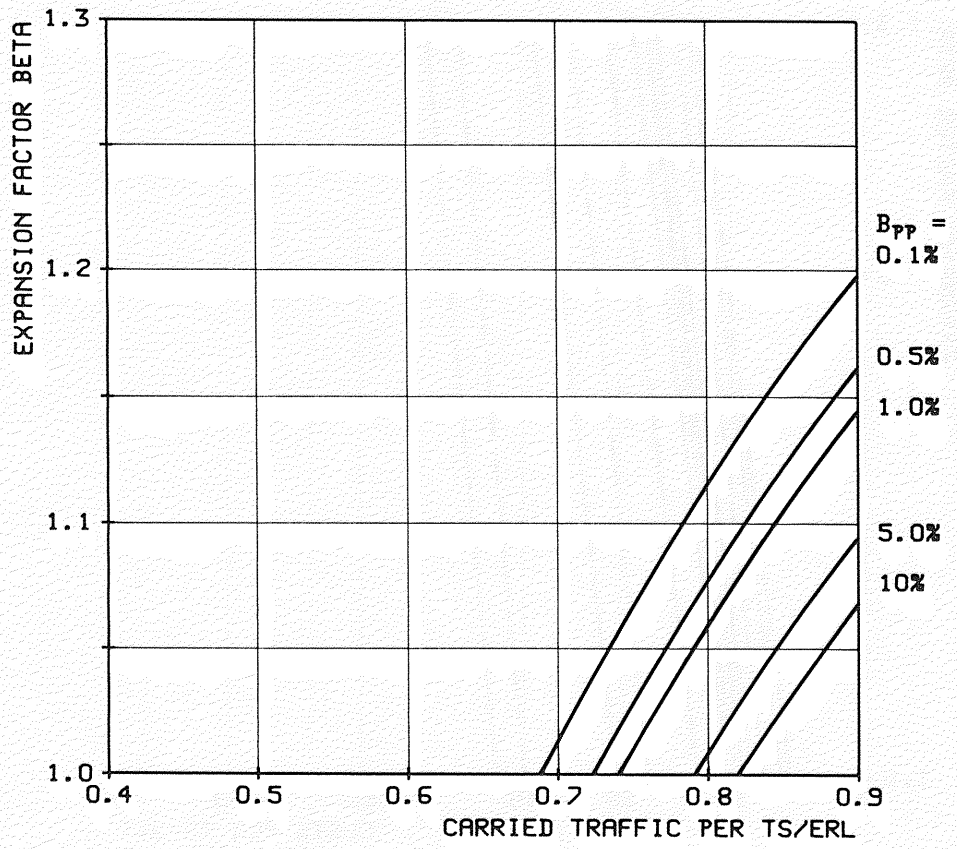


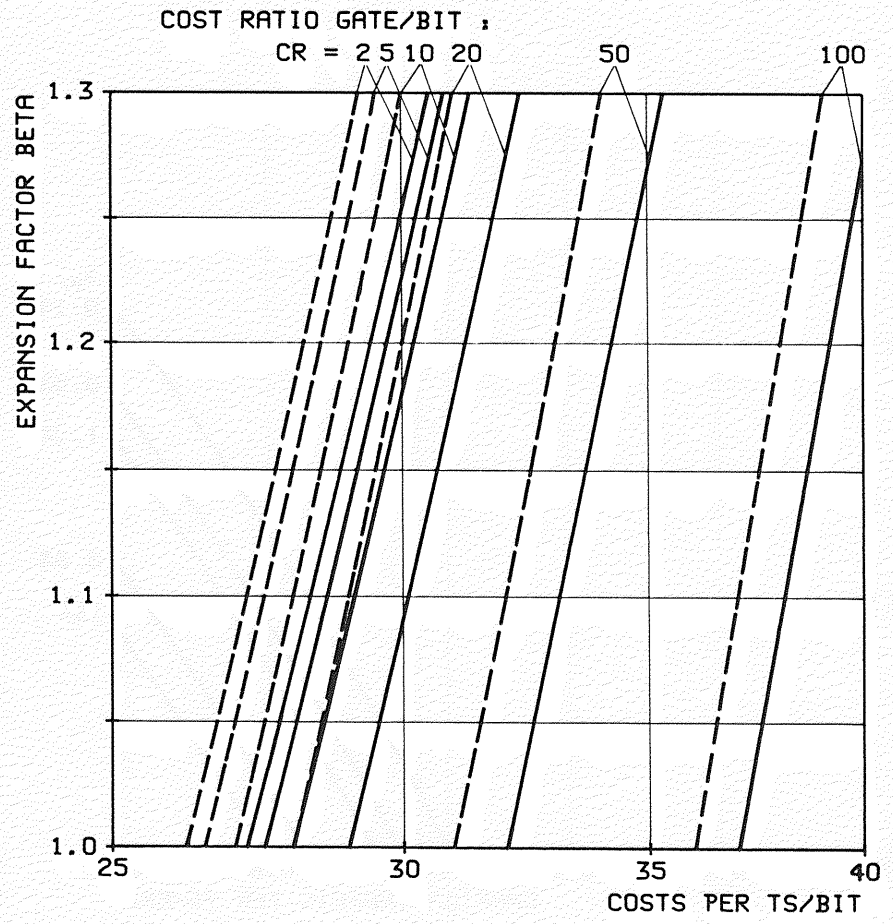


COMBINED SWITCHING 1 × 9 HW H_2 = 3
SEPARATED SWITCHING 2 × 9 HW M = 120

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

TSSST





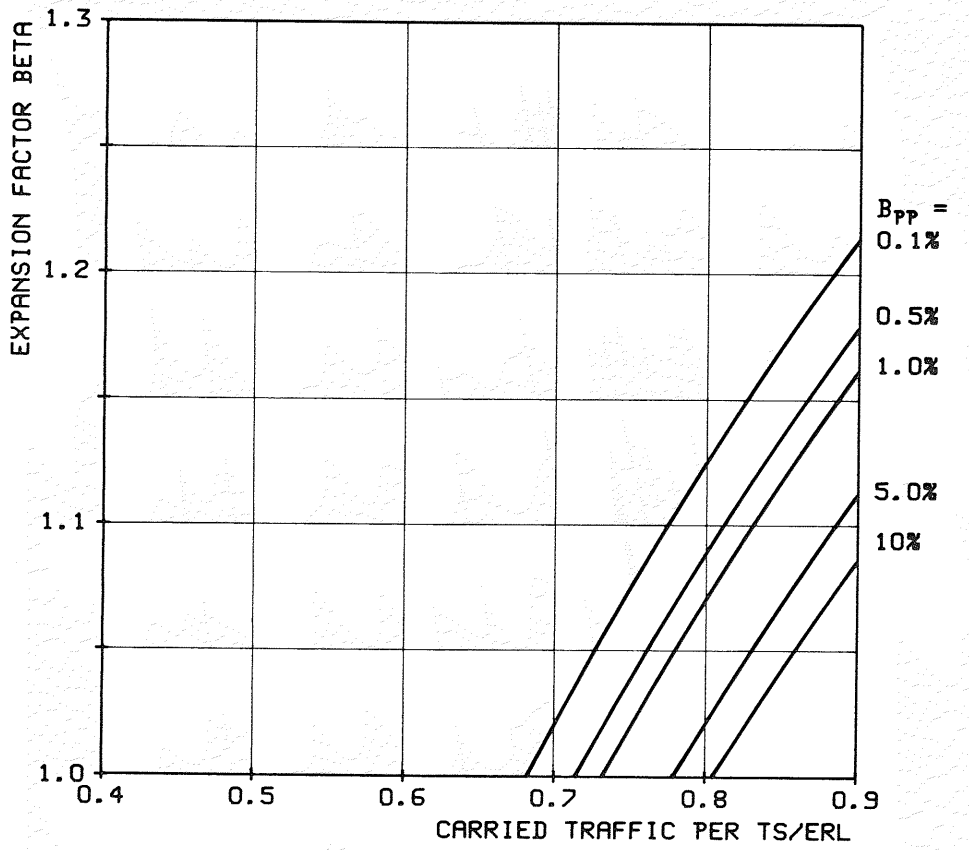
COMBINED SWITCHING 1 × 16 HW H_2 = 4

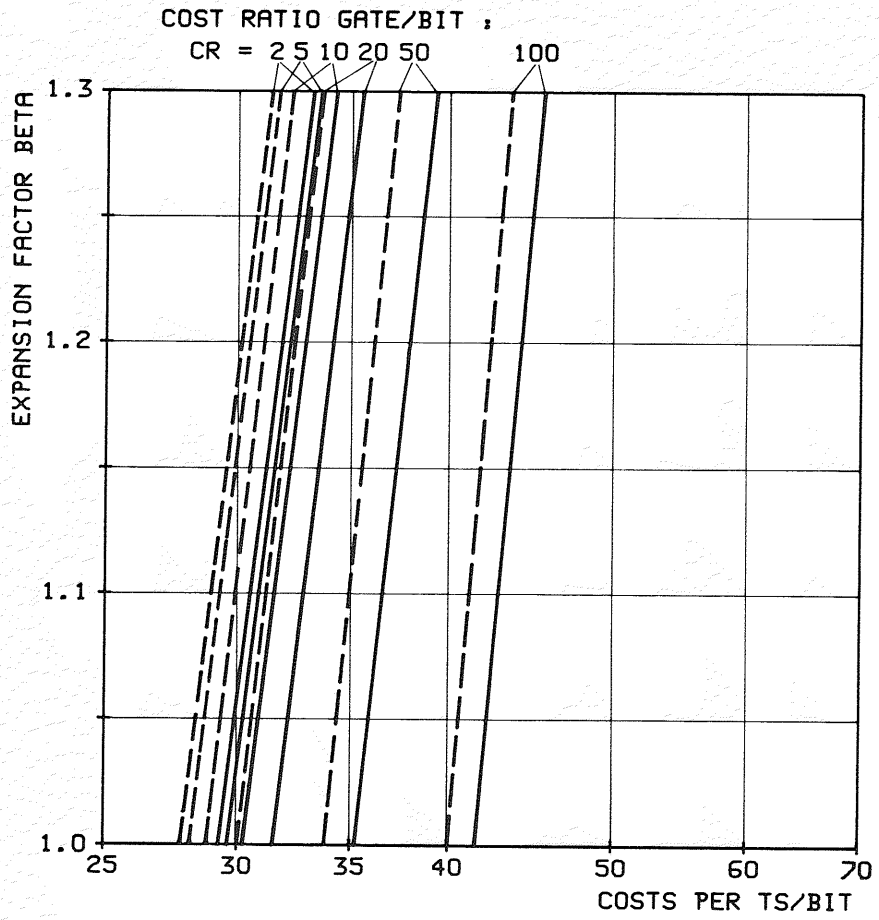
SEPARATED SWITCHING 2 × 16 HW M = 120

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

TSSST

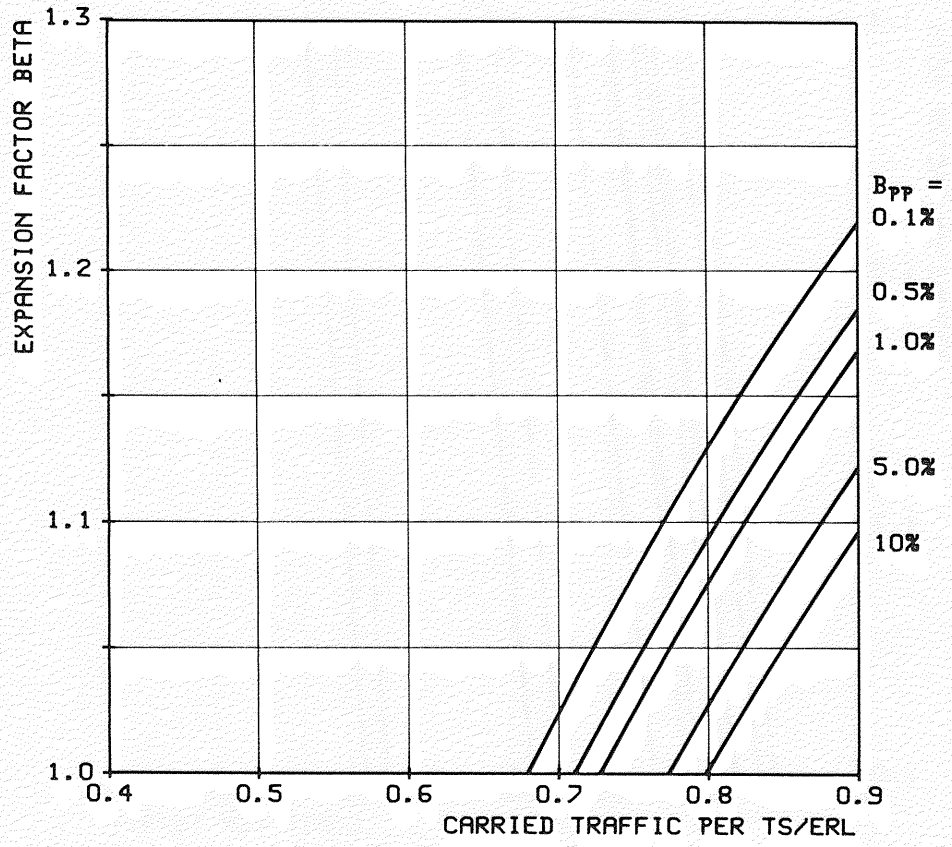


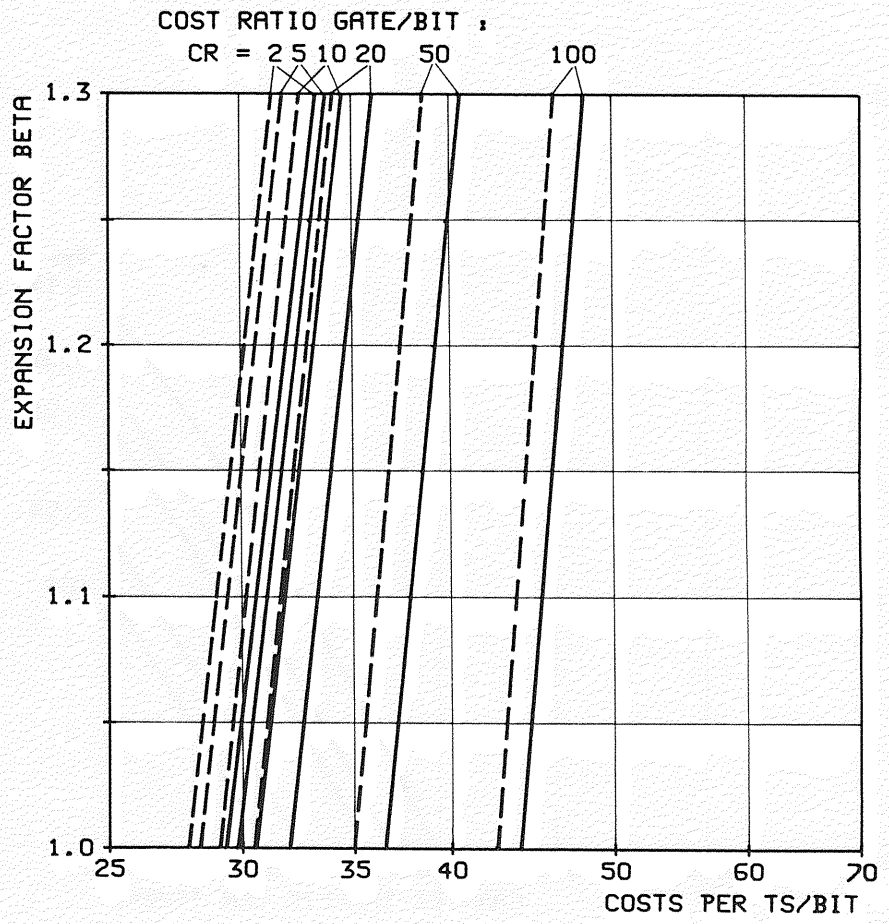


COMBINED SWITCHING 1 × 25 HW H_2 = 5
SEPARATED SWITCHING 2 × 25 HW M = 120

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

TSSST

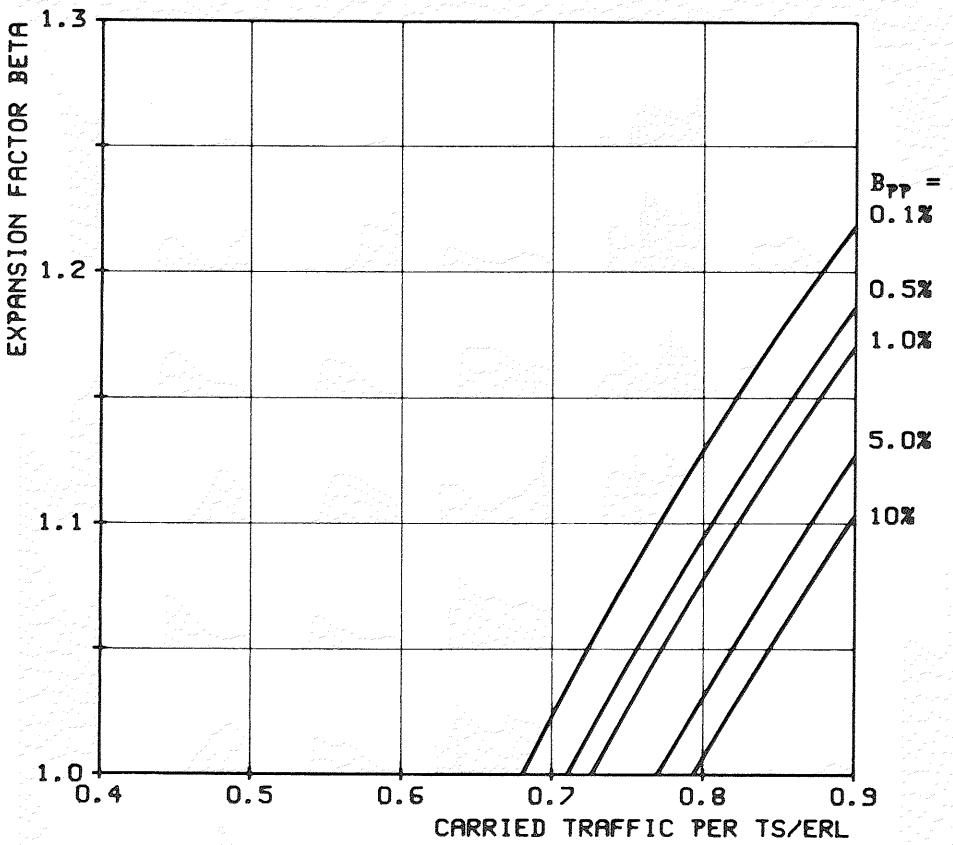


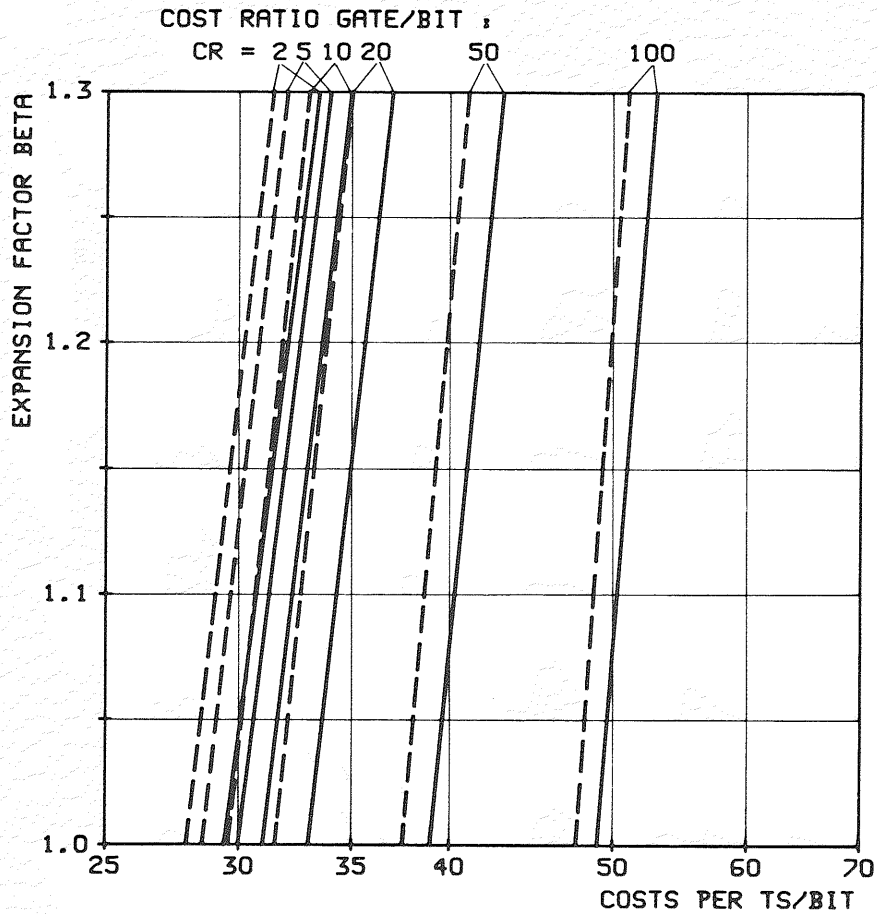


COMBINED SWITCHING 1 × 36 HW H_2 = 6
SEPARATED SWITCHING 2 × 36 HW M = 120

—— COMBINED SWITCHING
--- SEPARATED SWITCHING

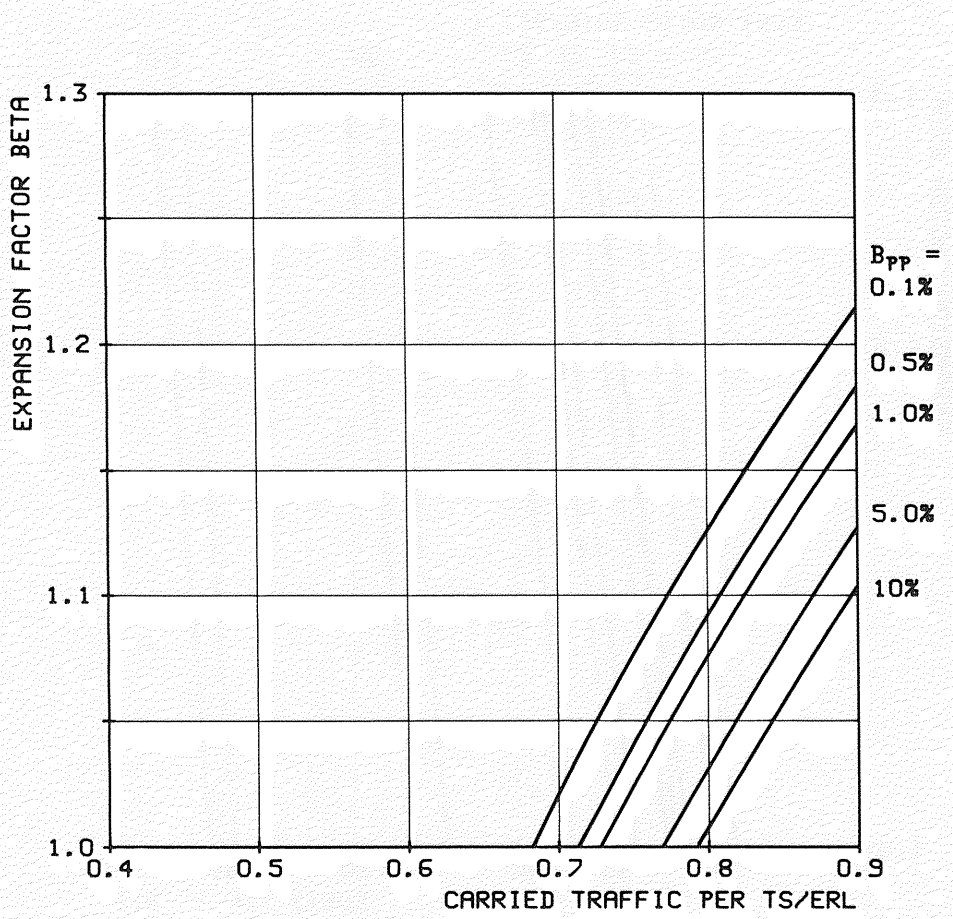
TSSST

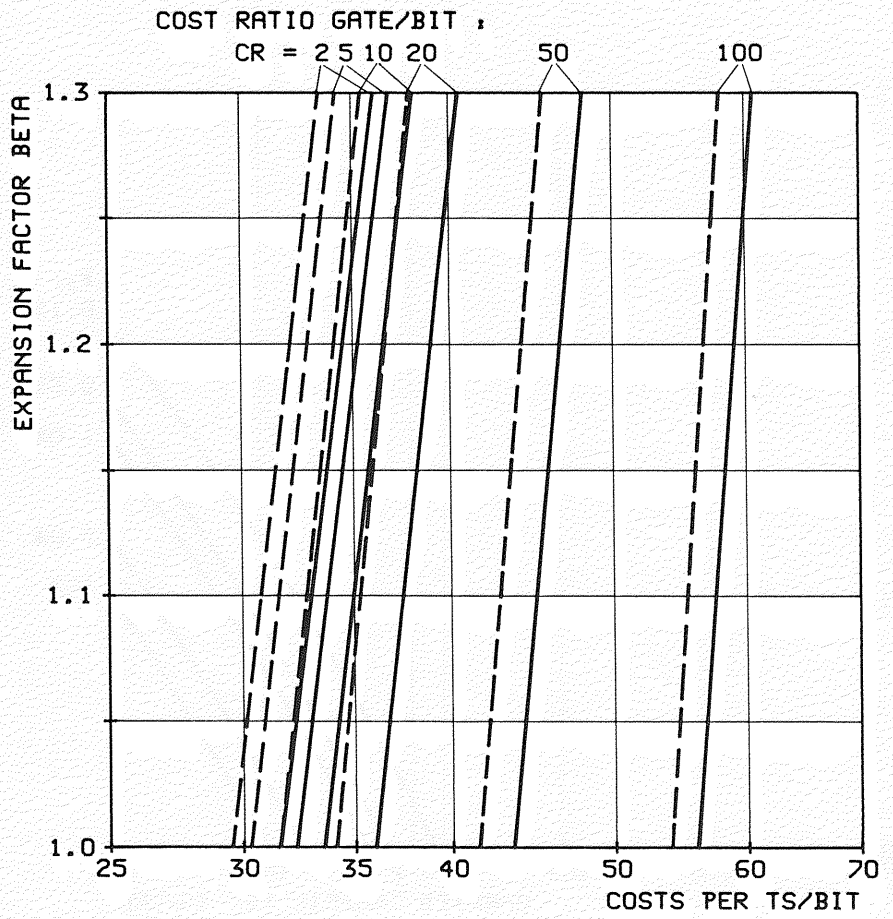




COMBINED SWITCHING 1 × 64 HW H_2 = 8 —— COMBINED SWITCHING
SEPARATED SWITCHING 2 × 64 HW M = 120 --- SEPARATED SWITCHING

TSSST

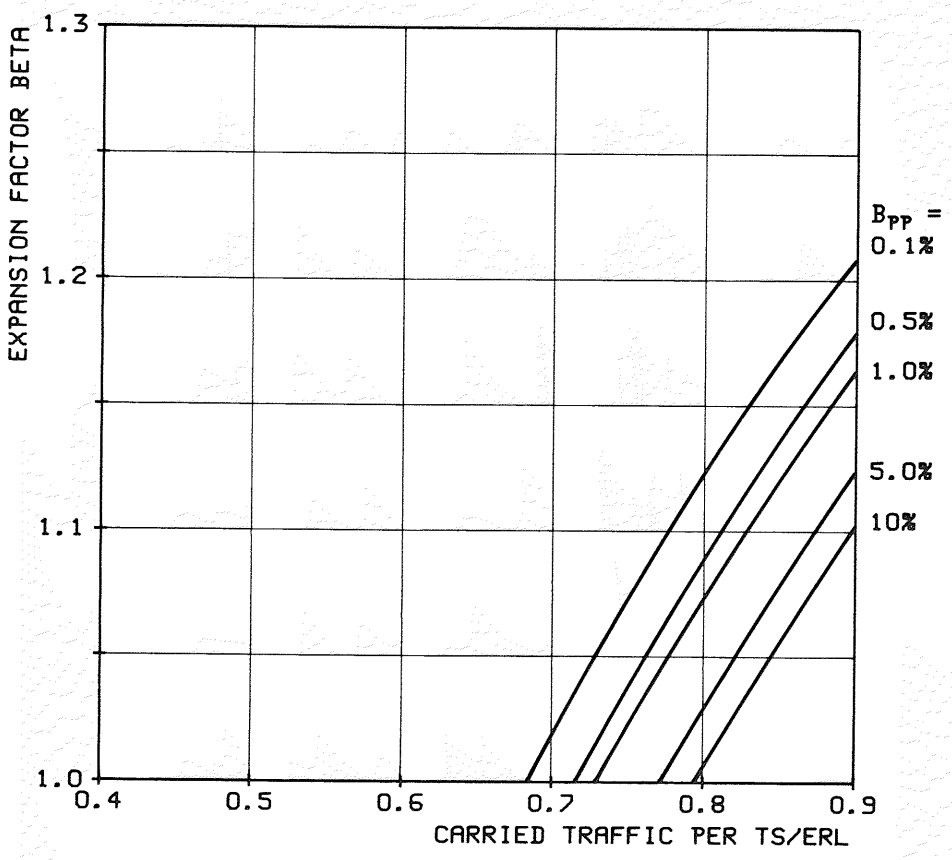


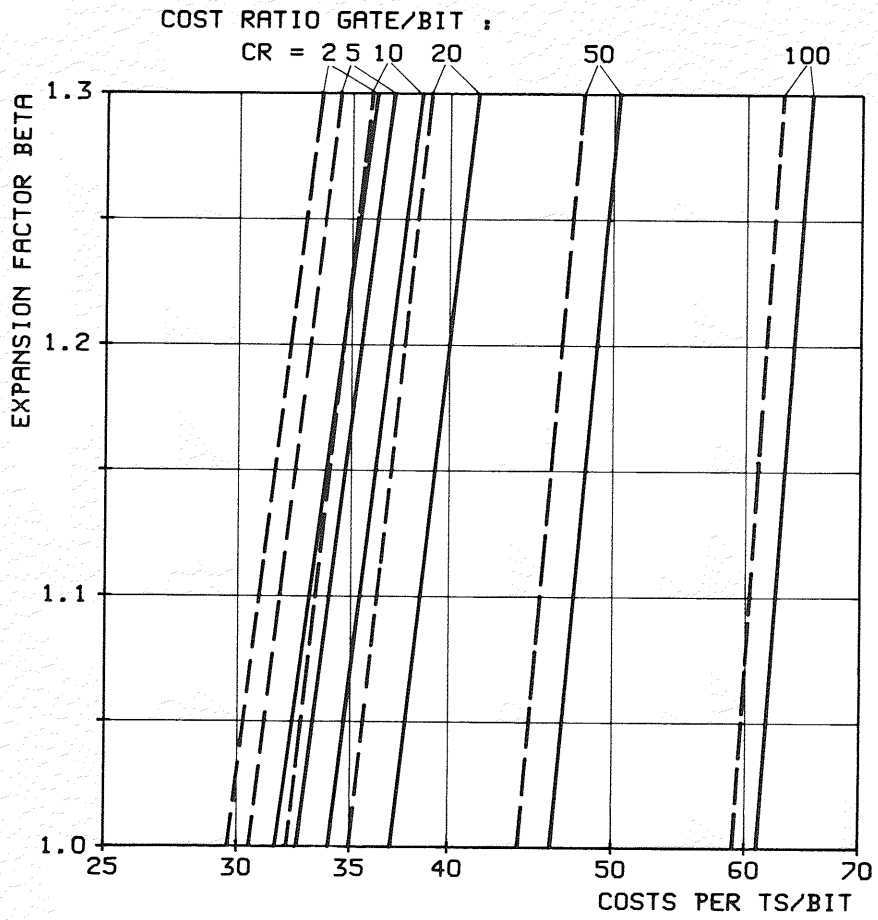


COMBINED SWITCHING 1 × 100 HW H_2 = 10 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 100 HW M = 120 --- SEPARATED SWITCHING

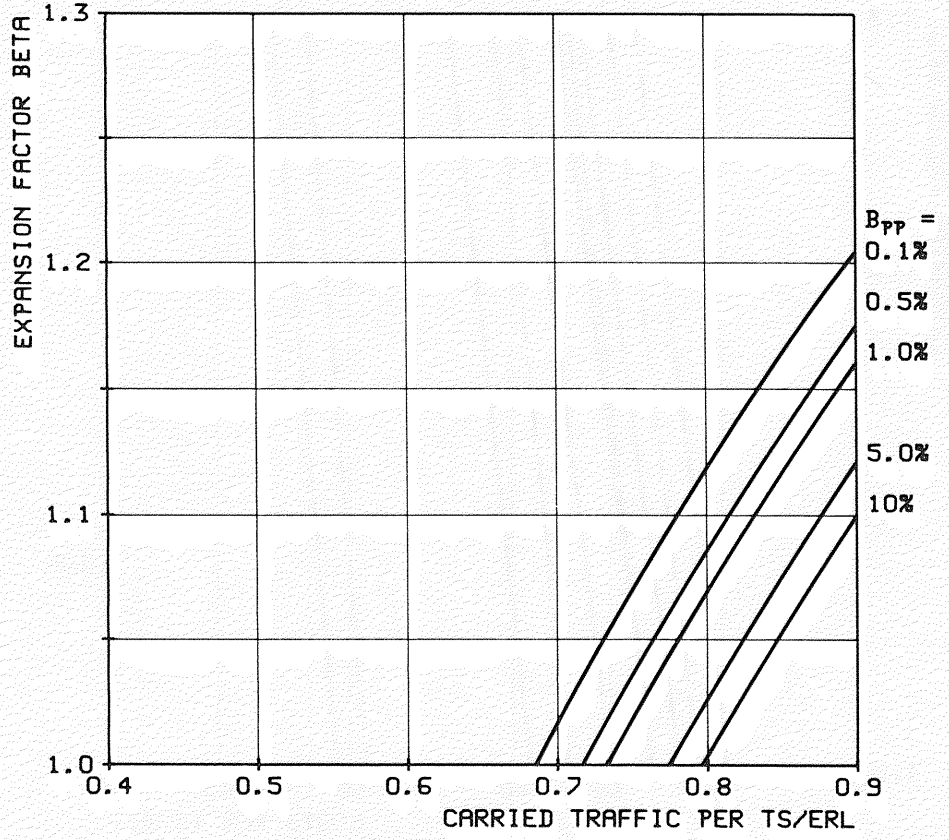
TSSST

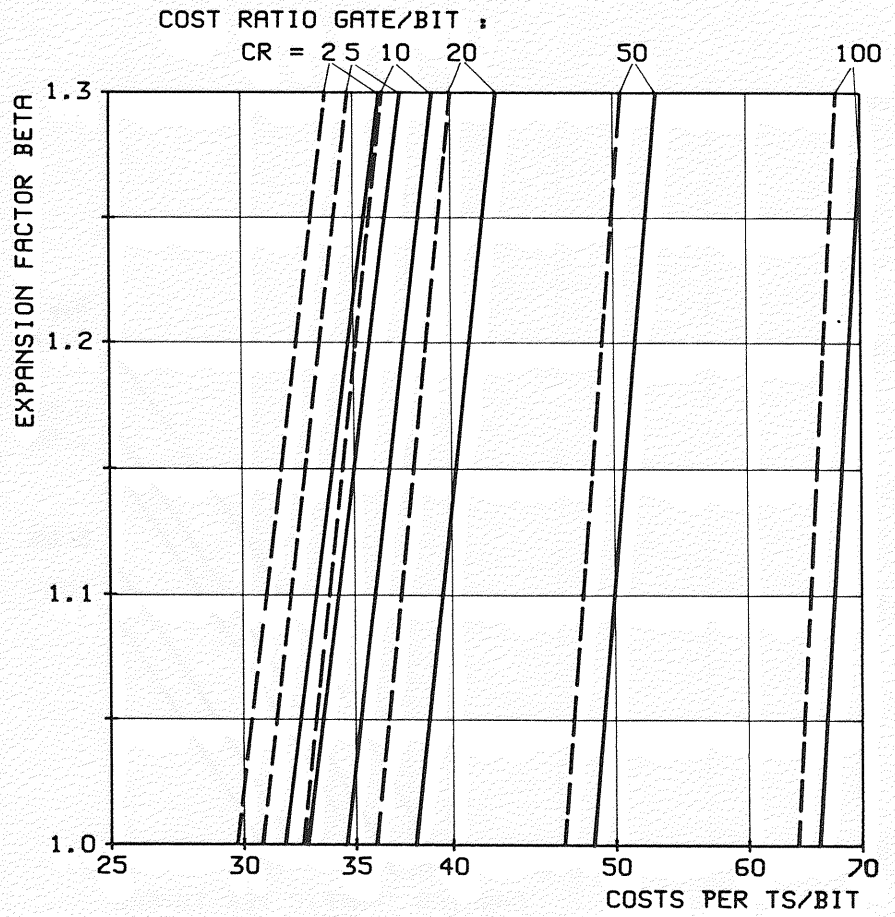




COMBINED SWITCHING 1 × 144 HW H_2 = 12 —— COMBINED SWITCHING
SEPARATED SWITCHING 2 × 144 HW M = 120 --- SEPARATED SWITCHING

TSSST



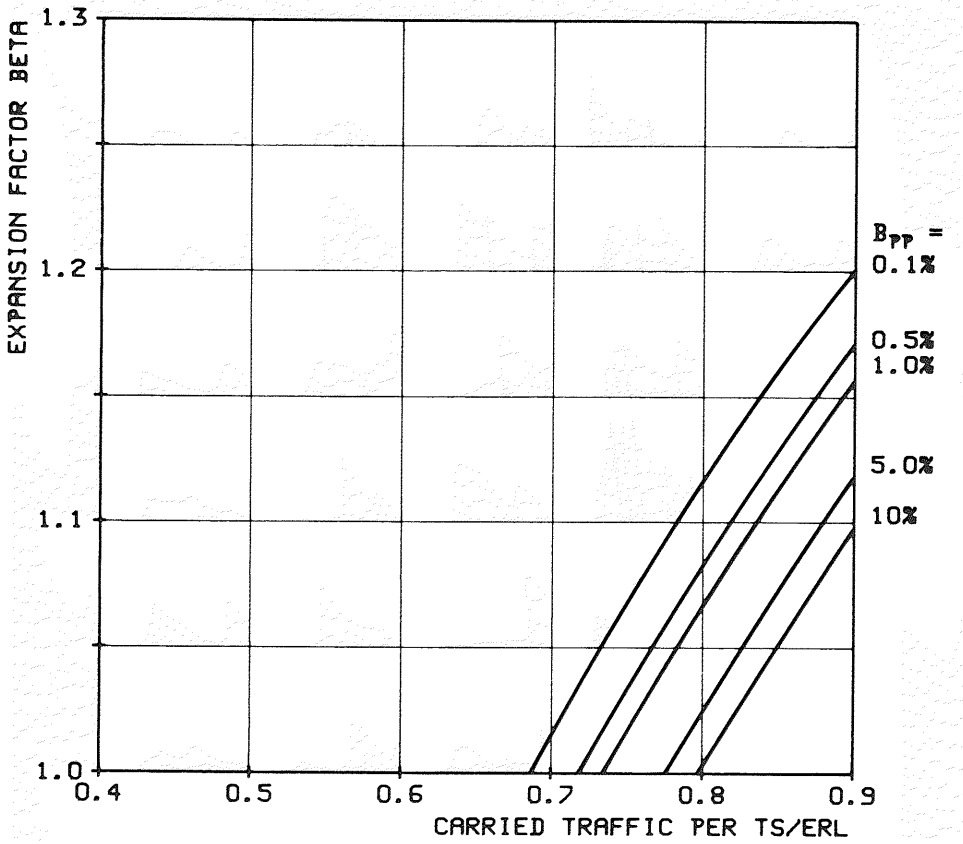


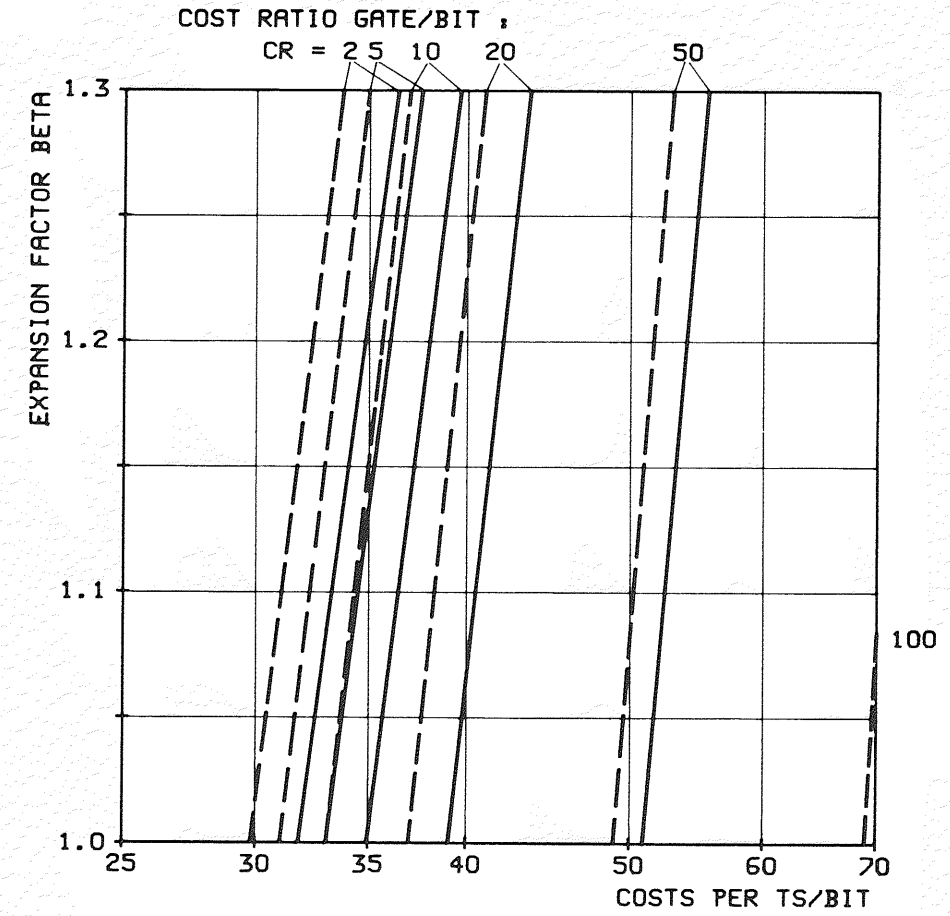
COMBINED SWITCHING 1 × 196 HW H_2 = 14 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 196 HW M = 120 --- SEPARATED SWITCHING

-CHART 110-

TSSST

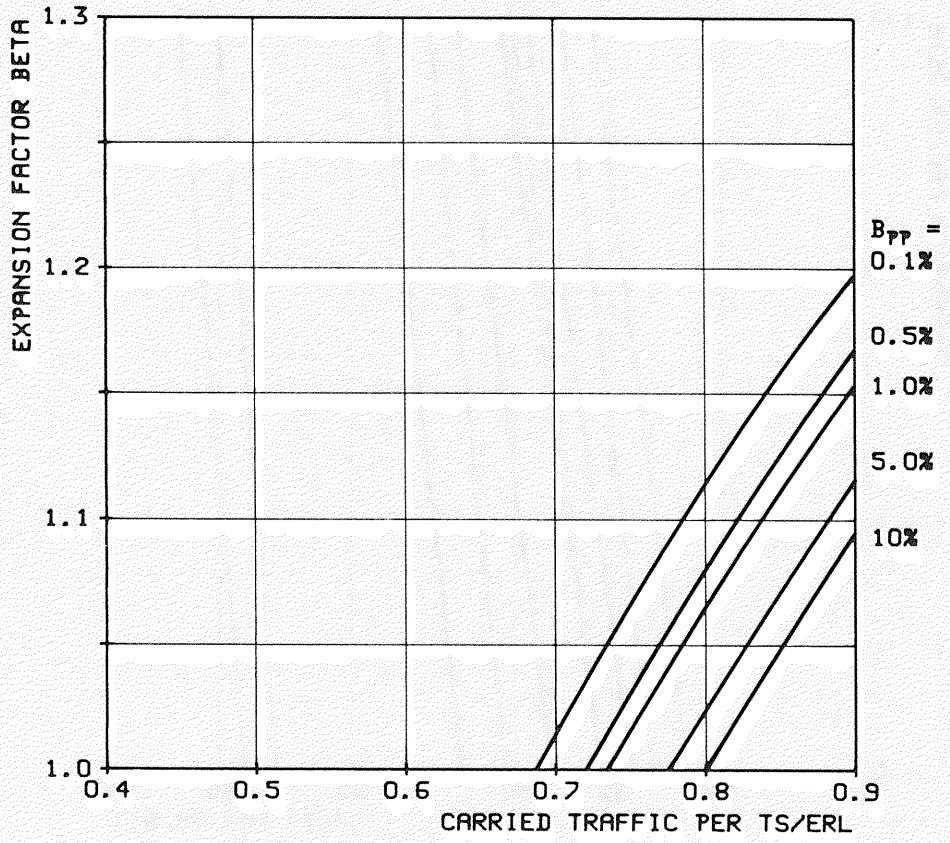


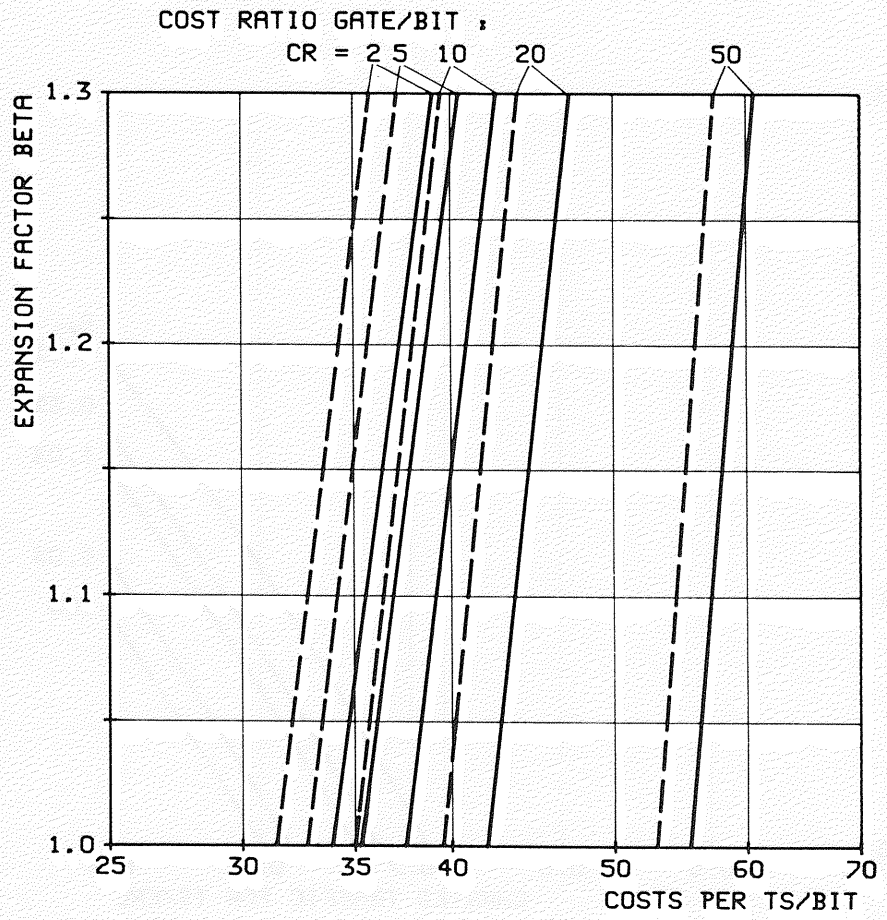


COMBINED SWITCHING 1 × 256 HW H_2 = 16 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 256 HW M = 120 --- SEPARATED SWITCHING

TSSST

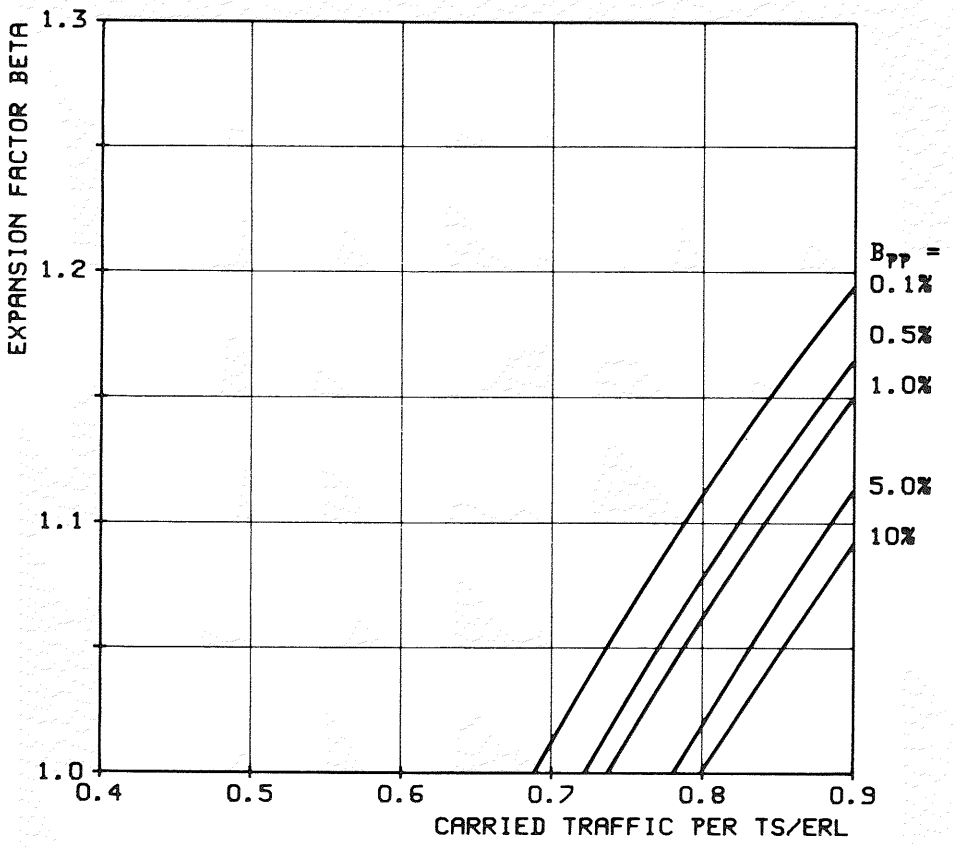


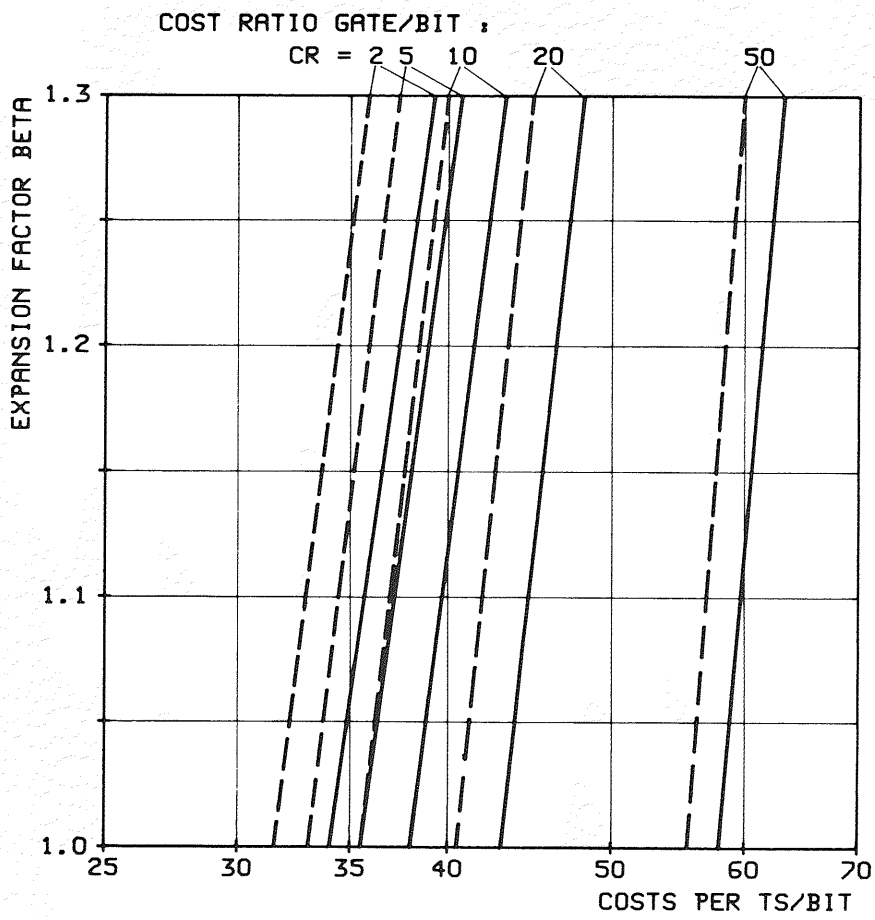


COMBINED SWITCHING 1 × 324 HW H_2 = 18 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 324 HW M = 120 --- SEPARATED SWITCHING

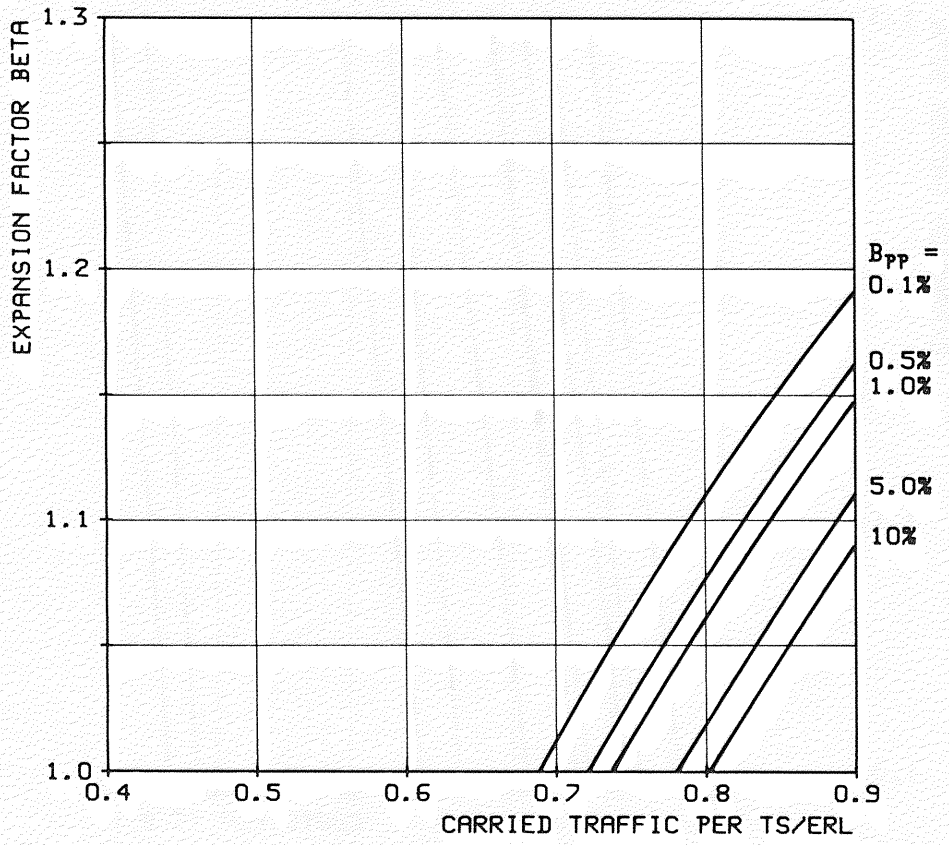
TSSST

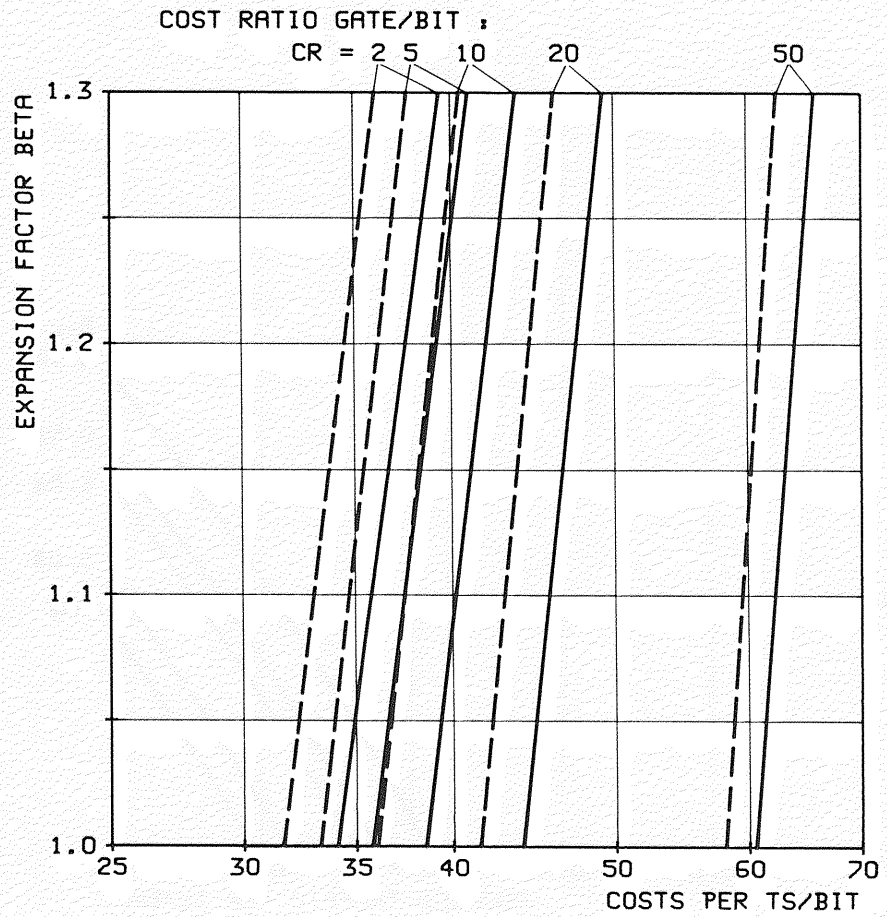




COMBINED SWITCHING 1 × 400 HW H_2 = 20 —— COMBINED SWITCHING
SEPARATED SWITCHING 2 × 400 HW M = 120 --- SEPARATED SWITCHING

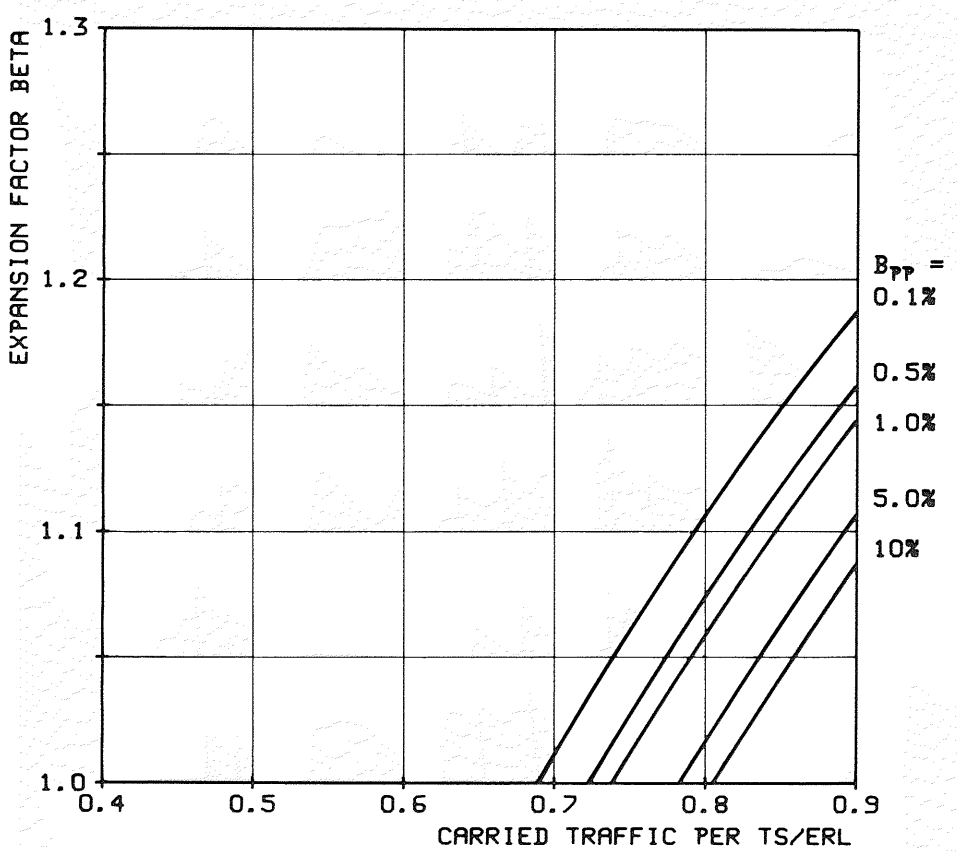
TSSST

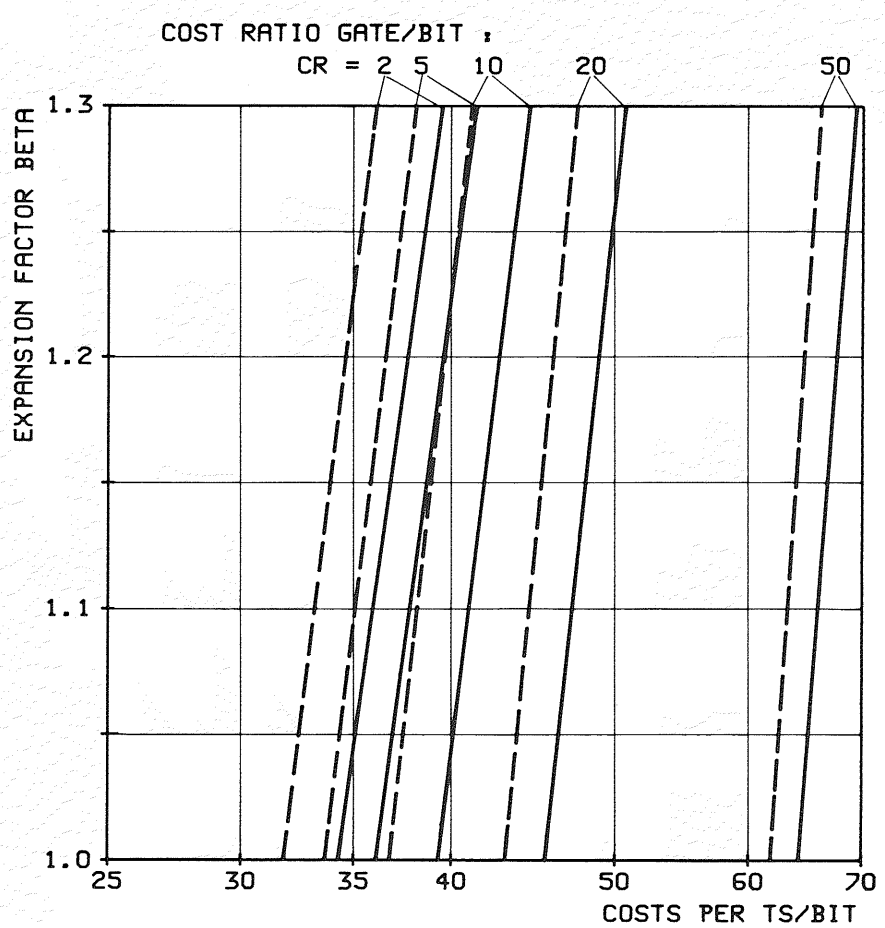




COMBINED SWITCHING	1 × 484 HW	H_2 = 22	—— COMBINED SWITCHING
SEPARATED SWITCHING	2 × 484 HW	M = 120	--- SEPARATED SWITCHING

TSSST

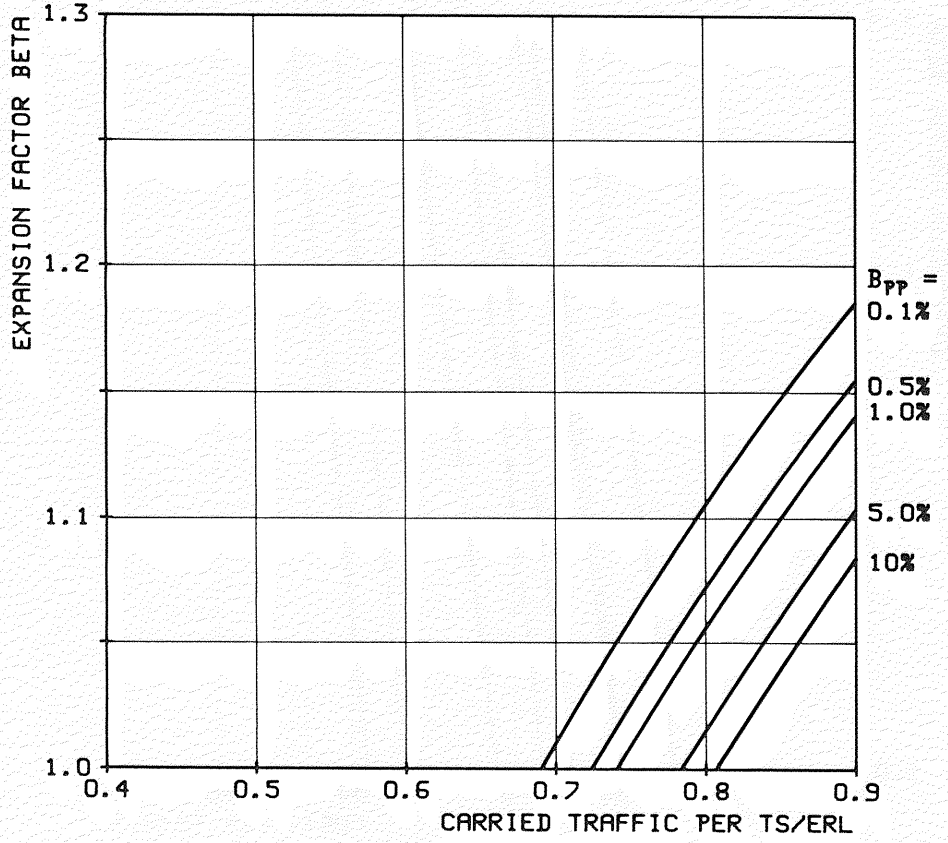


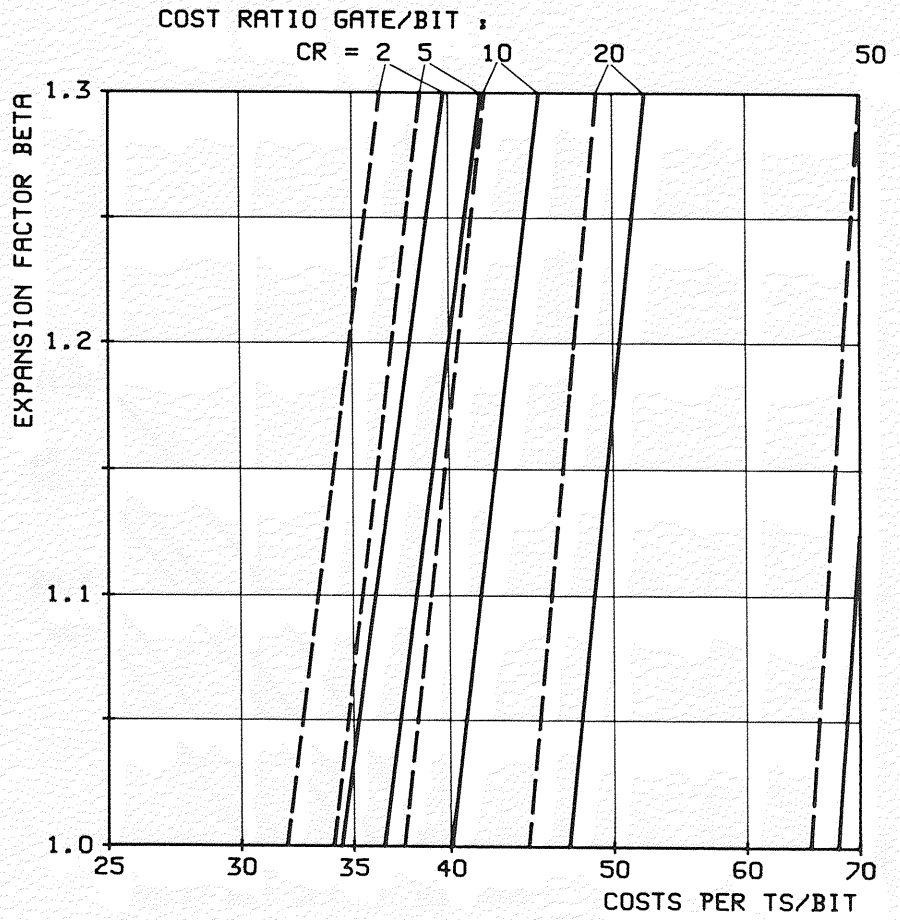


COMBINED SWITCHING 1 × 625 HW H_2 = 25 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 625 HW M = 120 --- SEPARATED SWITCHING

TSSST



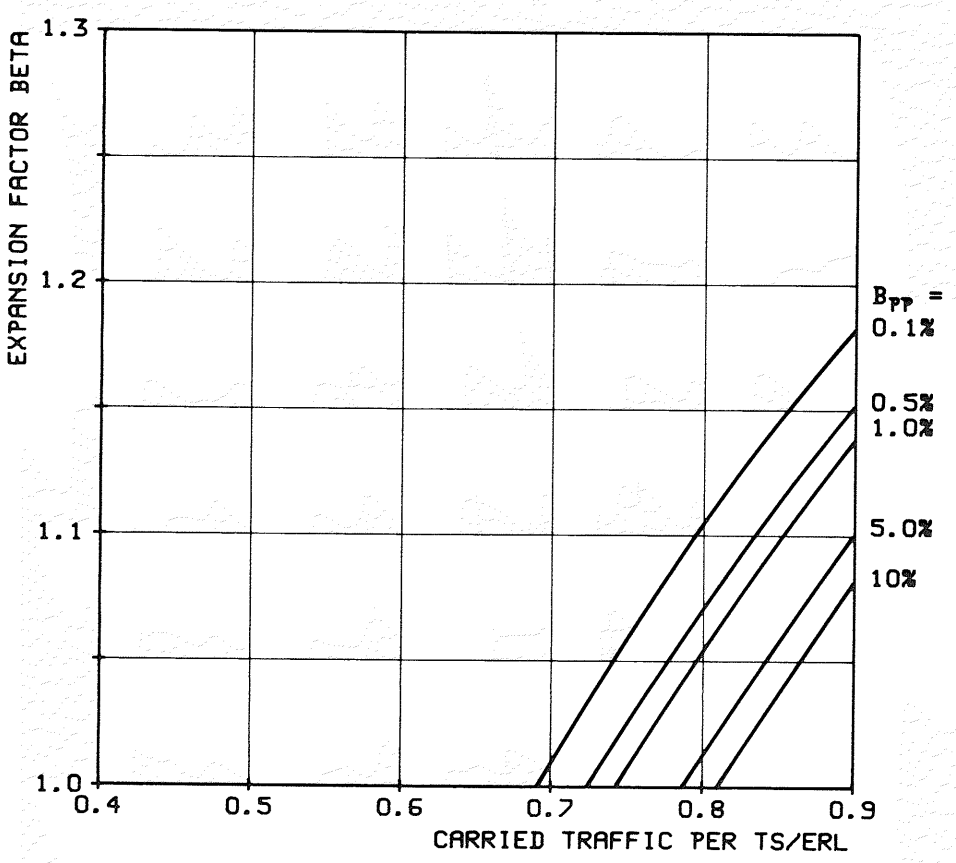


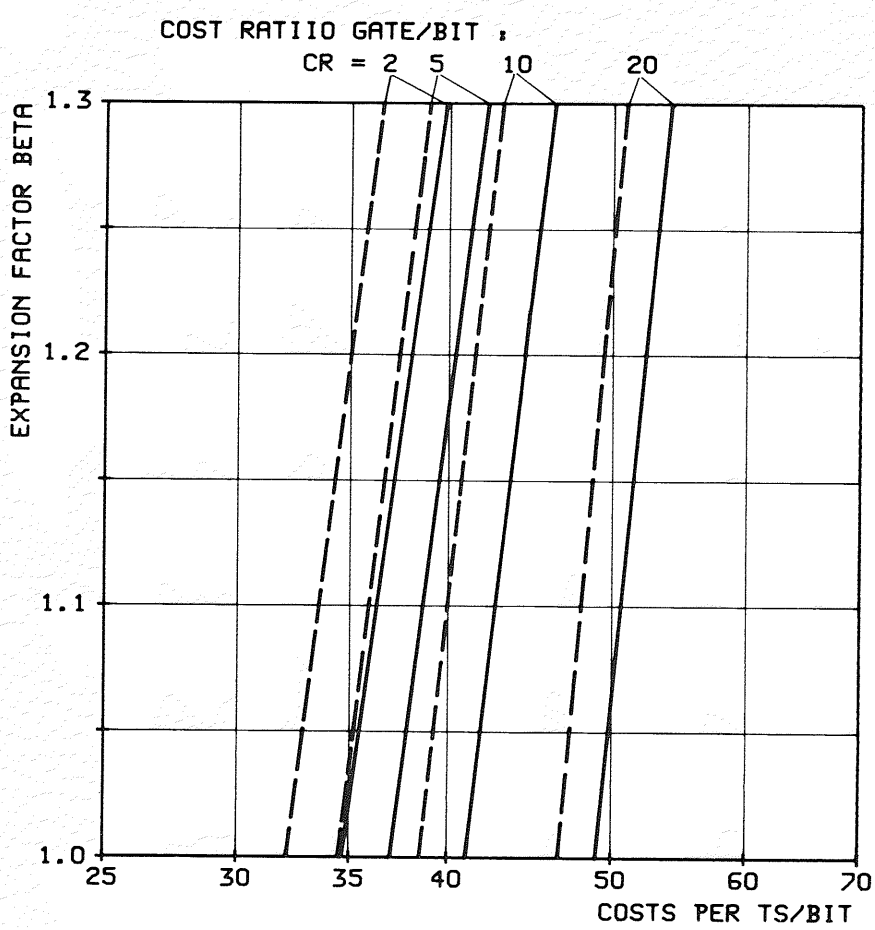
COMBINED SWITCHING 1 × 784 HW H_2 = 28 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 784 HW M = 120 --- SEPARATED SWITCHING

-CHART 116-

TSSST





COMBINED SWITCHING 1 × 1024 HW H_2 = 32 —— COMBINED SWITCHING

SEPARATED SWITCHING 2 × 1024 HW M = 120 --- SEPARATED SWITCHING

PCM SWITCHING ARRAY : SSTSS

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 9, 16, 25, 36, 64,
100, 144, 196, 256, 324,
400, 484, 625, 784, 1024,

SEPARATED SWITCHING : HW = 18, 32, 50, 72, 128,
200, 288, 392, 512, 648,
800, 968, 1250, 1568, 2048,

TIME-SLOTS (TS) PER HW : M = 120 TS

POINT-TO-POINT LOSS, PCT1 : B_{PP} = 0.1, 0.5, 1.0, 5.0, 10.0%

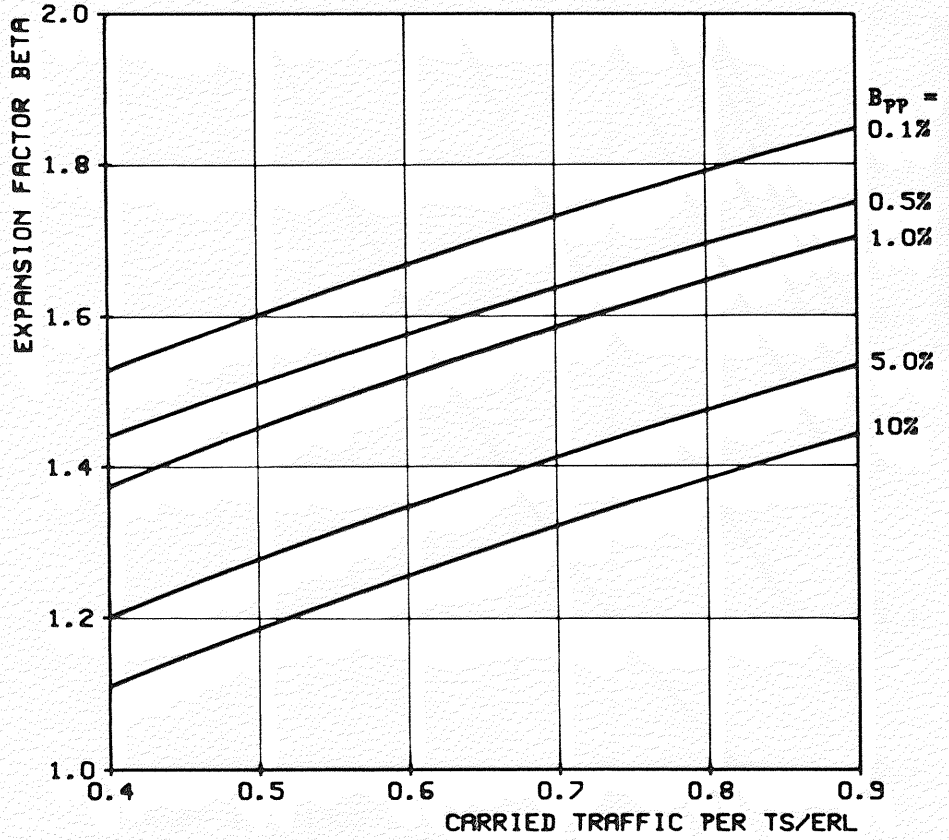
COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

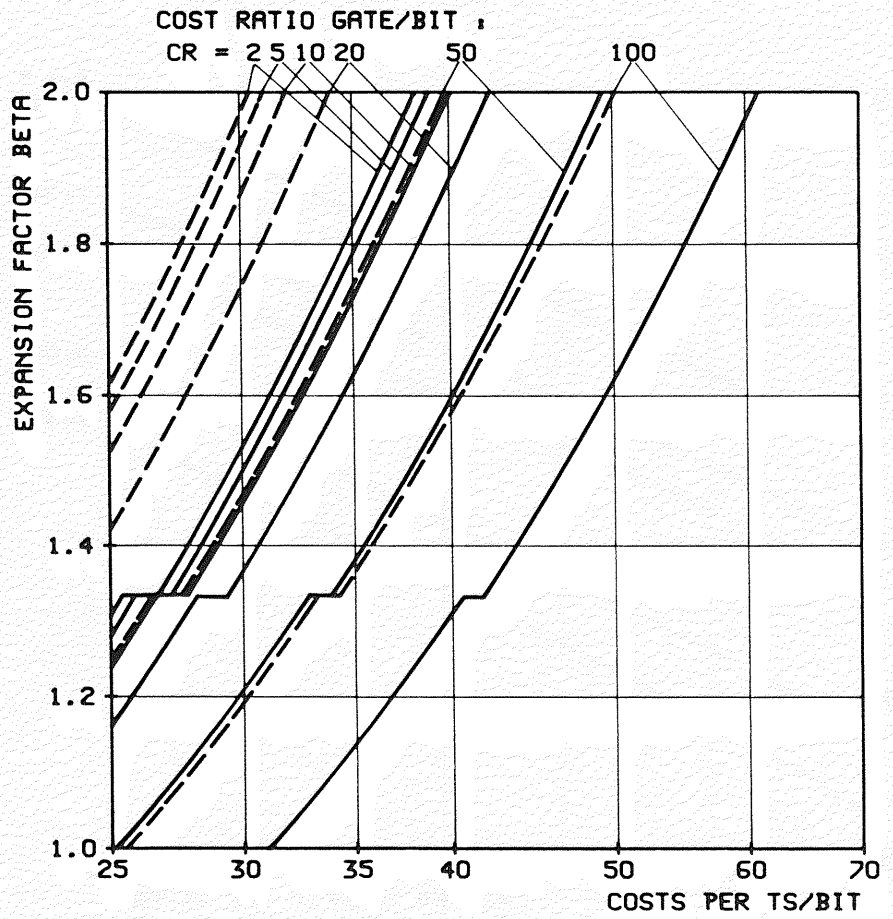
BLOCK SIZE

COMBINED SWITCHING : $H_1 = \sqrt{HW}$

SEPARATED SWITCHING : $H_1 = \sqrt{HW/2}$

SSTSS





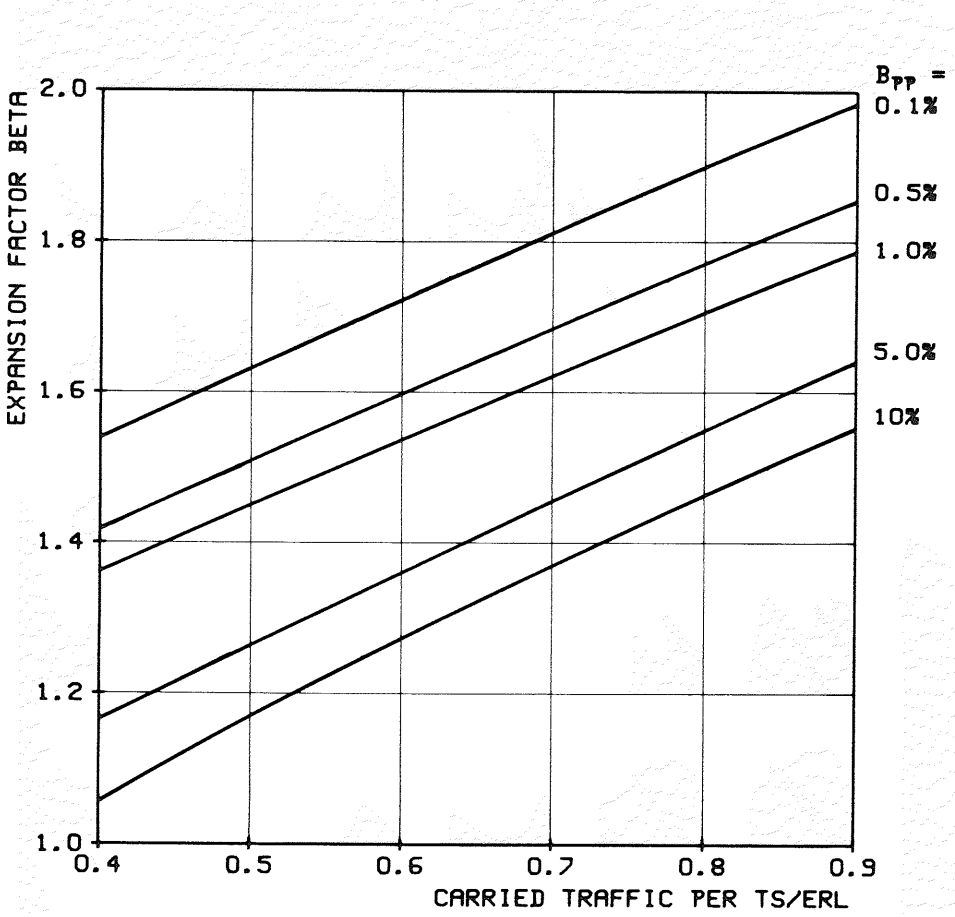
COMBINED SWITCHING 1 × 9 HW H_1 = 3

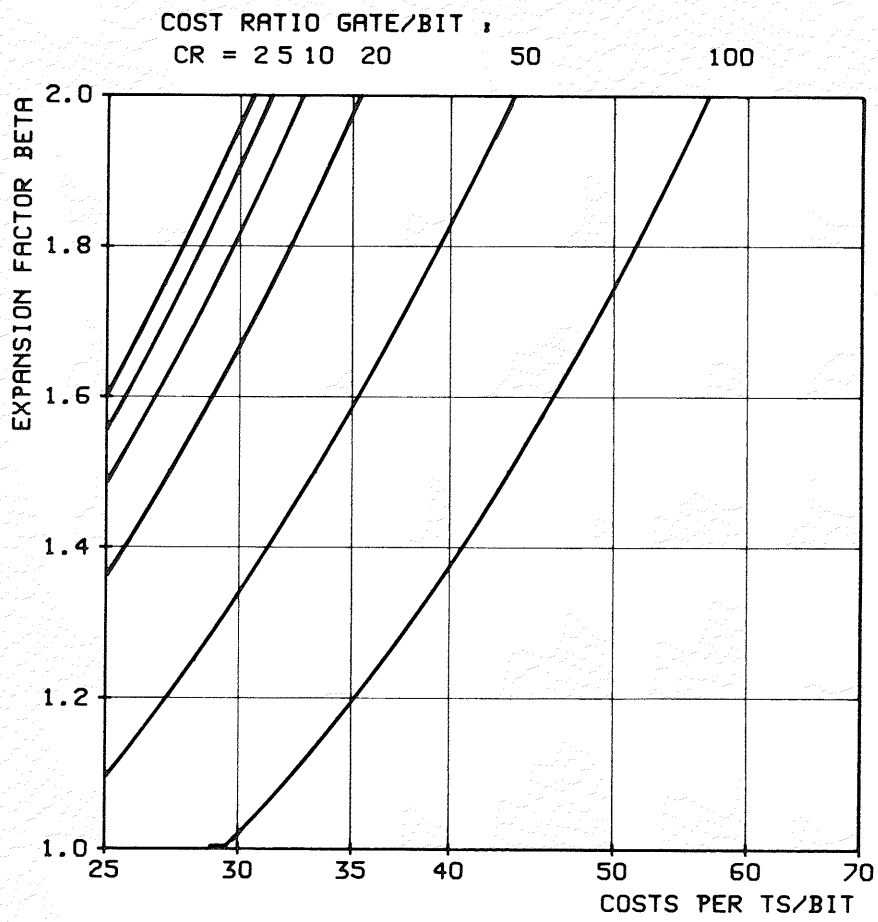
SEPARATED SWITCHING 2 × 9 HW M = 120

—— COMBINED SWITCHING

--- SEPARATED SWITCHING

SSTSS

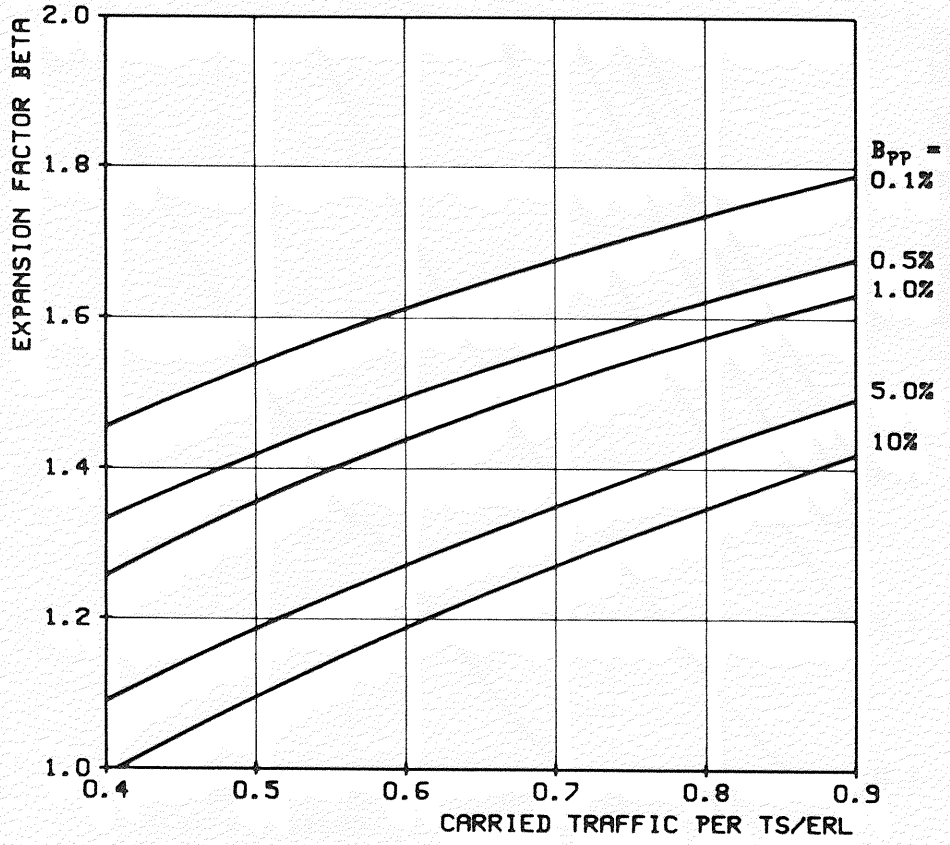


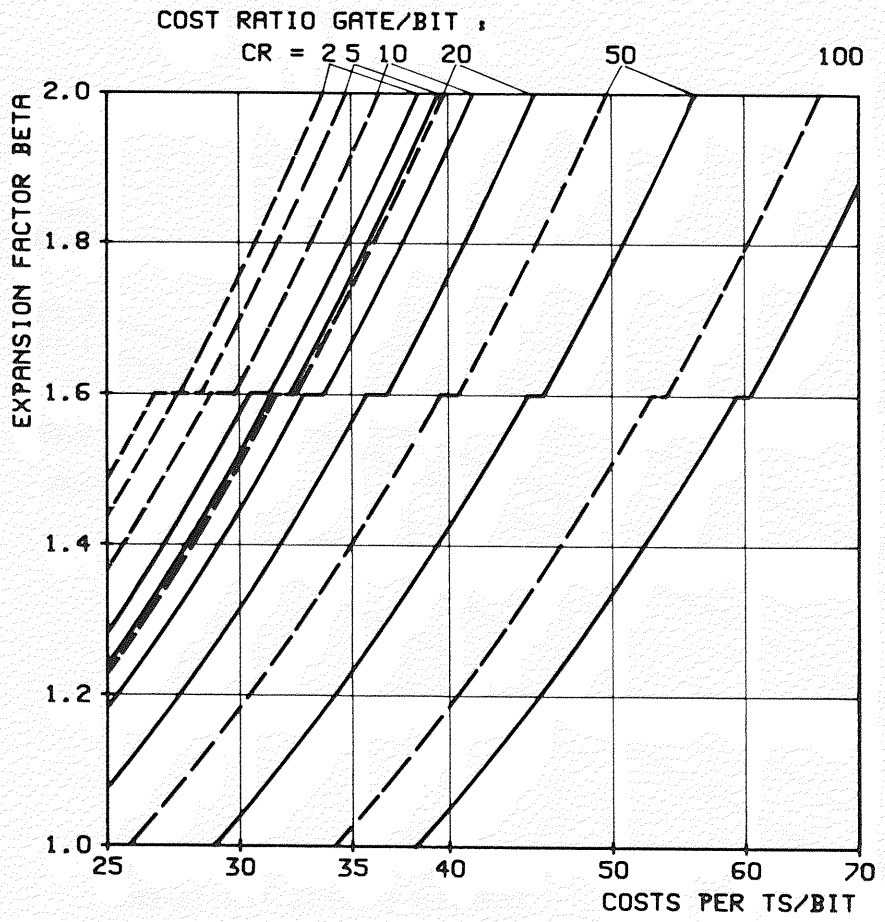


COMBINED SWITCHING 1 × 16 HW H_1 = 4
SEPARATED SWITCHING 2 × 16 HW M = 120

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

SSTSS

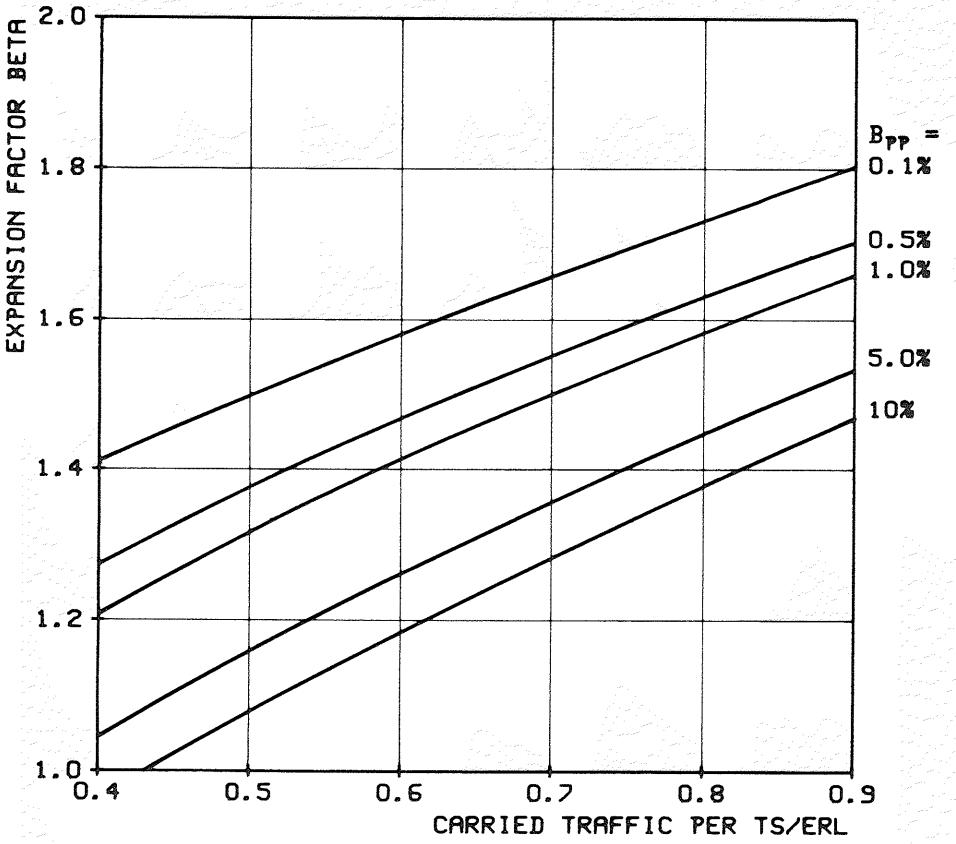


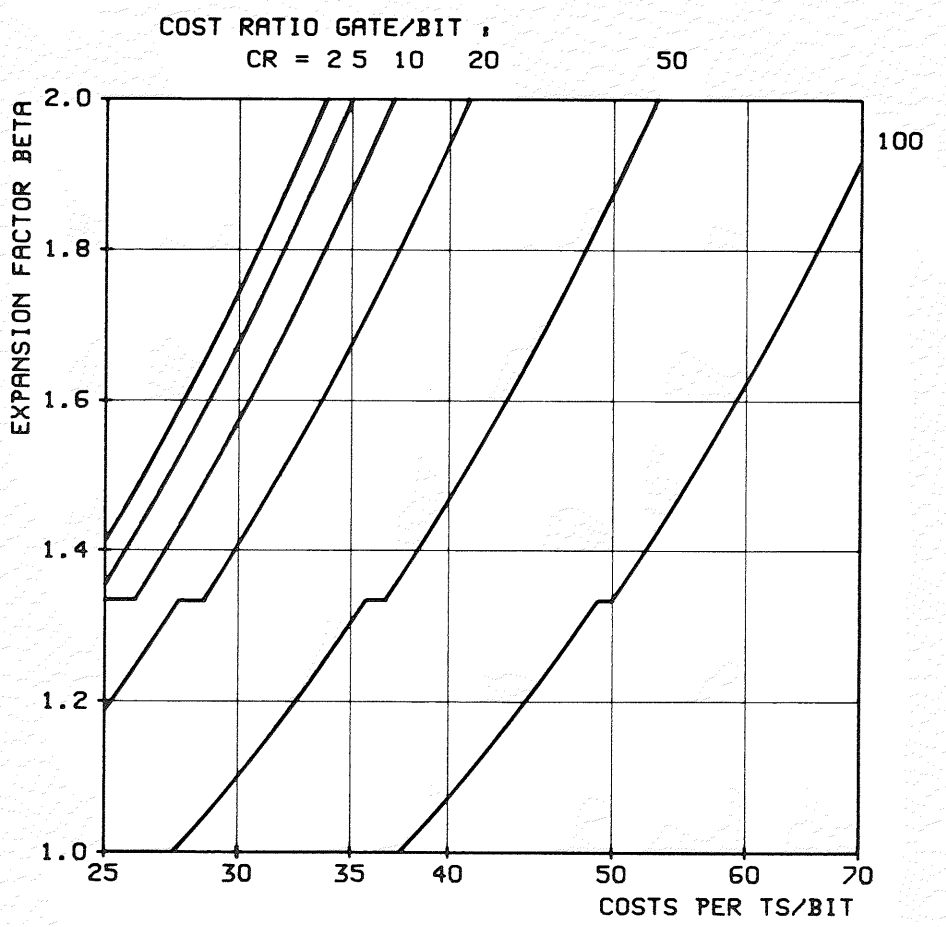


COMBINED SWITCHING	1 × 25 HW	H_1 = 5	—— COMBINED SWITCHING
SEPARATED SWITCHING	2 × 25 HW	M = 120	--- SEPARATED SWITCHING

-CHART 120-

SSTSS

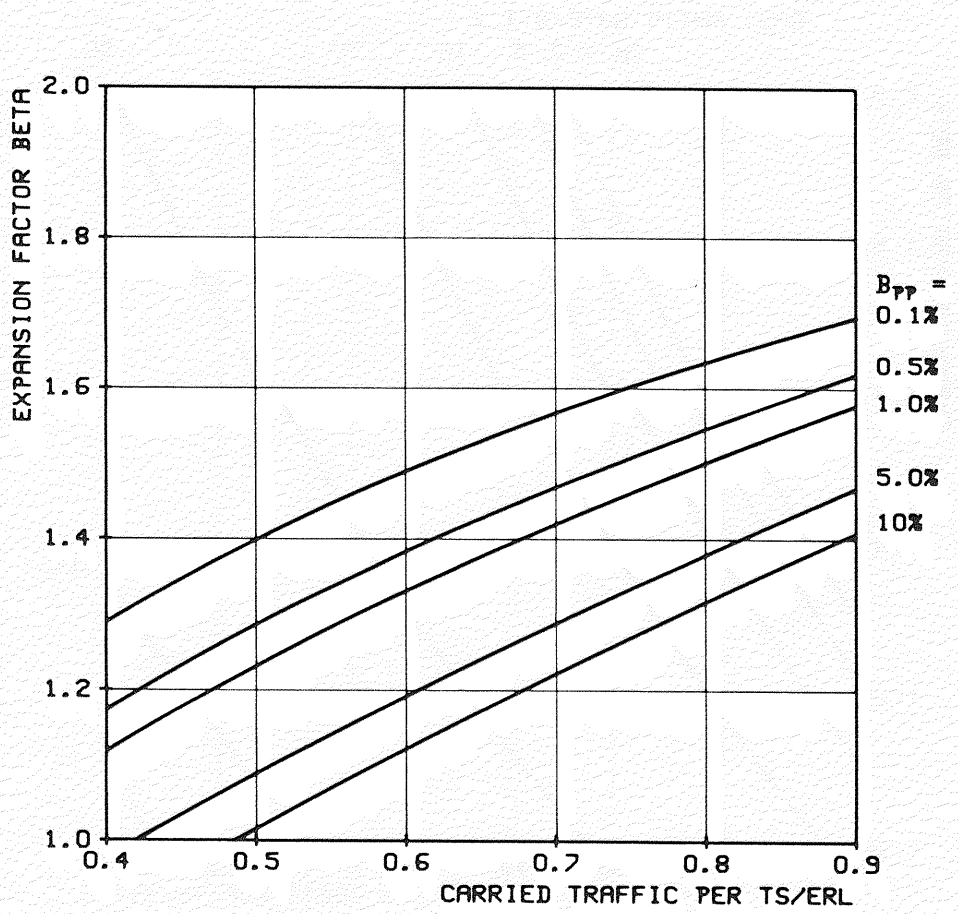


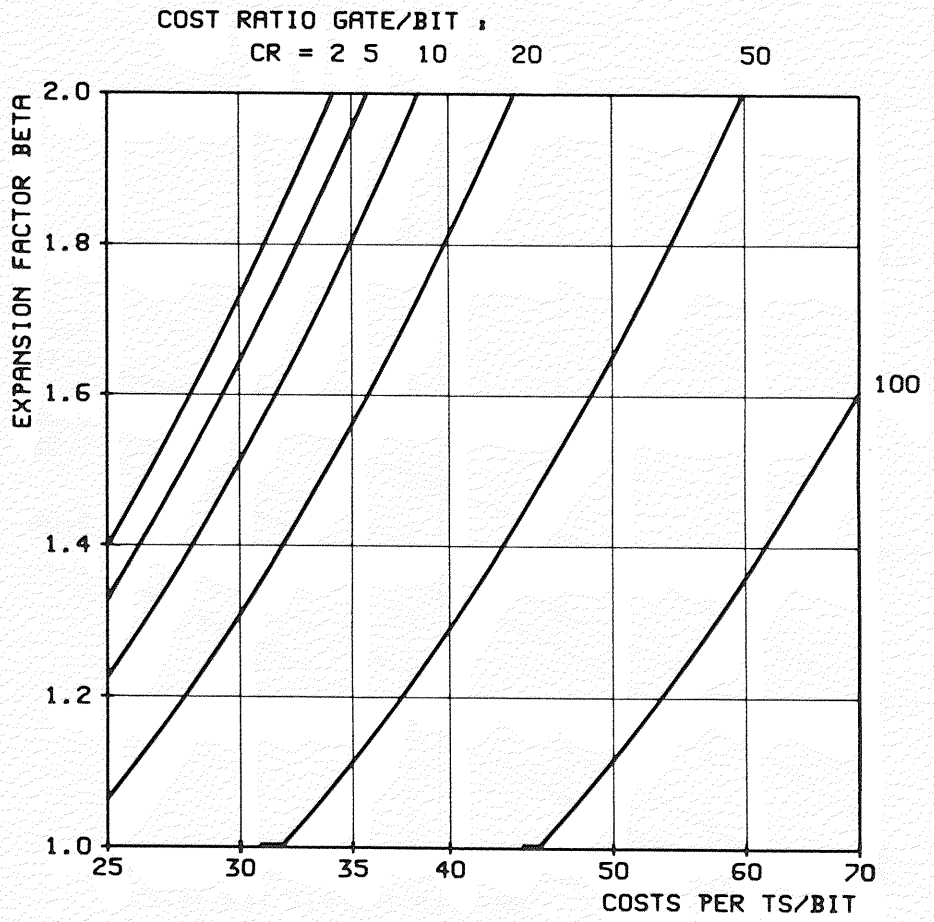


COMBINED SWITCHING 1 × 36 HW H_1 = 6
SEPARATED SWITCHING 2 × 36 HW M = 120

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

SSTSS

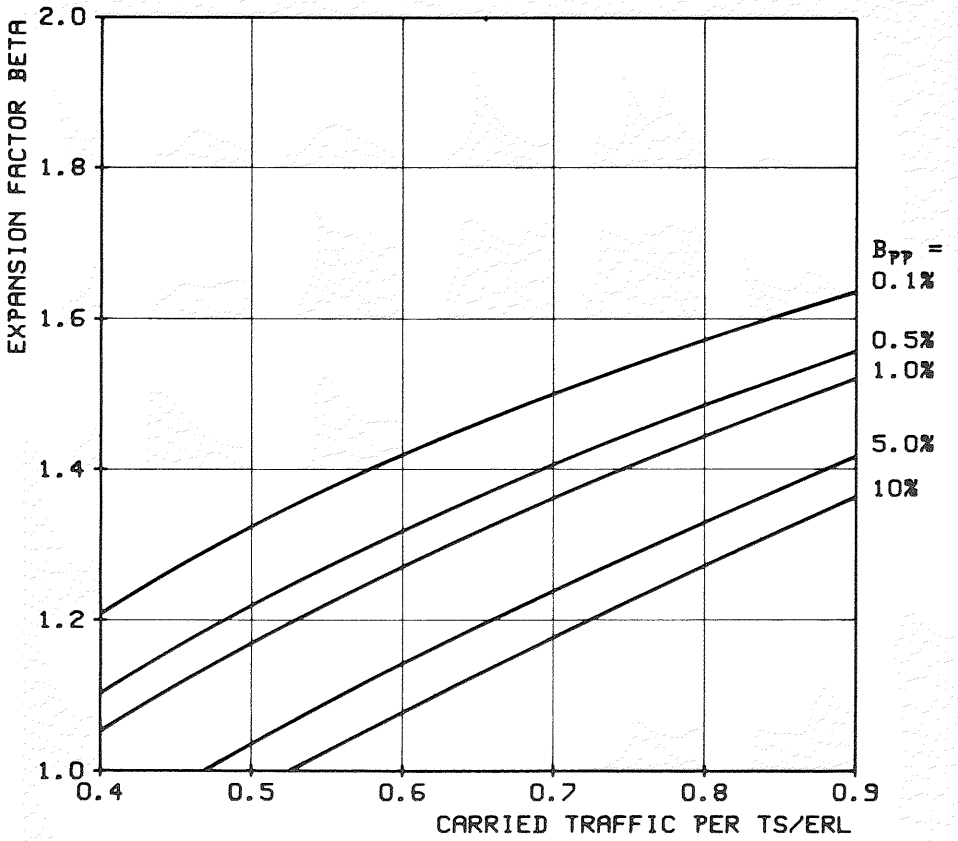


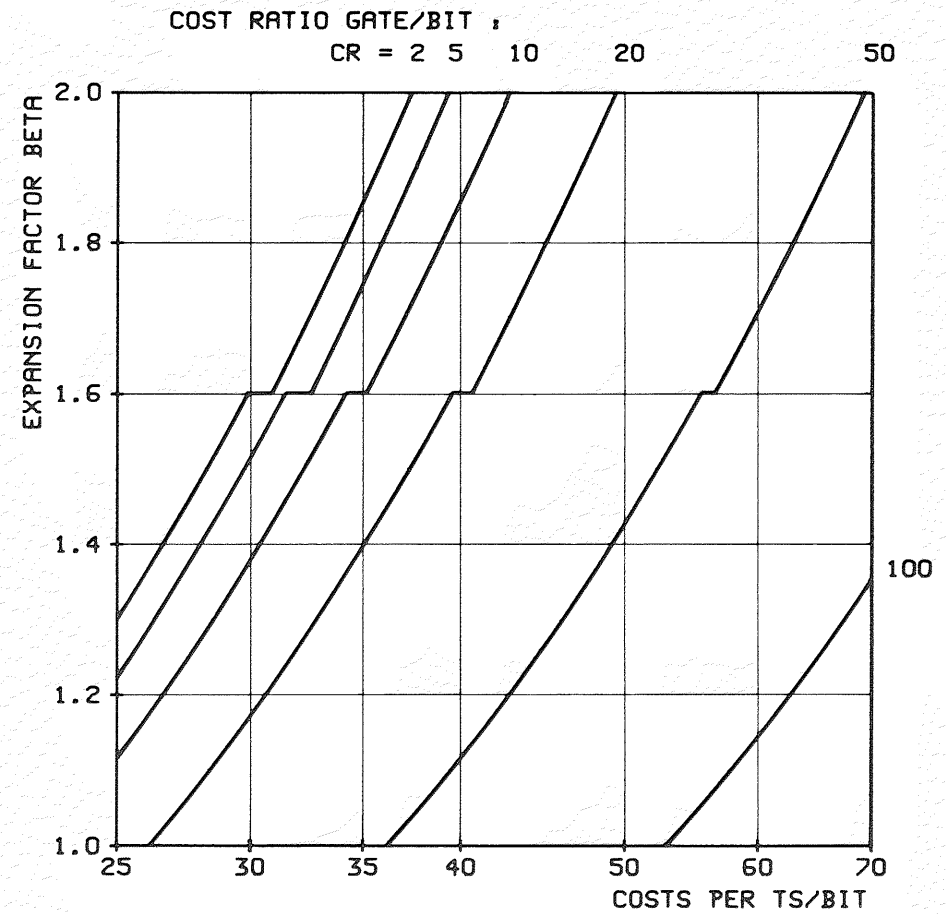


COMBINED SWITCHING 1 × 64 HW H_1 = 8
SEPARATED SWITCHING 2 × 64 HW M = 120

—— { COMBINED SWITCHING
SEPARATED SWITCHING

SSTSS



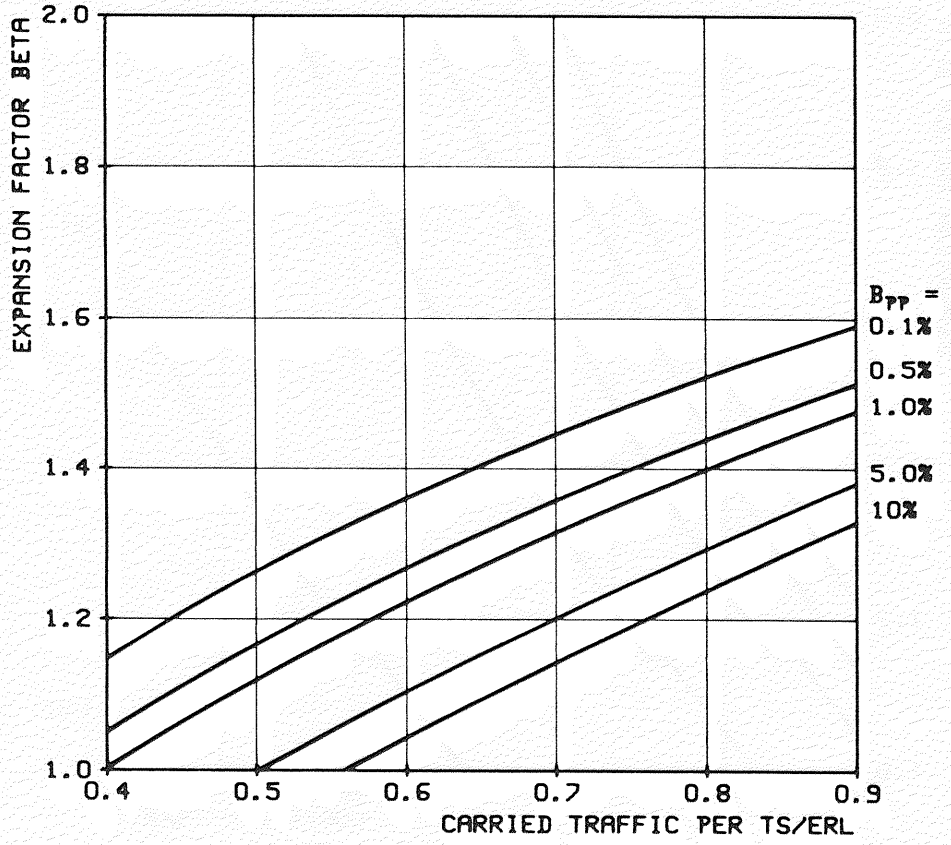


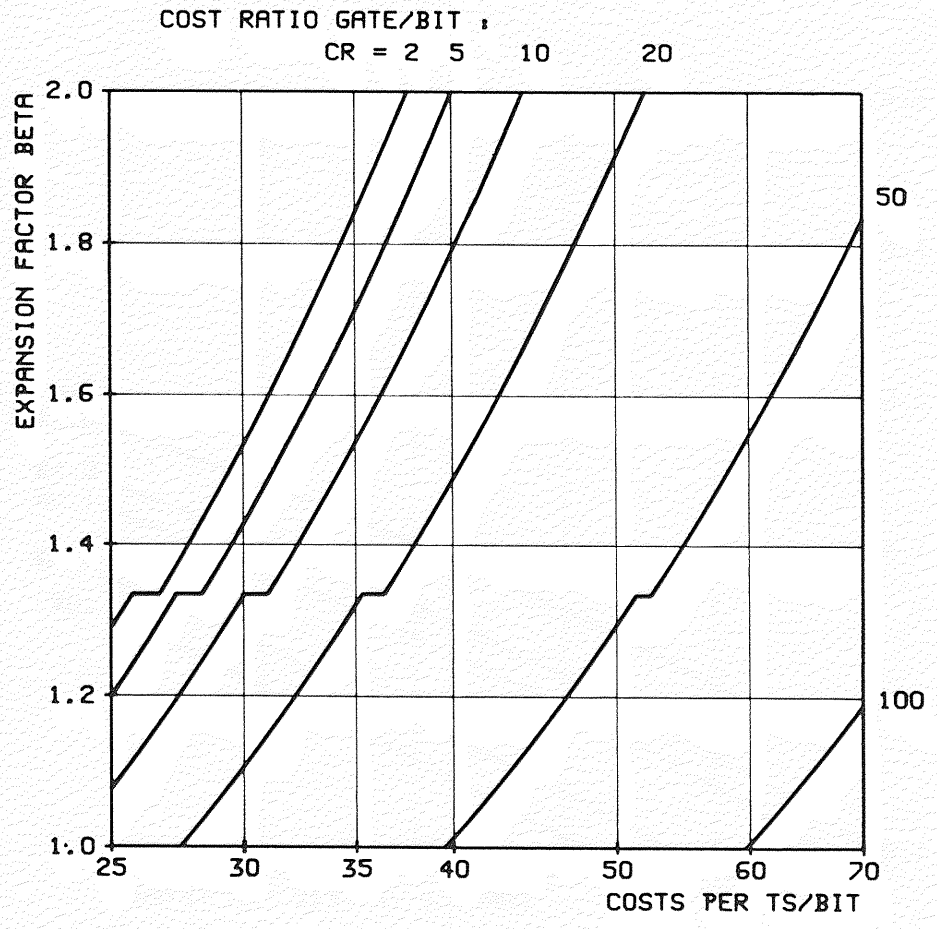
COMBINED SWITCHING 1 × 100 HW H_1 = 10

SEPARATED SWITCHING 2 × 100 HW M = 120

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

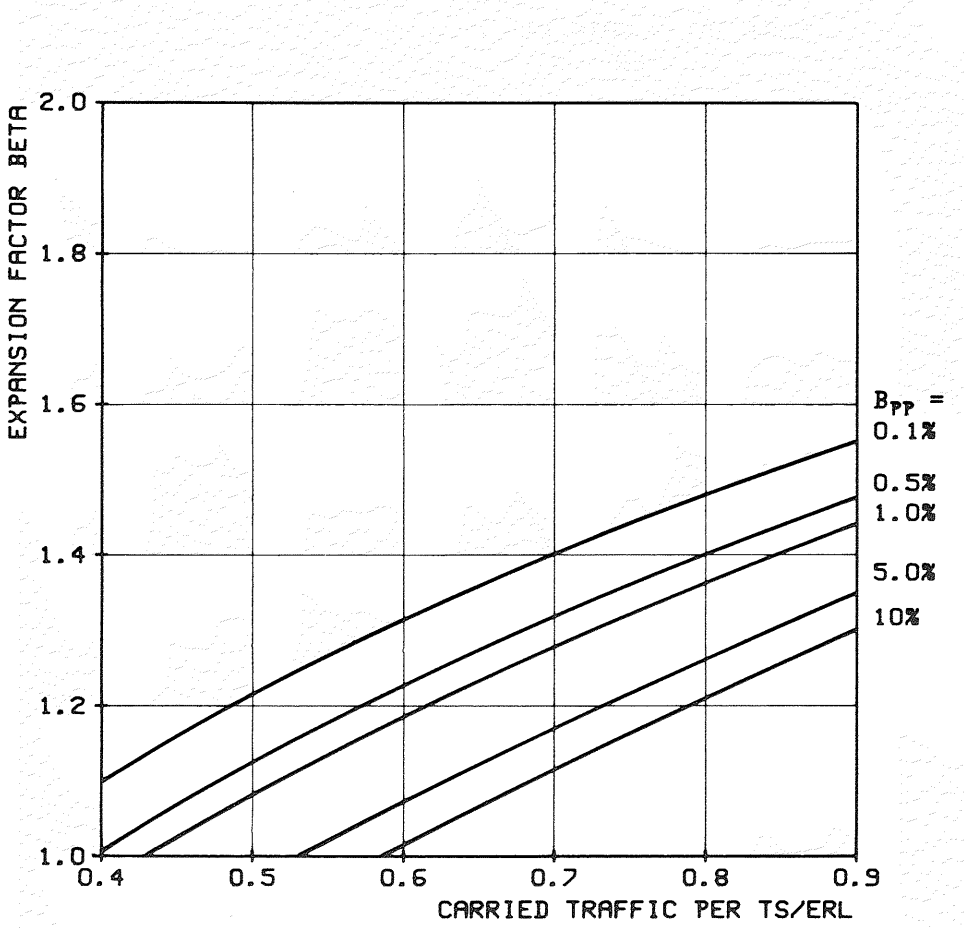
SSTSS

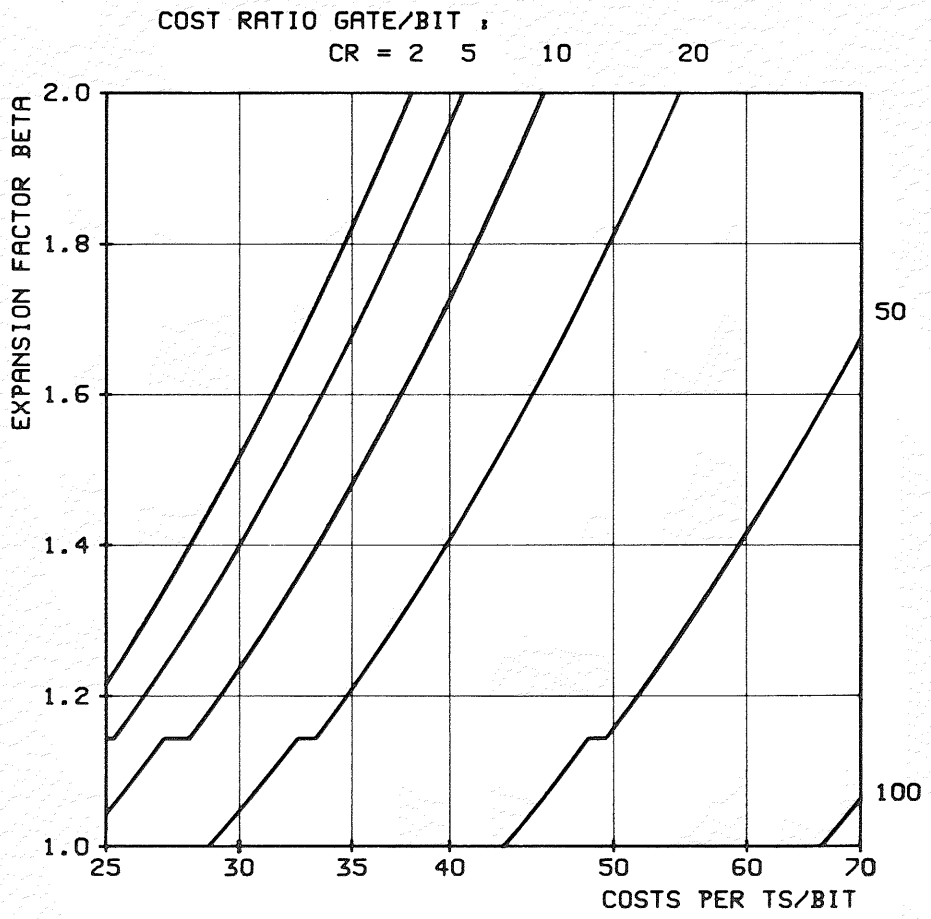




COMBINED SWITCHING	1 × 144 HW	H_1 = 12	——{ COMBINED SWITCHING
SEPARATED SWITCHING	2 × 144 HW	M = 120	{ SEPARATED SWITCHING

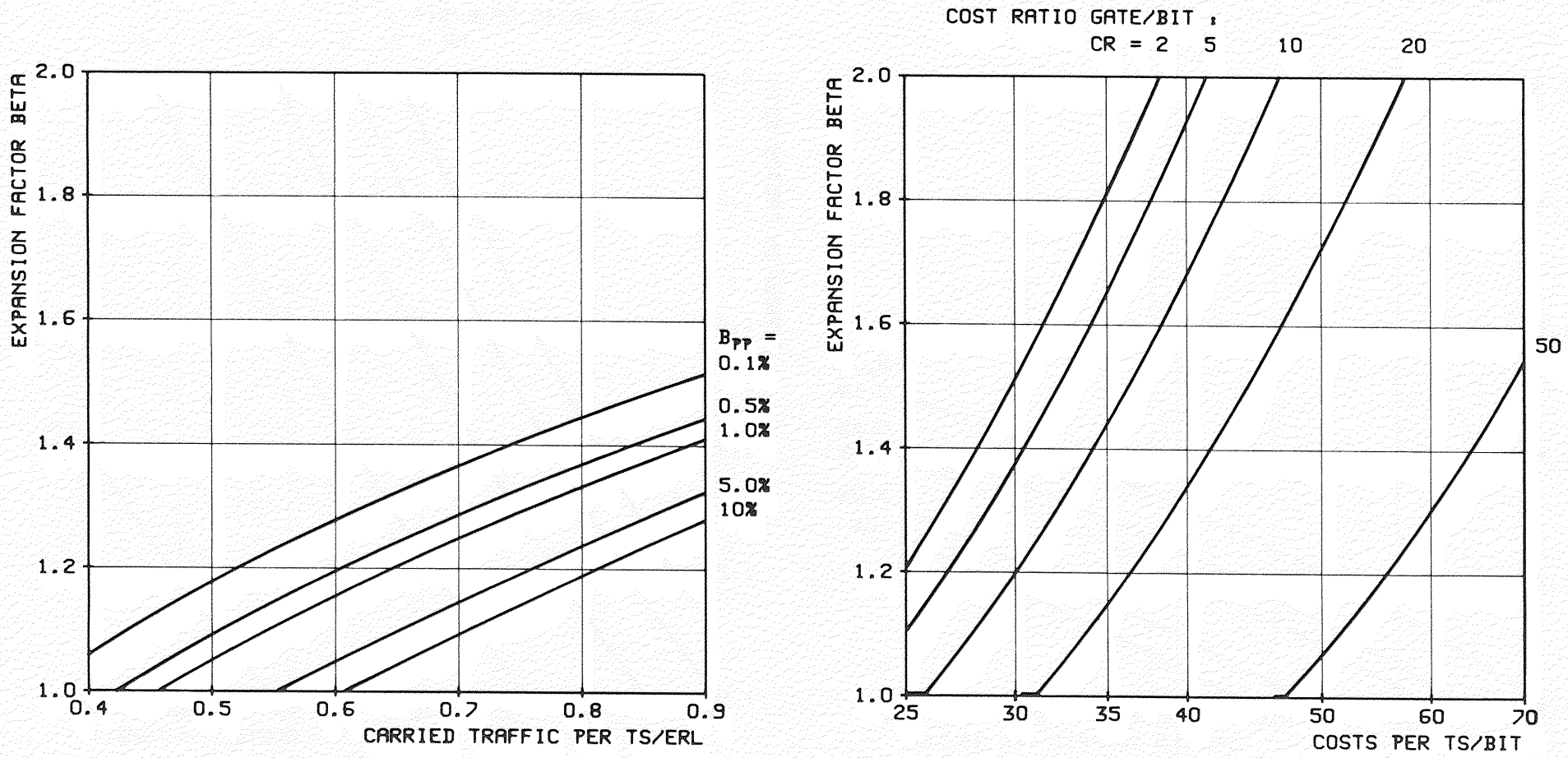
SSTSS





COMBINED SWITCHING	1 × 196 HW	H_1 = 14	——{ COMBINED SWITCHING
SEPARATED SWITCHING	2 × 196 HW	M = 120	{ SEPARATED SWITCHING

SSTSS

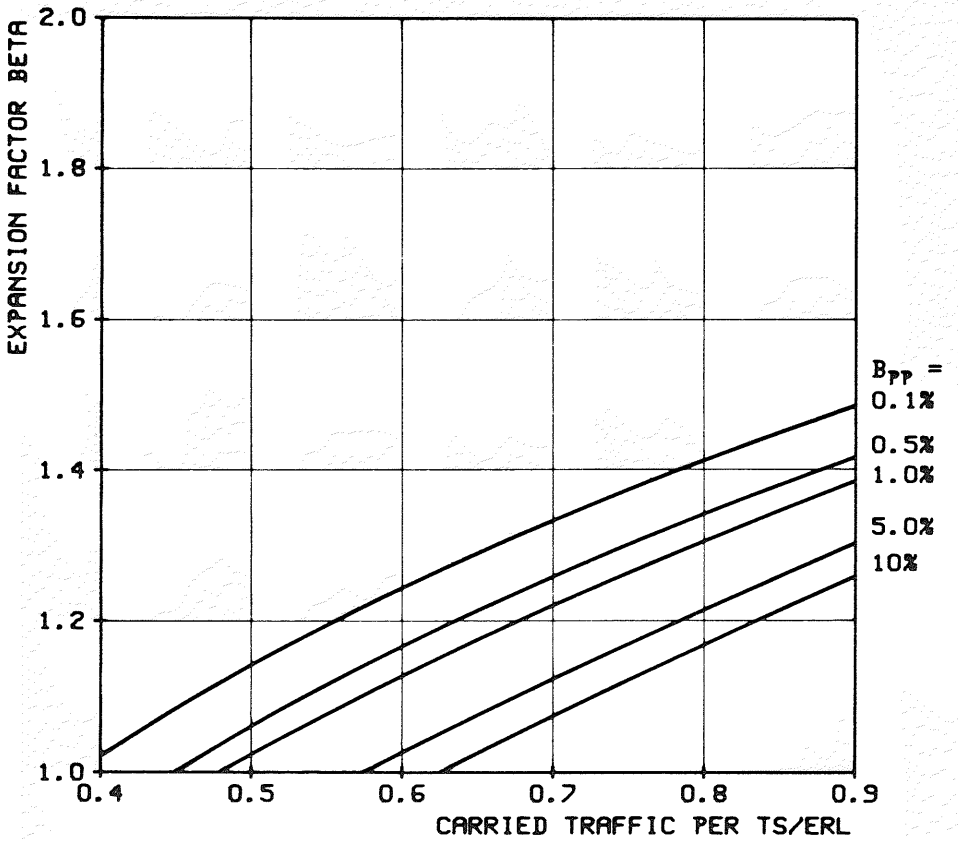


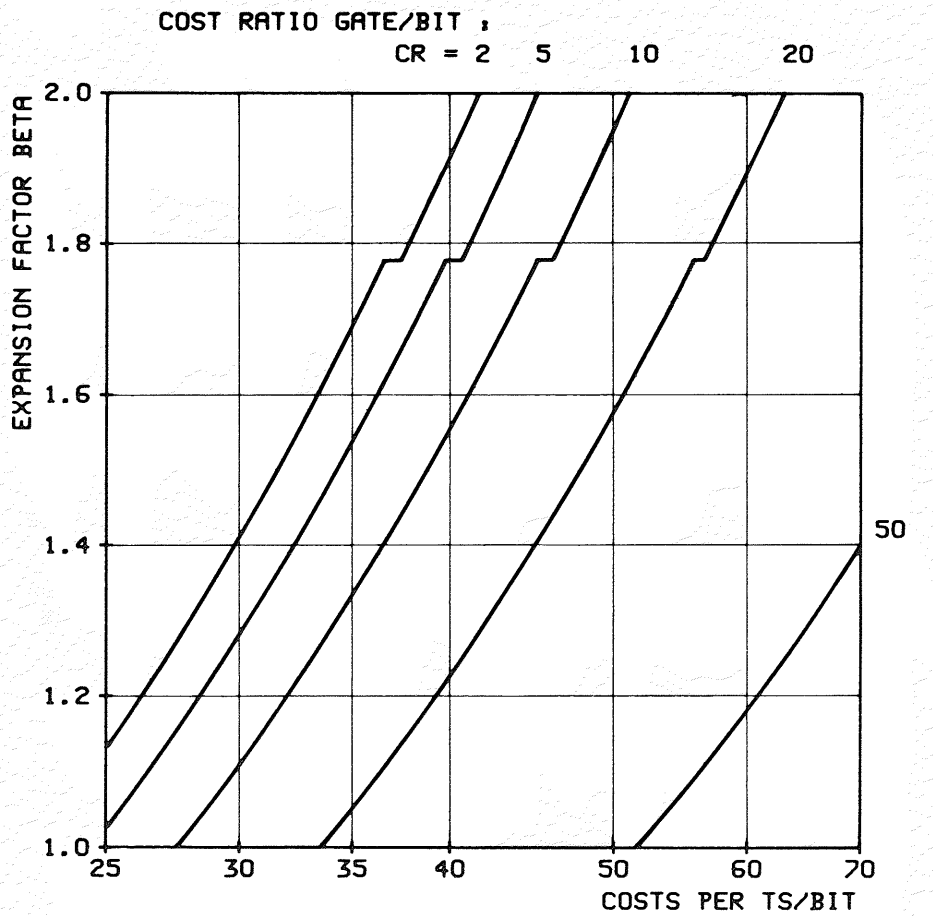
COMBINED SWITCHING 1 × 256 HW H_1 = 16

SEPARATED SWITCHING 2 × 256 HW M = 120

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

SSTSS

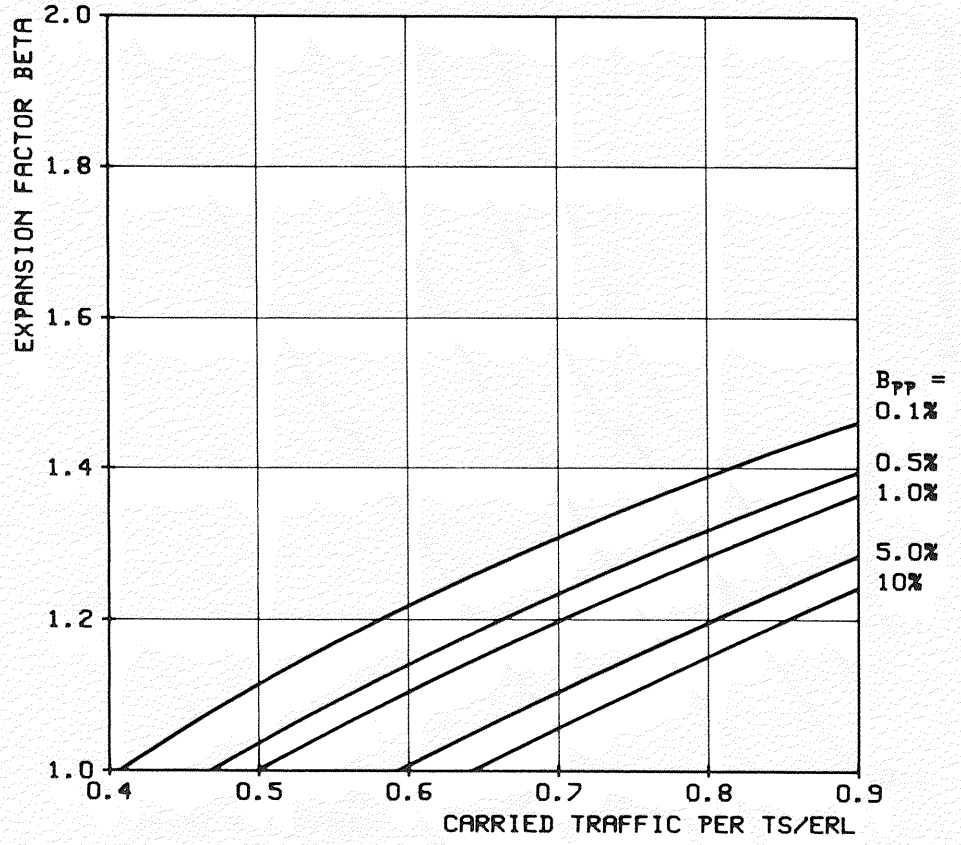


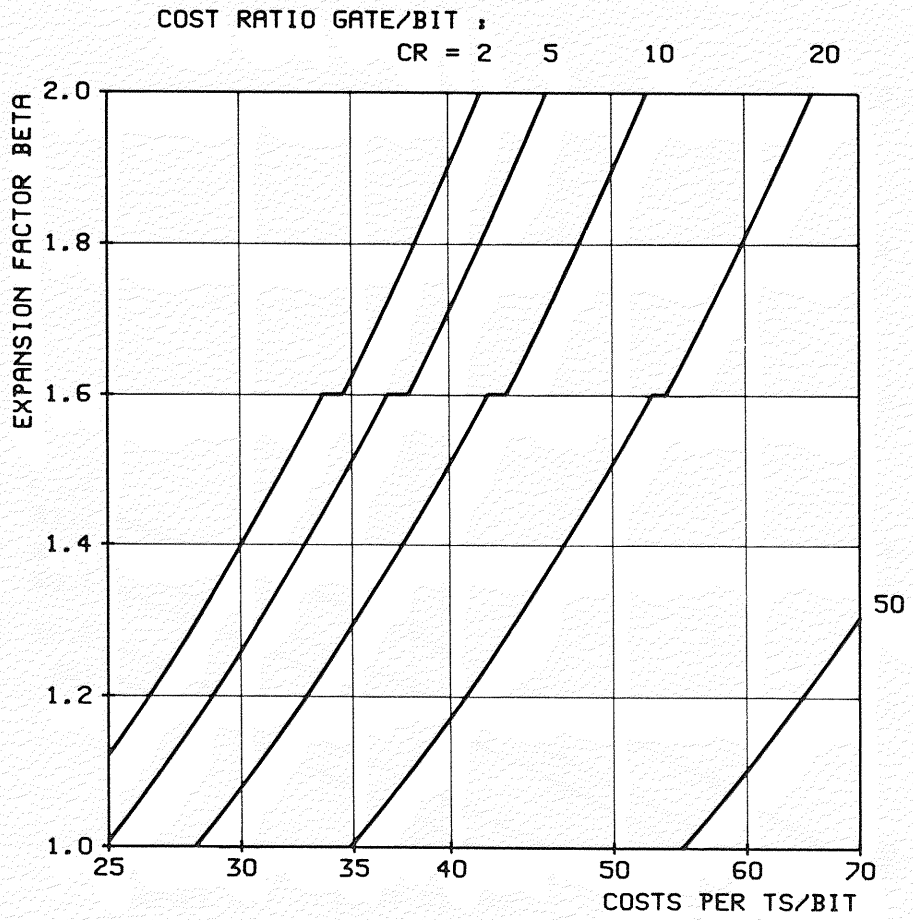


COMBINED SWITCHING 1 × 324 HW H_1 = 18
SEPARATED SWITCHING 2 × 324 HW M = 120

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

SSTSS

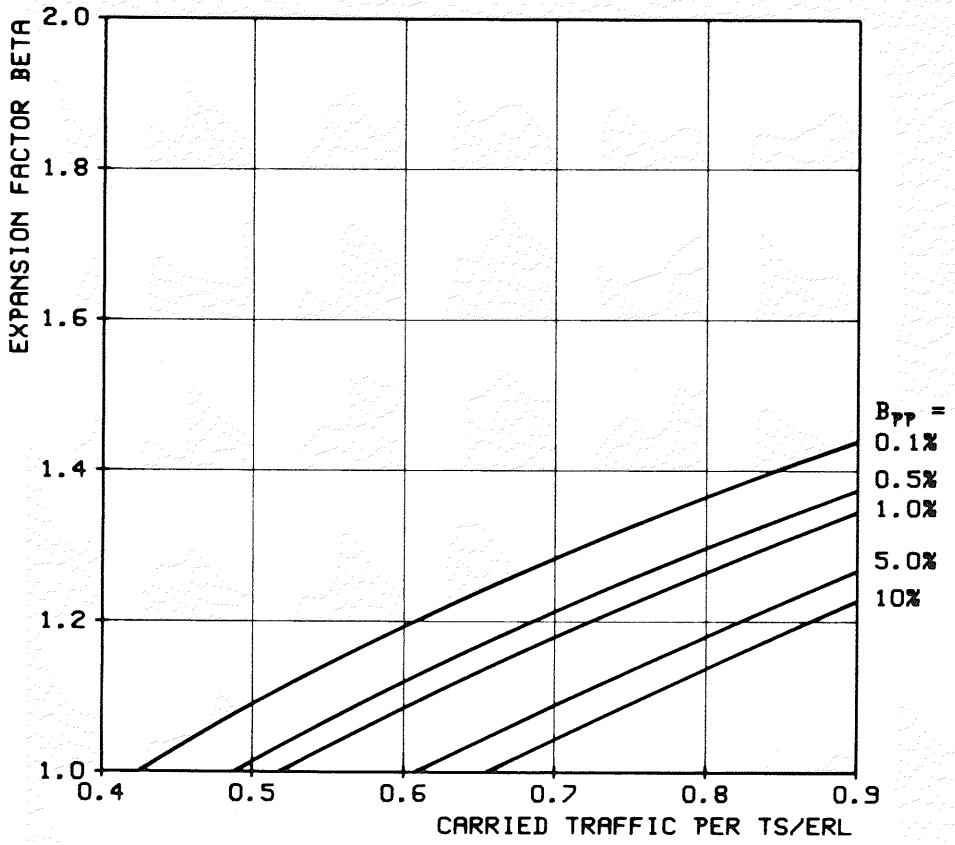


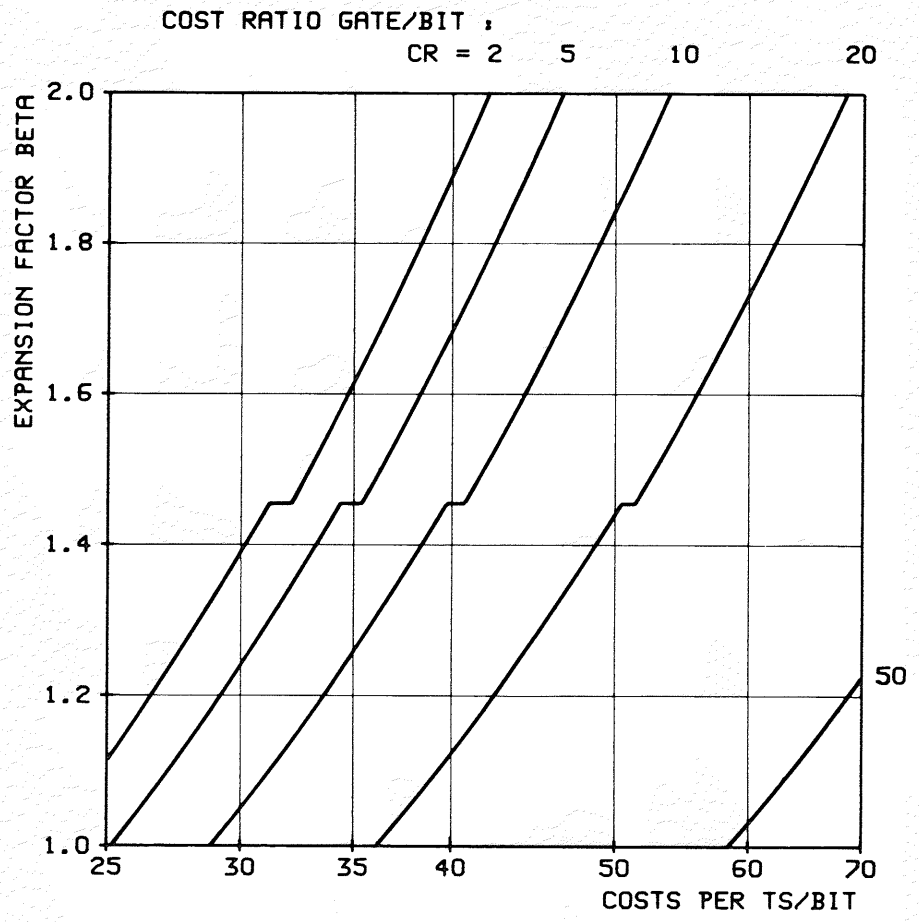


COMBINED SWITCHING 1 × 400 HW H_1 = 20
SEPARATED SWITCHING 2 × 400 HW M = 120

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

SSTSS

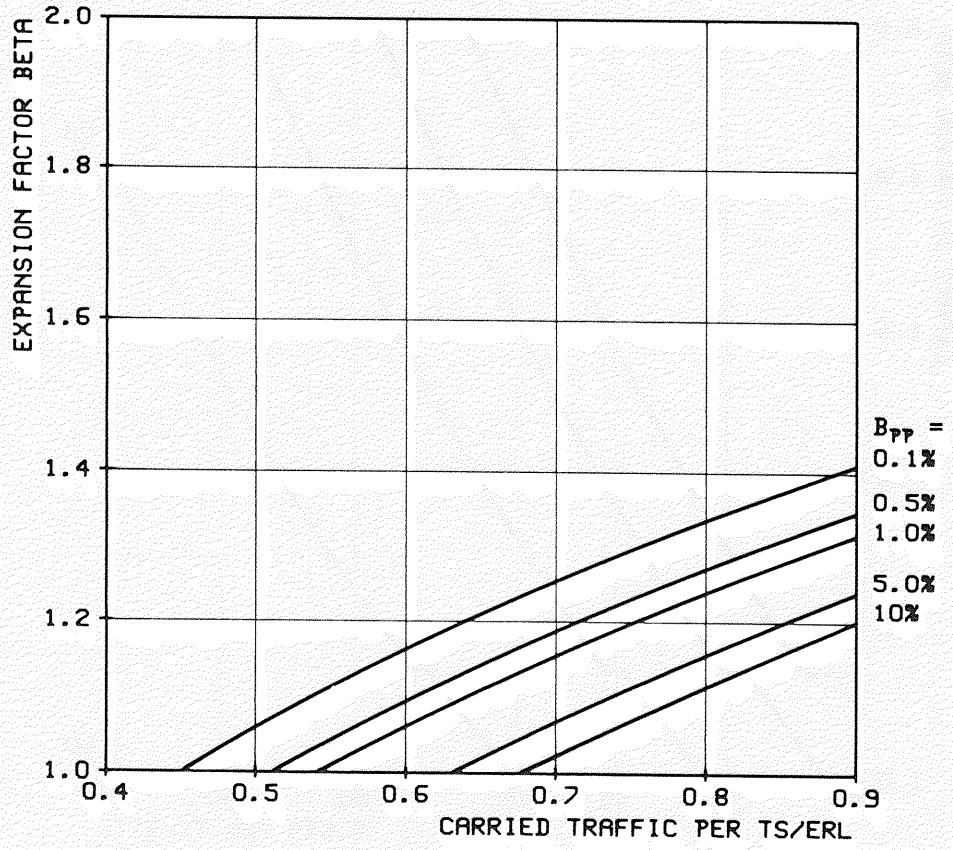


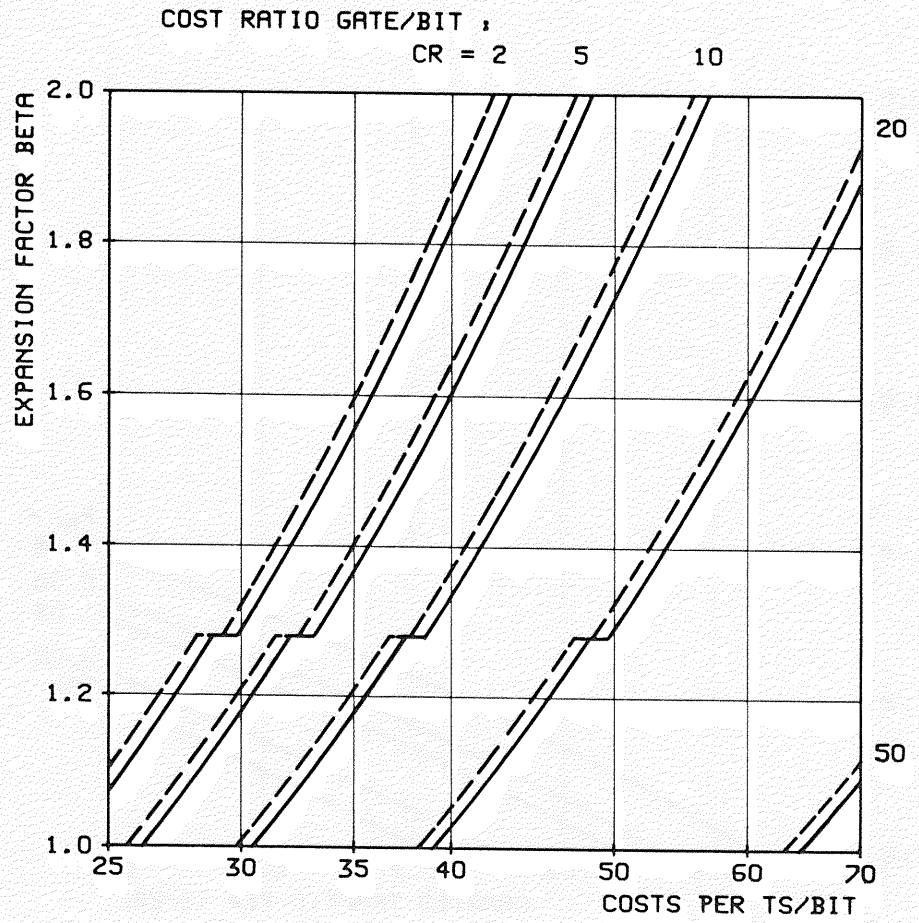


COMBINED SWITCHING 1 × 484 HW H_1 = 22
SEPARATED SWITCHING 2 × 484 HW M = 120

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

SSTSS





COMBINED SWITCHING 1 × 625 HW H_1 = 25

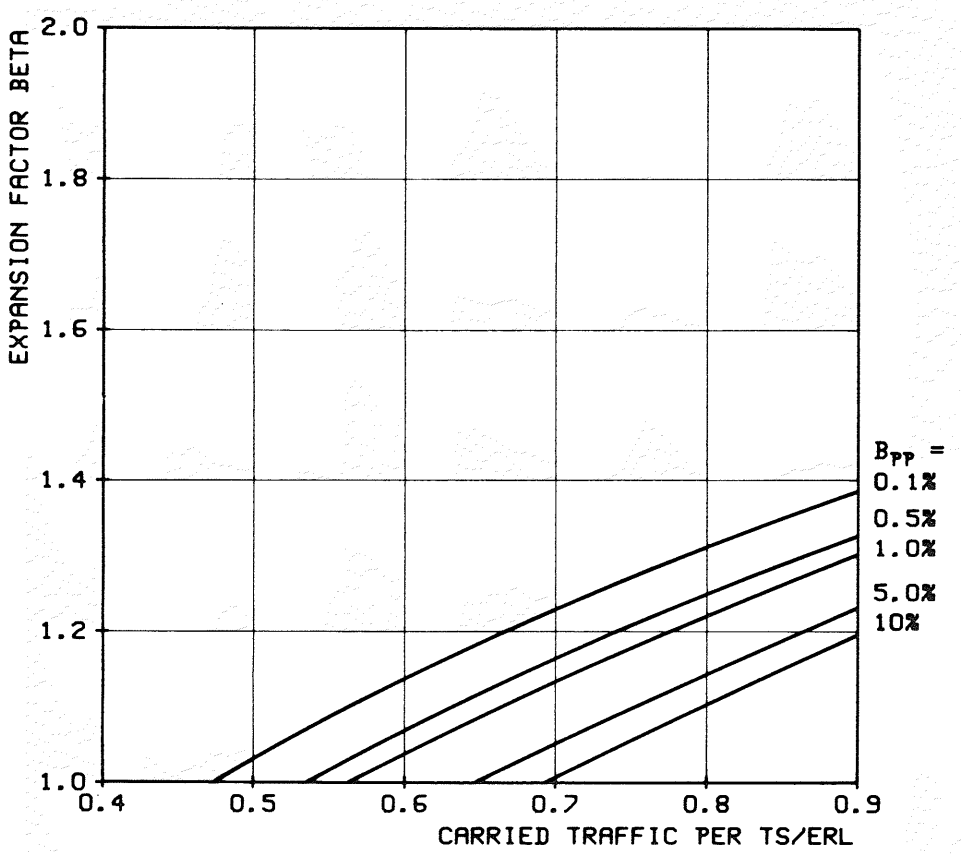
SEPARATED SWITCHING 2 × 625 HW M = 120

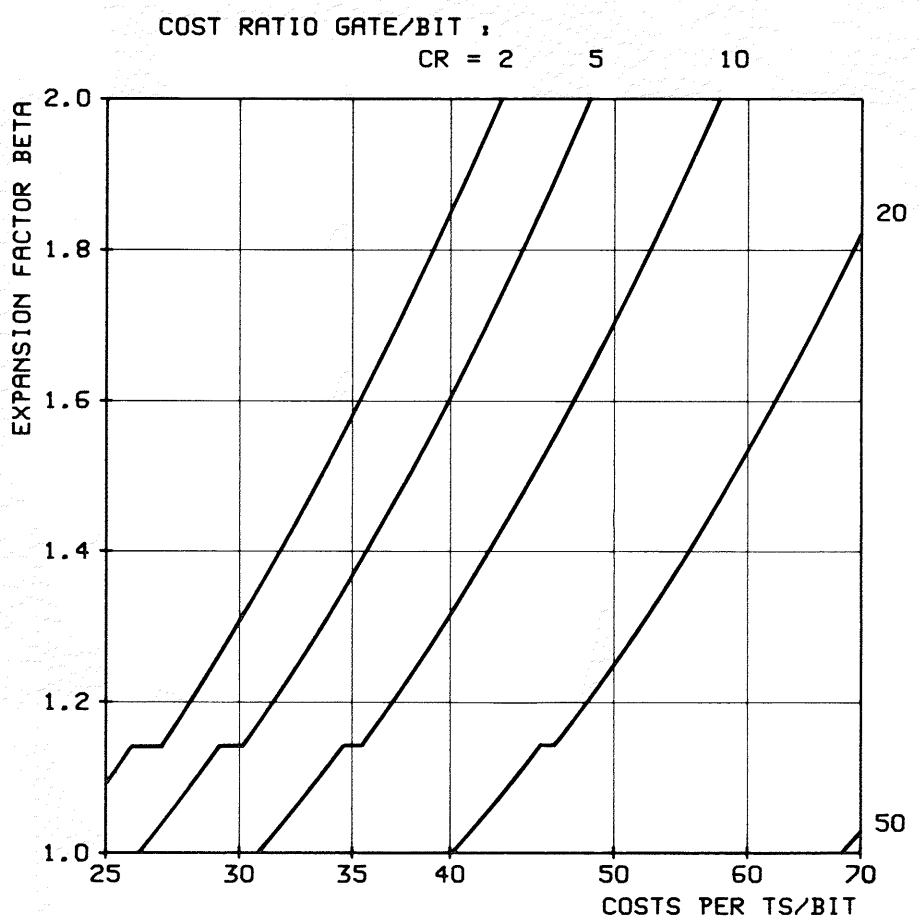
—— COMBINED SWITCHING

--- SEPARATED SWITCHING

-CHART 130-

SSTSS

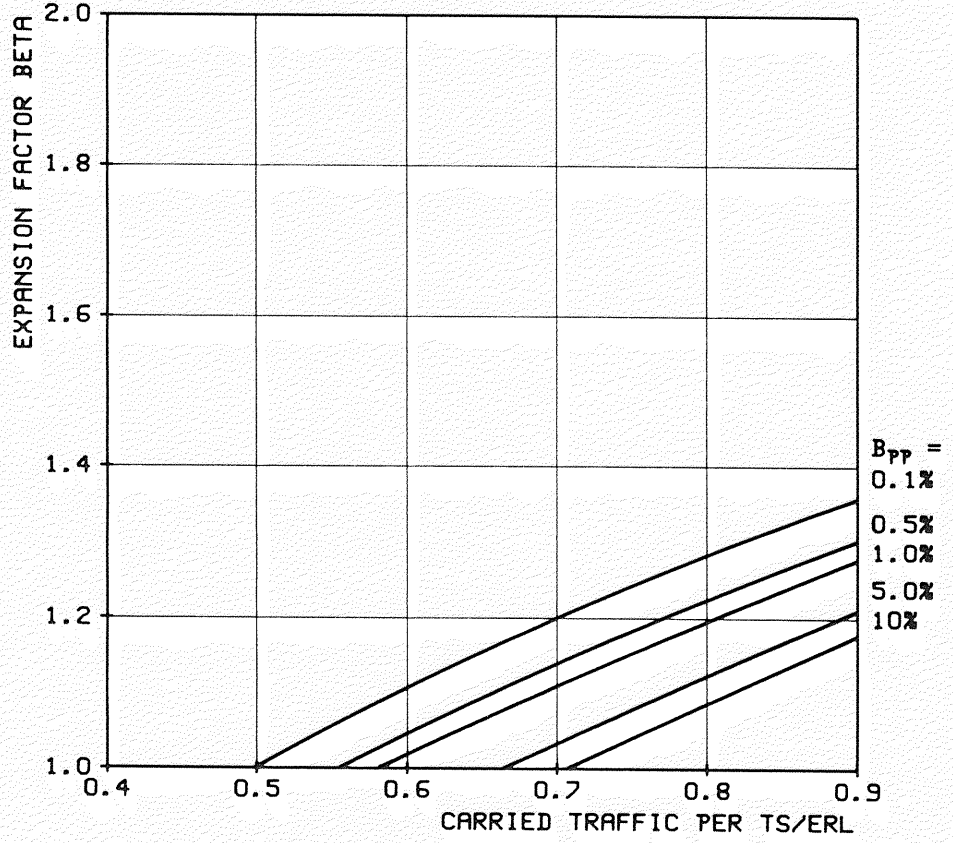


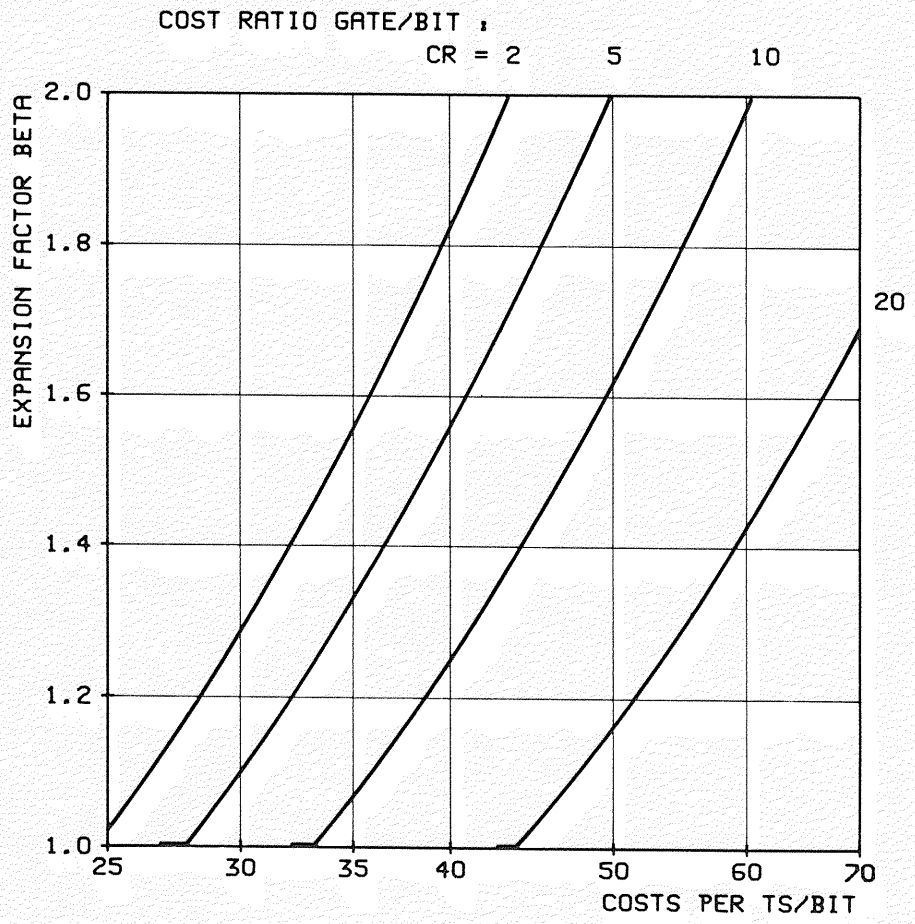


COMBINED SWITCHING 1 × 784 HW H_1 = 28
SEPARATED SWITCHING 2 × 784 HW M = 120

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

SSTSS





COMBINED SWITCHING	1 × 1024 HW	H_1 = 32	—— { COMBINED SWITCHING
SEPARATED SWITCHING	2 × 1024 HW	M = 120	{ SEPARATED SWITCHING

PCM SWITCHING ARRAY : TSSSSI

NUMBER OF HIGHWAYS (HW)

COMBINED SWITCHING : HW = 64, 125, 216, 343, 512, 729, 1000,

SEPARATED SWITCHING : HW = 128, 250, 432, 686, 1024, 1458, 2000,

TIME-SLOTS (TS) PER HW : M = 120 TS

POINT-TO-POINT LOSS, PCT1 : B_{PP} = 0.1, 0.5, 1.0, 5.0, 10.0%

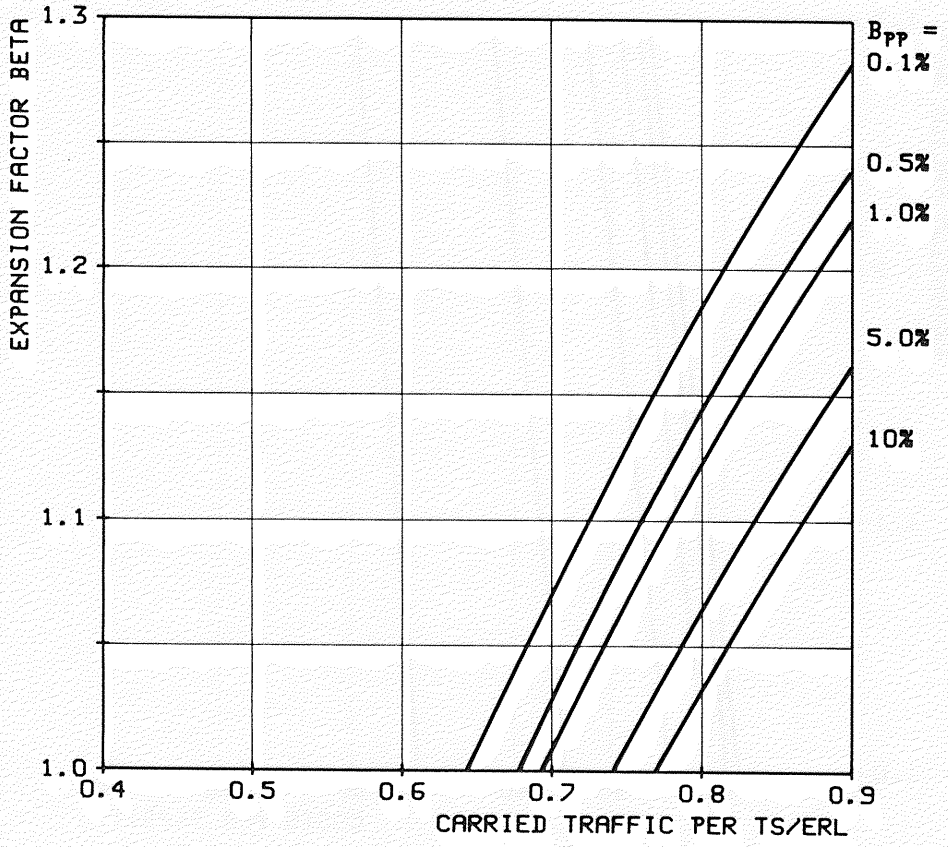
COST RATIO GATE/BIT : CR = 2, 5, 10, 20, 50, 100

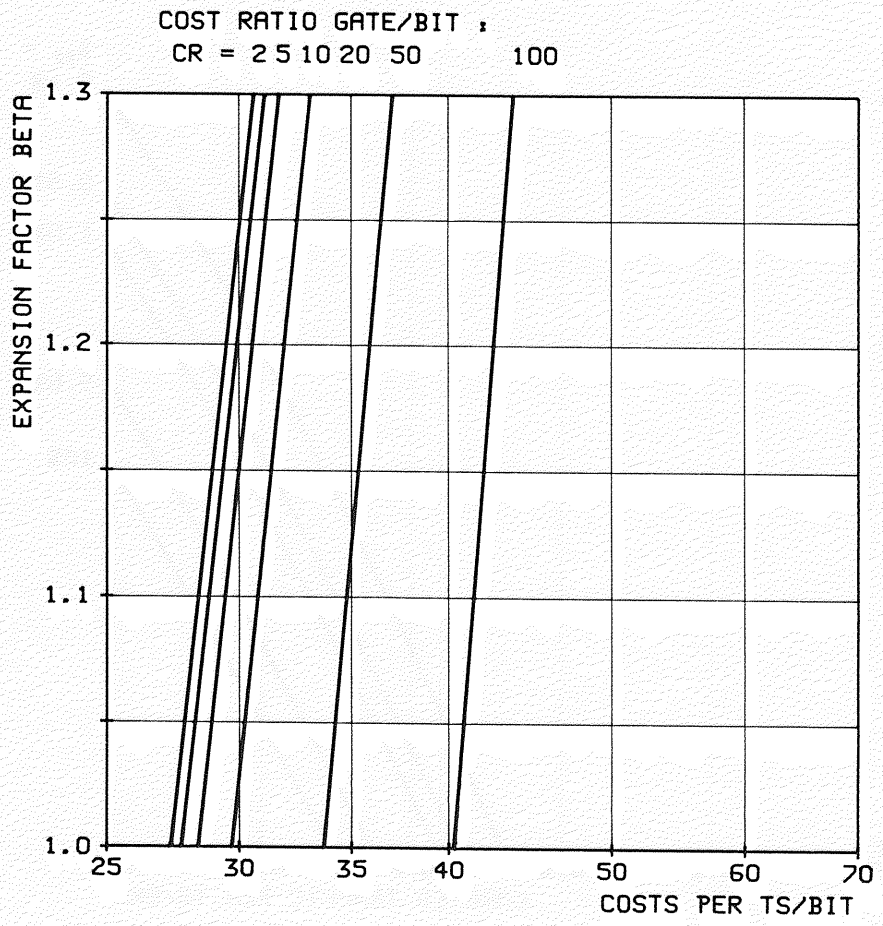
BLOCK SIZE

COMBINED SWITCHING : $H_2 = \sqrt[3]{HW}$

SEPARATED SWITCHING : $H_2 = \sqrt[3]{HW/2}$

TSSSST

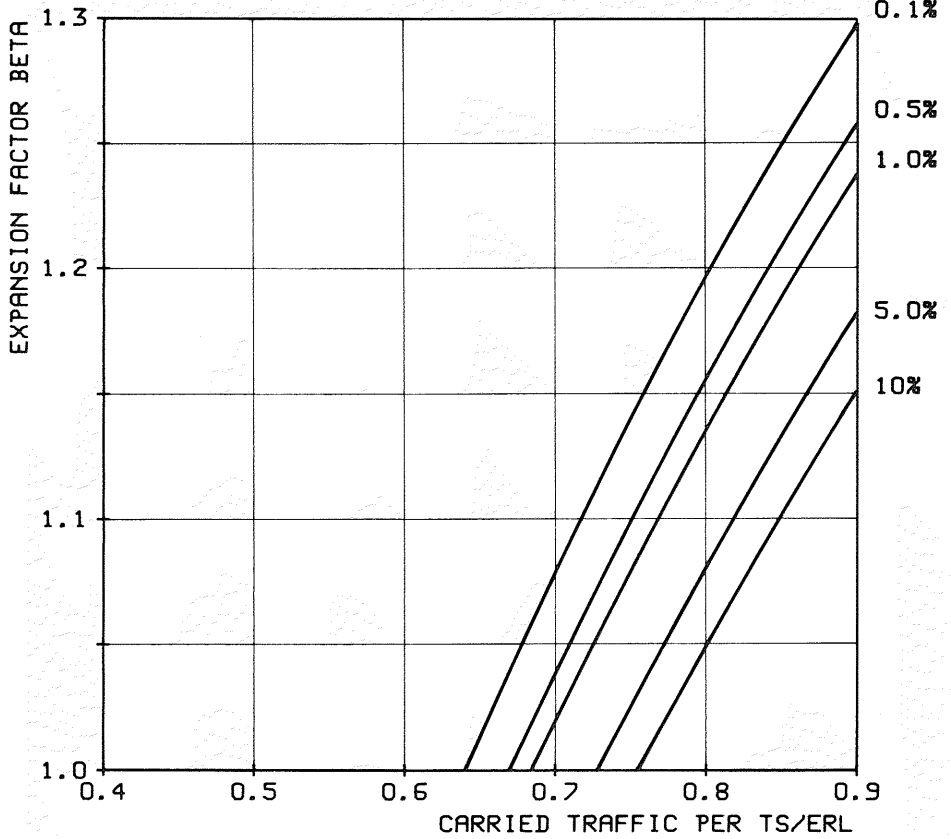


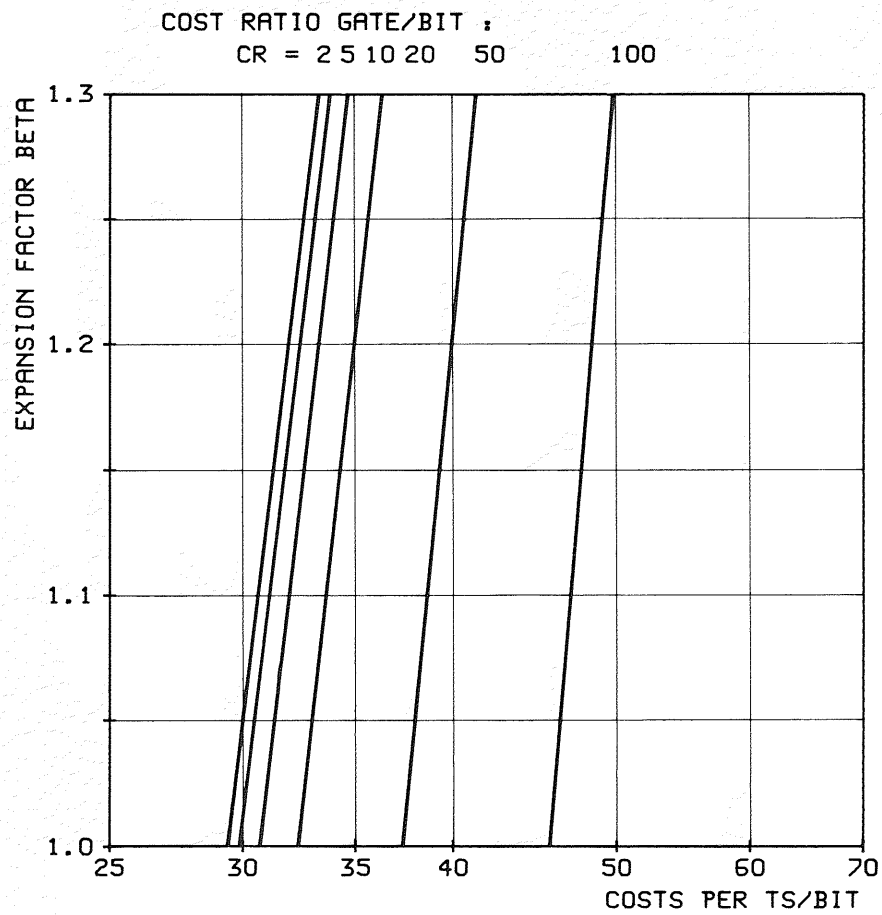


COMBINED SWITCHING 1 × 64 HW H_2 = 4
SEPARATED SWITCHING 2 × 64 HW M = 120

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

TSSSST

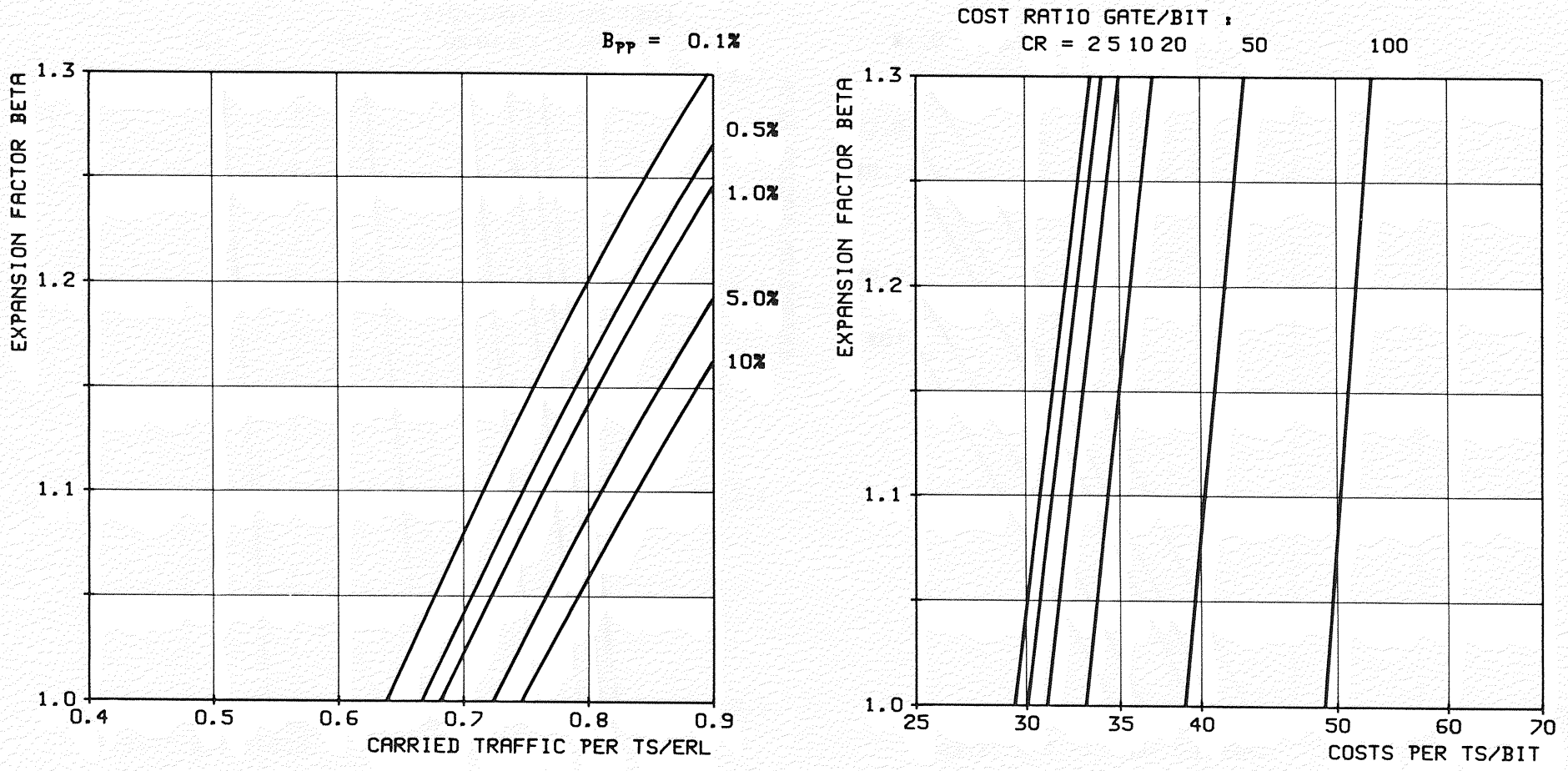




COMBINED SWITCHING 1 × 125 HW H_2 = 5
SEPARATED SWITCHING 2 × 125 HW M = 120

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

TSSSST

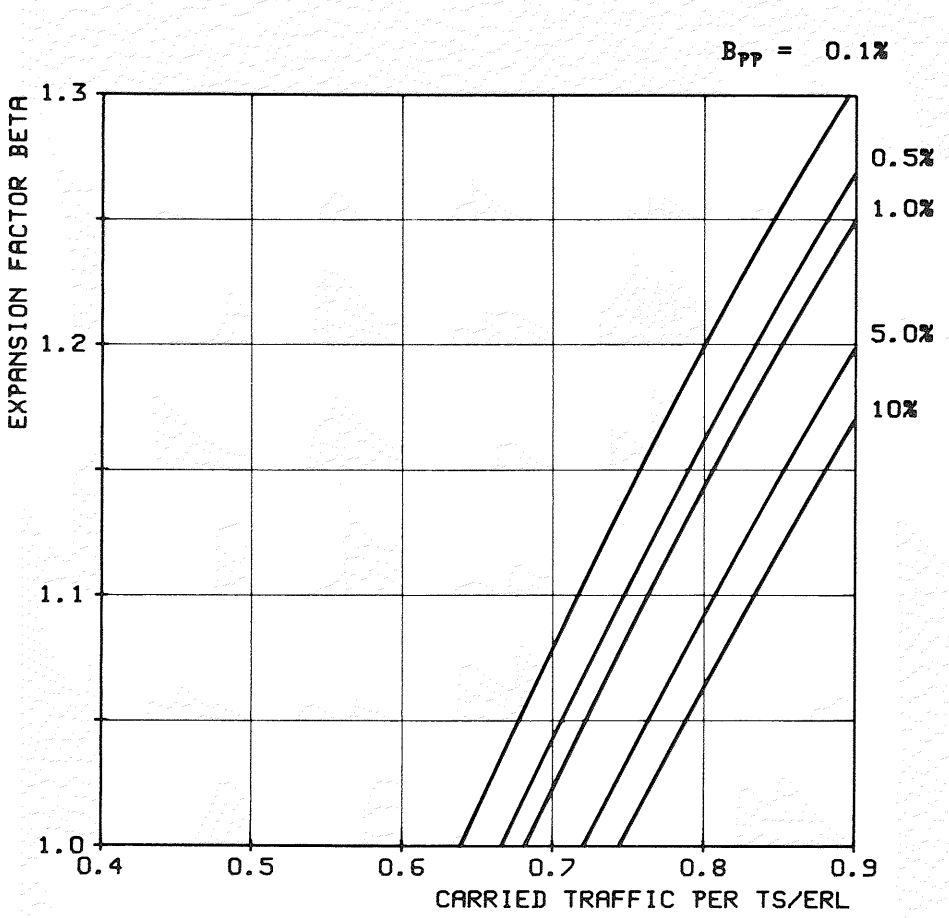


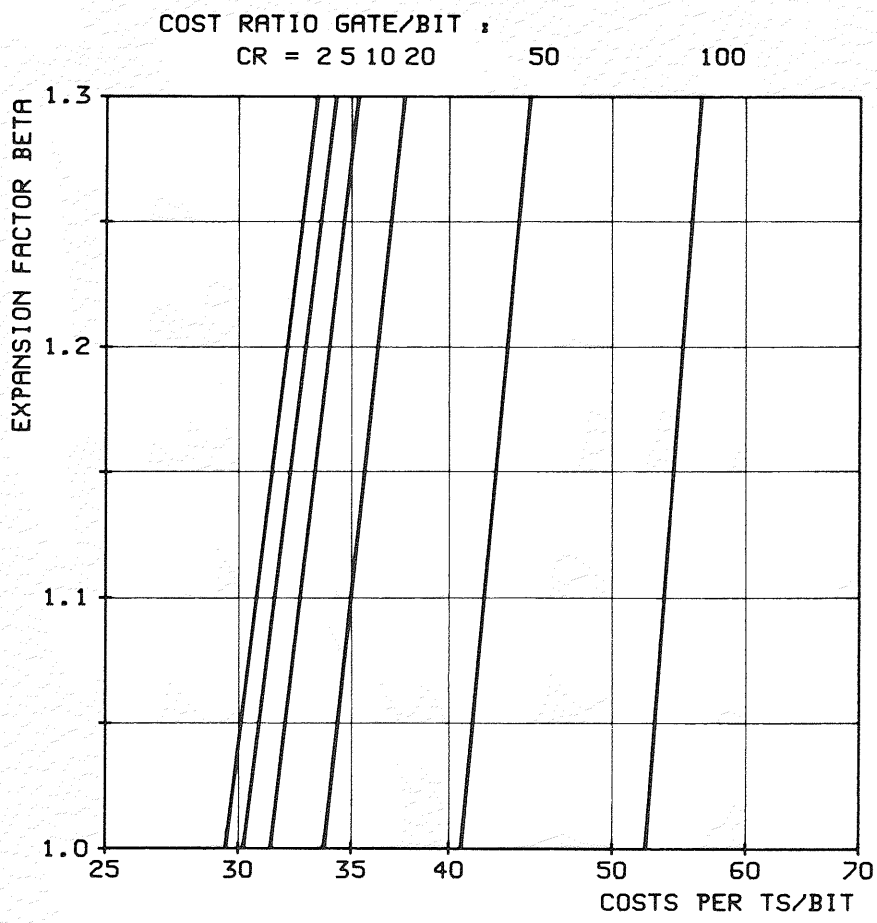
COMBINED SWITCHING 1 × 216 HW H_2 = 6
SEPARATED SWITCHING 2 × 216 HW M = 120

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

-CHART 135-

TSSSST

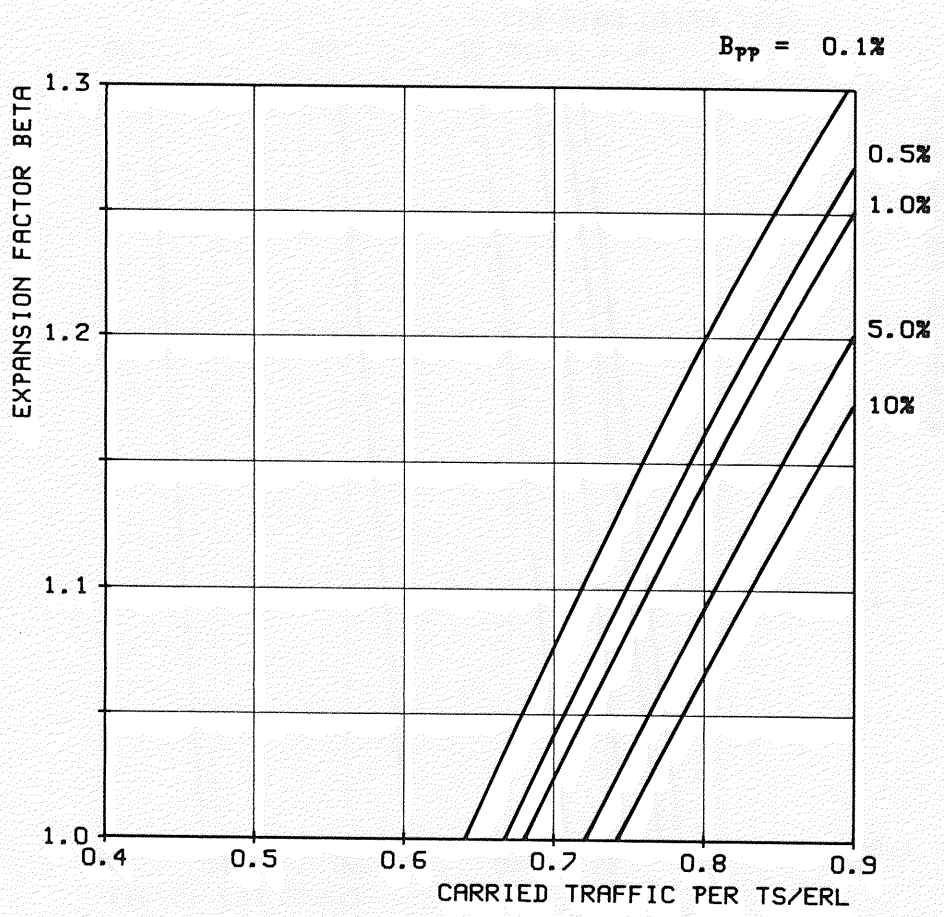


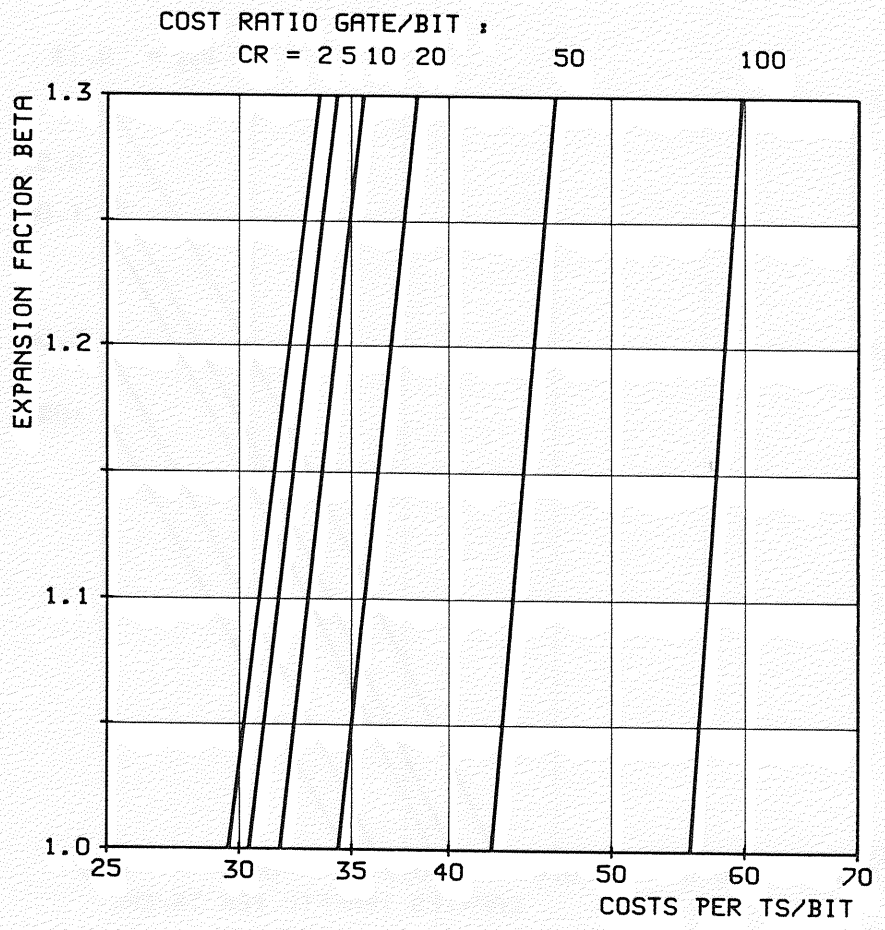


COMBINED SWITCHING 1 × 343 HW H_2 = 7
SEPARATED SWITCHING 2 × 343 HW M = 120

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

TSSSST

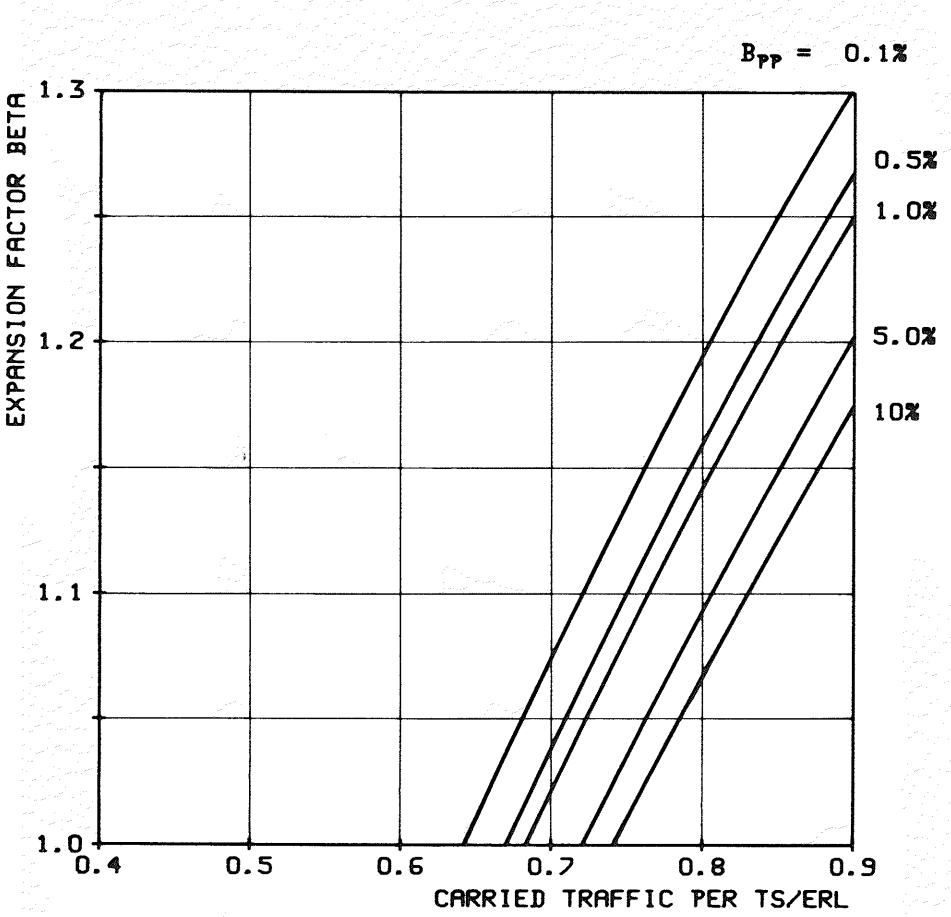


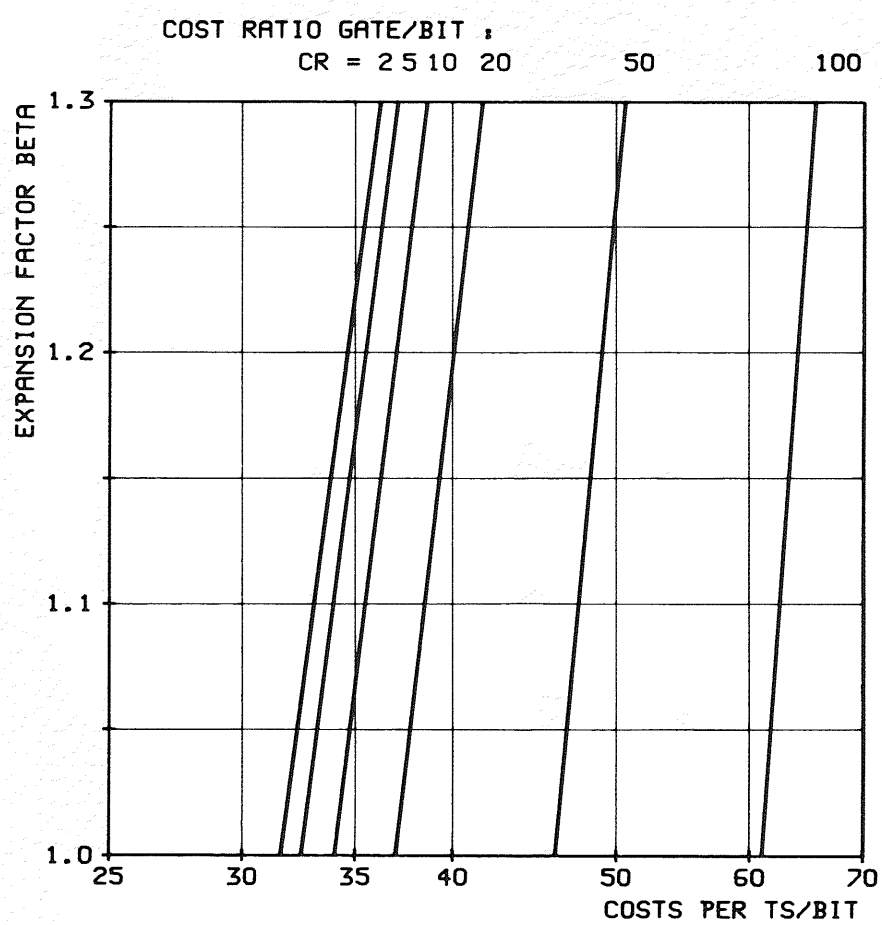


COMBINED SWITCHING 1 × 512 HW H_2 = 8
SEPARATED SWITCHING 2 × 512 HW M = 120

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING

TSSSST

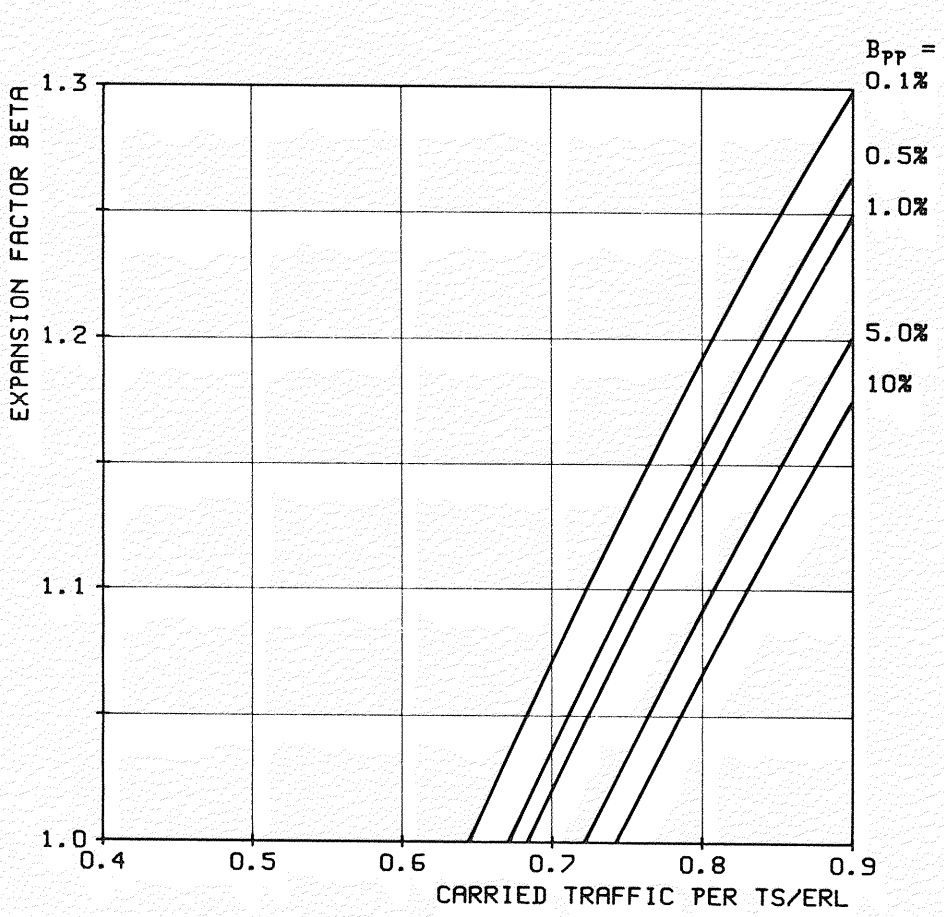


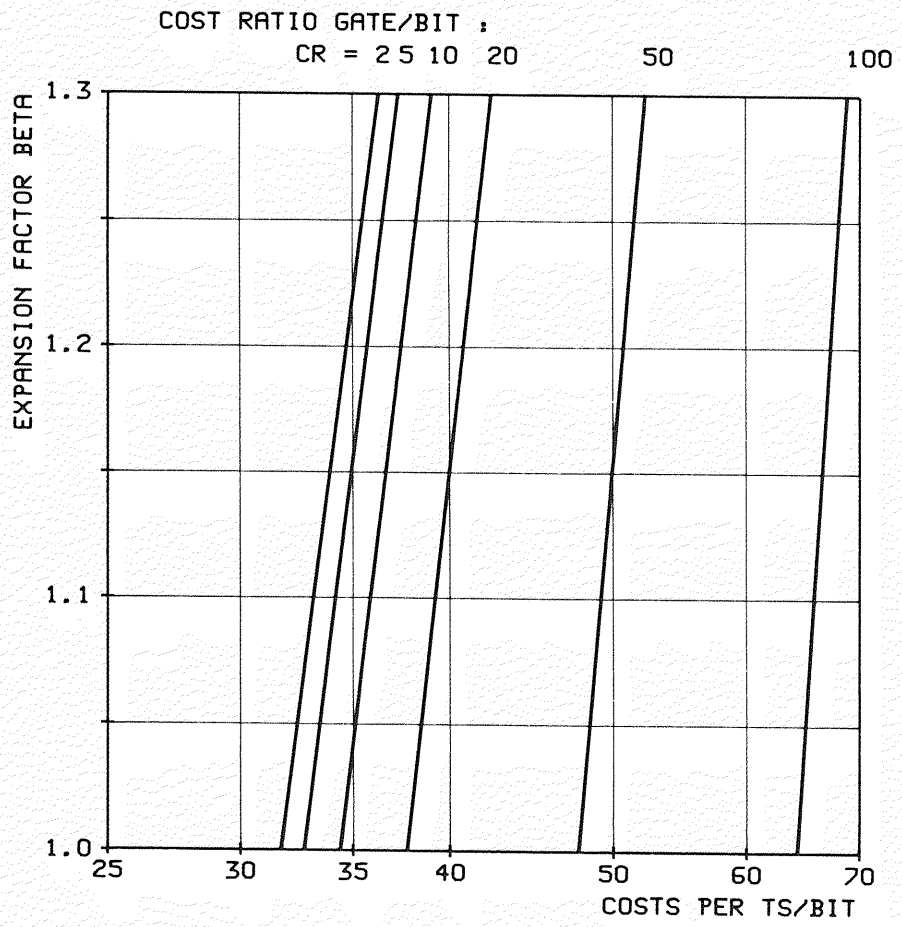


COMBINED SWITCHING 1 × 729 HW H_2 = 9
SEPARATED SWITCHING 2 × 729 HW M = 120

—— { COMBINED SWITCHING
{ SEPARATED SWITCHING

TSSSST





COMBINED SWITCHING 1 × 1000 HW H_2 = 10
SEPARATED SWITCHING 2 × 1000 HW M = 120

——{ COMBINED SWITCHING
{ SEPARATED SWITCHING