END-TO-END TRANSPORT DELAYS IN LOCAL AREA NETWORKS

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ABSTRACT

Decentralized computer communication systems are based on local area networks (LAN) which connect various users to a common transmission channel. This paper presents a modified structure of a LAN, supported by a multi-access-protocol, to improve the utilization of the network interfaces, to combine the advantages of the contention and reservation protocols, and to achieve high efficiency and stability. The performance aspects of the access stations, like processor scheduling, cluster-internal connections, buffer limitations, and bidirectional traffic conditions are discussed by the models of the network access controller (NAC) and the channel access module (CAM). The analysis identify the main factors contributing to the end-to-end-transport-delays in local area networks. It will be shown that the system performance is more dominated by the interface processing and queueing rather than by the channel access delays.

1. INTRODUCTION

The increasing need of flexibility and reliability in computer based communication systems and the decreasing costs of hardware components, e.g. communication controllers, lead more and more to dezentralized solutions for such distributed systems. Local area networks (LAN) form the interconnection and transmission subsystems for these systems within a limited area.
Two basic interconnection topologies have shown most practical among all investigated networks: Ring systems, like the Cambridge Ring or others [1,2], are actually a series of connections between the consecutive access stations and use active interfaces to connect the stations to the network, whereas bus systems like the Ethernet [3] consist of a passive common transmission channel, onto which all access stations tap.

To provide an integral transport-system for open systems interconnections the access stations to the local area network have to perform most of those functions which are defined in the levels 1 - 4 of the extended ISO-OSI reference model, taking into account the special structure of local area networks.

These functions are:

- synchronization
- access management
- data encapsulation/decapsulation
- establishment and release of connections
- sequence control
- flow control
- error detection and error recovery
- segmenting and concatenation of data
- transfer of data units (packets,frames)
- supervisory functions
- access station management

The functions of level 2a are covered by multi-access-protocols which are used in the LAN to assign the channel capacity to the competing users. The CSMA/CD protocol standing for the contention protocols, used in bus structured systems, and the Token Passing Scheme as a reservation protocol, used in ring stuctured systems, are the mostly known access protocols for LAN's and they have been accepted by ISO and IEEE as standards [11,12]. These protocols have been analyzed in great detail [4,5,6,7] and compared to each other [5,6], but if the additional functions of the access stations mentioned above are taken into account, it is clearly seen that the implemented access method may contribute only in part to the general performance of the system.
Additional performance aspects are the processing overhead at the access stations to execute the higher protocol functions, the times spent for the interactions between the different protocol levels, the management of buffers and processors within the access station, and the speed mismatch between the transmission channel, the access stations, and the attached devices.
In this paper, some of these performance aspects, particularly those caused by the network interface structure are considered in detail, and it is shown that the system performance may be more influenced by the interface processing and queueing rather than by the channel access protocol and the channel speed.

Section 2 describes the system architecture which is subdivided into 3 main functional layers: peripherals, network access controllers (NAC), and the communication subsystem, consisting of the channel access modules (CAM) and the transmission channel.

In Section 3 the system is modelled and divided into submodels which are analyzed separately: the network access controller, the channel access module, and the access protocol.

Finally, some of the main factors are identified which contribute to the end-to-end-transport delays in local area networks.

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2. SYSTEM ARCHITECTURE

The basic idea of local area networks is to provide a cost-effective communication system between computers, terminals, or I/O-devices within a spatially limited area. Under these conditions, decentralized structures become important using high speed carriers and integrated circuits. The demand of standardized interfaces and the need of higher protocol functions lead to a greater functionality of the network access points which results in higher costs. These costs can only be reduced by an effective use of the equipment, but this is contradicting to the large number of peripherals and their low traffic intensities.

To combine the main advantages of a common carrier local area network with the requirements of open systems interconnection, we conclude the following design requirements:

- a communication protocol with high throughput and low transfer times combining the advantages of contention and reservation protocols.
- a hybrid system structure with a decentralized communication subsystem and with network access stations clustering a limited number of peripheral devices, providing higher protocol functions for shared use, and guaranteeing economic use of the implemented resources.

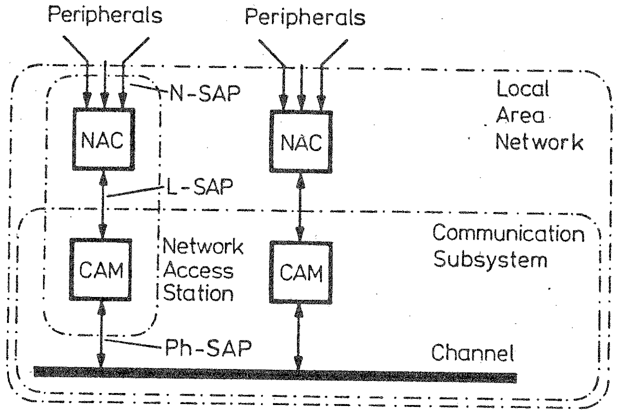

Fig. 1 System structure

NAC	network access controller
CAM	channel access module
N-SAP	network service access point
L-SAP	link service access point
Ph-SAP	physical service access point

Fig.1 shows the basic system structure of the considered system. The peripheral devices are connected to the common transmission channel by the network access stations (NAS) in a clustered manner via the network service access points (N-SAP). The access stations are subdivided into two parts: the network access controller (NAC) and the channel access module (CAM).
The NAC provides basically the functions of levels 2b and 3 of the ISO-OSI-reference model; It consists of I/O-interface modules for the realization of terminal and host protocols, a microprocessor based control module for the call functions and for internal supervisory functions, a main data storage module and an interface module connecting the NAC to the communication subsystem, consisting of the CAM's and the common channel.
This interface represents the link service access point (L-SAP). The CAM performs the functions of layers 1 and 2a which have essentially to be processed at the speed of the common channel, e.g. synchronization, carrier sensing, collision detection, processing of frame control information, and intermediate buffering of frames. The CAM interfaces with the common channel by the physical service access point (Ph-SAP). Communication among the channel access modules runs under the control of a carrier-sense-multiple-access-protocol with collision detection and access conflict resolution by dynamic send priorities (CSMA-CD-DP) [8]. The send priorities are realized by staggered transmission delays which refer to the maximum propagation delay and the number of connected NAS's.

This 3-level structure (instead of the commonly discussed simple 2-level-structure) has the following advantages:

- Reduction of the number of access points
- Economic use of the common channel by minimizing the access control overhead
- Shared use of higher network protocol functions by the clustered peripherals.

3. MODELLING AND PERFORMANCE ANALYSIS

3.1 System Modelling

Besides the costs being involved by hardware and software implementation, the usefulness of a distributed system depends heavily on its throughput and delay performance. These characteristics are most sensitive to resource allocation, overhead, and traffic statistics.
The quantitative qualification is subject to modelling and performance analysis.

The main topics are:

- throughput and delay
- system response with respect to unbalanced load and dynamic overload
- identification of the most influencing system parameters
- optimization of system parameters.

Due to the complexity of the system, the complete model is subdivided into three submodels:

- the network access controller (NAC)
- the channel access module (CAM)
- the access protocol (CSMA-CD-DP).

These submodels are treated individually to identify the main influencing parameters.

3.2 The Network Access Controller

3.2.1 Modelling

Besides the call control functions, the main communication processing functions of the NAC are:

- receiving of data units from the peripherals
- transmission of data units to the peripherals
- packetizing/depacketizing of data
- buffering of data and packets
- address processing
- transmission of packets to the CAM
- receiving of packets from the CAM

These functions are the mostly time consuming ones and due to the bidirectional characteristic of the traffic, the internal structure of the NAC has to be considered carefully. The grouping of the functions into sending and receiving direction leads to the basic submodel of the NAC as a processor model with four server phases, see Fig 2.

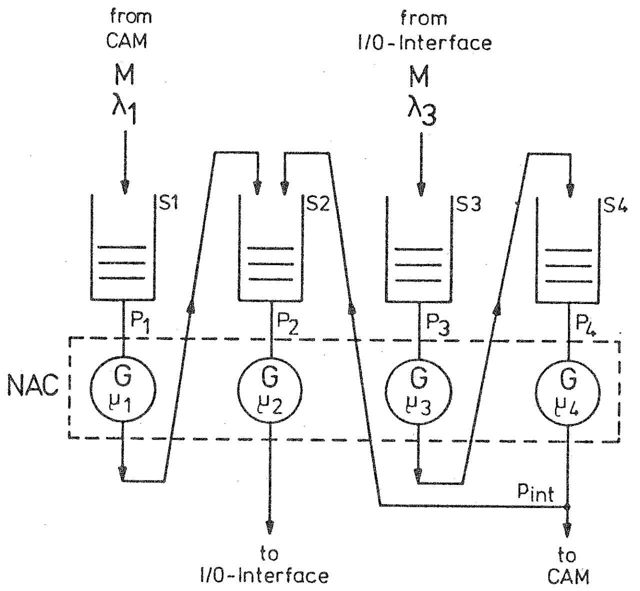

Fig. 2 Queueing model of the network access controller (NAC)
P_i: priority level of queue i

Phase 1 describes the transmission of received data units from the CAM-buffer to the NAC-data-buffer, including serial/parallel conversion, data decapsulation, address processing, sequence and flow control.
Phase 2 corresponds to those functions which are used for the transmission of data units to the different attached devices via the I/O-interfaces.
Phase 3 describes the transmission from the I/O-interfaces to the input buffer within the NAC. Collecting the data by the I/O-interfaces is assumed to run in parallel and is therefore covered by this phase. The completion of the arrivals of data units at the NAC-input-buffer is described by negative exponentially distributed interarrival times. This phase includes the time for data encapsulation and address processing, too.
Phase 4 deals with the transmission of ready data packets from the NAC-data-buffer into the CAM-buffer. This phase includes the parallel/serial conversion and the processing time for sequence and flow control.
Internal connections within the cluster of peripherals via the access station are modelled by the additional linkage from phase 4 to queue 2 and the branching probability p_{int}.

The priority schedule by which the different processor phases are activated will be discussed in Section 3.2.2 and the cluster-internal connections are considered in Section 3.2.4.

The analysis is carried out by a mean value analysis and workload considerations, depending on the actual priority schedule.

The most important results of this model are:

- the flow times through the NAC for sending and receiving direction
- the resulting queue lengths and, therefore, the determination of the NAC storage capacity.

The flow times through the NAC are defined as follows:

$$
\begin{aligned}
T_{Rec.} &= \text{Waiting time in CAM-buffer} && (S1)\\
&+ \text{Service time in phase 1} &&\\
&+ \text{Waiting time in NAC-data-buffer} && (S2)\\
&+ \text{Service time in phase 2} &&
\end{aligned}
$$

$$
\begin{aligned}
T_{Send} &= \text{Waiting time in input-buffer} && (S3)\\
&+ \text{Service time in phase 3} &&\\
&+ \text{Waiting time in NAC-data-buffer} && (S4)\\
&+ \text{Service time in phase 4} &&
\end{aligned}
$$

The offered load is defined by:

$$\rho = \lambda_1/\mu_1 + \lambda_1/\mu_2 + \lambda_3/\mu_3 + \lambda_3/\mu_4$$

3.2.2 Processor Schedules

The first problem which arise in the structuring of the NAC and which is treated by the presented model is the scheduling of the processor phases.

To minimize the overhead, the scheduling of the phases follows a nonpreemptive priority scheme.

Giving highest priorities to the processing of foreign data units guarantees the fastest clearing of received data from the CAM.
However, if the NAC gets no packets through to the CAM-buffer, since there are always packets to receive, the station will waste its access rights and the station throughput will be degraded.
If priority is given to the sending direction, the CAM-send-buffer could be overloaded and packets sent by other stations and arriving at the considered station in sequence (back-to-back packets) will block the capacity of the common channel, due to the overloading of the CAM-receive-buffer. Therefore the channel throughput will be degraded.
Giving higher priorities to phases 1 and 3 raises the throughput of the I/O-interfaces and the CAM-buffers, but the NAC-data-buffer could be overloaded and the flow times are increasing. On the other hand, if phases 2 and 4 get the higher priorities, the necessary capacity of the NAC-data-buffer is minimized and the flow times through the NAC are decreasing.

3.2.3 Results

Tab.1 gives an overview of the resulting waiting times in each queue for some selected schedules. The formulae given in Tab.1 have been found by application of residual service times from renewal theory and Little's theorem, see, e.g. [10].

Fig. 3a,b displays results about the flow times through the NAC for the receiving and sending direction and for all priority schedules.
The arrival rates are symmetrical and the service times are exponentially distributed with mean 1.0 for each of the four phases. It is assumed that cluster-internal connections do not exist ($p_{int} = 0.0$).

P_1 P_2 P_3 P_4	$E[T_{W1}]$	$E[T_{W2}]$	$E[T_{W3}]$	$E[T_{W4}]$
2 1 4 3	$\dfrac{E[T_R] + \rho_1 h_2}{1-\rho_1-\rho_2}$	0	$\dfrac{E[T_R] + \rho_1 h_2 + \rho_3 h_4}{(1-\rho_1-\rho_2-\rho_3-\rho_4)(1-\rho_1-\rho_2)}$	$\dfrac{h_3(\rho_1+\rho_2)}{1-\rho_1-\rho_2}$
1 2 4 3	$\dfrac{E[T_R]}{1-\rho_1}$	$\dfrac{\rho_1+\rho_2}{1-\rho_1-\rho_2}\left[\dfrac{E[T_R]}{1-\rho_1} + h_1\right]$	$\dfrac{E[T_R] + \rho_1 h_2 + \rho_3 h_4}{(1-\rho_1-\rho_2-\rho_3-\rho_4)(1-\rho_1-\rho_2)}$	$\dfrac{h_3(\rho_1+\rho_2)}{1-\rho_1-\rho_2}$
3 1 4 2	$\dfrac{E[T_R] + \rho_1 h_2 + \rho_3 h_4}{1-\rho_1-\rho_2}$	0	$\dfrac{E[T_R] + \rho_1 h_2 + \rho_3 h_4}{(1-\rho_1-\rho_2-\rho_3-\rho_4)(1-\rho_1-\rho_2)}$	0

Tab. 1 Waiting times within the NAC-queues for selected processor schedules ($p_{int} = 0.0$)

$h_i = 1/\mu_i$	average service time	$\rho_i = \lambda_1/\mu_i$ $i = 1,2$	utilization phase 1,2
P_i	priority level queue i	$\rho_j = \lambda_3/\mu_j$ $j = 3,4$	utilization phase 3,4
$E[T_R] = 0.5 \cdot \sum_{i=1}^{4} \rho_i h_i (1+c_{hi}^2)$		c_{hi}	service time coeff. of variation

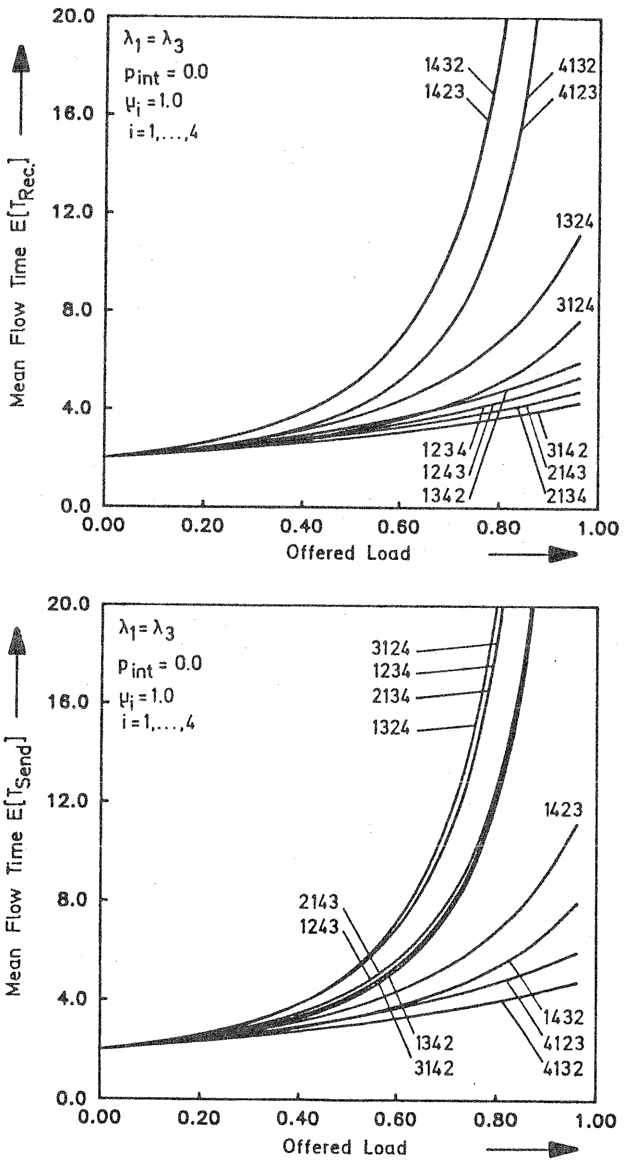

Fig. 3a,b Flow times vs. offered load
NAC processor schedules

3.2.4 Cluster-Internal Connections

The clustering of peripheral devices to one network access station allows the connection of two devices without using the communication subsystem. Only the NAC to which these devices are attached, is involved in the connection.
Data units belonging to an internal connection arrive at the NAC-input-buffer and will be processed like all other data units. After recognition of the address information, the NAC-processor decides to route back these data units to the NAC-data-buffer used for ready data units which will be sent to the I/O-interfaces. The processing of connections among devices attached to the same NAC results in an additional processor load, because these connections use functions of the sending and receiving path within the NAC simultaneously.

Hence, the processor load is given by:

$$\rho_{tot} = \lambda_1/\mu_1 + \lambda_1/\mu_2 + \lambda_3/\mu_3 + \lambda_3/\mu_4 + p_{int}\lambda_3/\mu_2$$

Fig. 4a,b displays the flow times versus the offered load for a representative schedule (1234) and for different probabilities of cluster-internal connections. The arrival rates are again assumed to be symmetrical and the service times are exponentially distributed with mean 1.0 for each phase.
The results for $p_{int} = 0.0$ and $p_{int} = 1.0$ are the limiting cases of the model; for $p_{int} = 0.0$ there exists no cluster-internal connection and for $p_{int} = 1.0$ no data units are sent to the CAM.

Cluster-internal connections influence especially the sending direction of the NAC. However, the increasing of the flow times in the receiving direction are rather small.

3.2.5 Limited Buffer Capacity and Buffer Partitioning

The basic model of the NAC, given in Section 3.2.1 does not take into account the limitations of the NAC-data-buffers and gives only global criterions for the optimization of the buffer-partitioning.

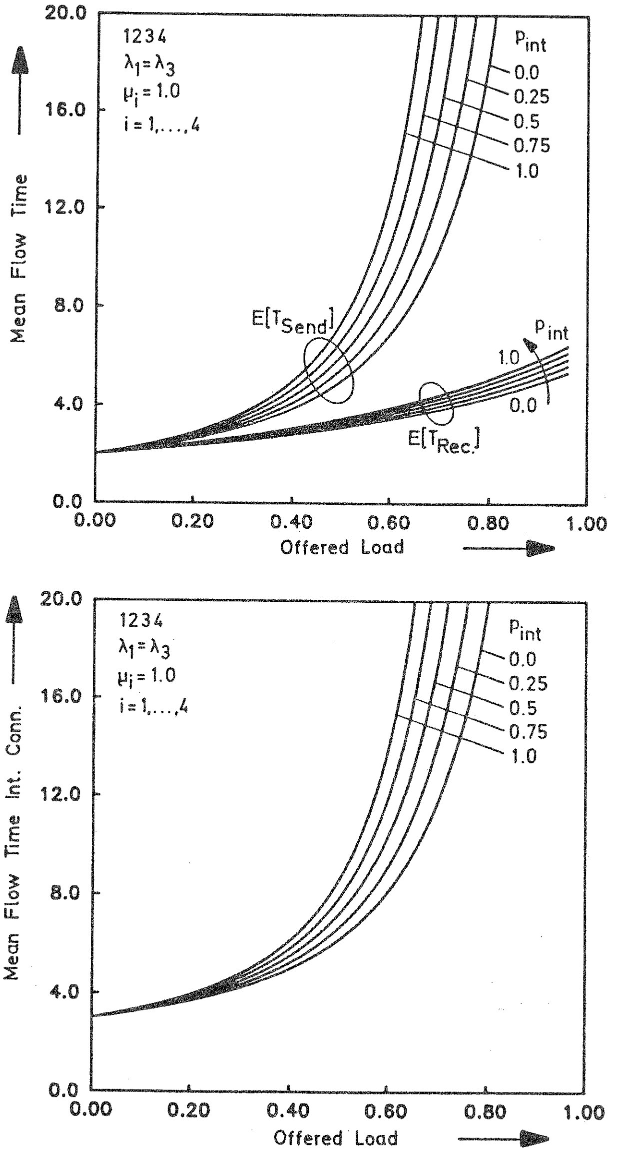

Fig. 4a,b Flow times vs. offered load Cluster-internal connections

Therefore, a model with limited queue lengths has been developed and analyzed for Markovian arrival and service processes. Additionally the processor schedule is extended to avoid internal blocking: Reaching a preset capacity limit of the storage, highest priority is given to the phases 2 and 4 to empty the buffers.

This model allows the dimensioning of the NAC-buffers, particularly for nonsymmetrical traffic characteristics. Fig. 5 shows the resulting flow times for sending and receiving direction for different buffer capacities. The arrival rates are assumed to be symmetrical, the service rates are equal for all phases with mean 1.0, and cluster-internal connections do not exist ($p_{int} = 0.0$).

Due to the limited buffer capacities, the blocking probabilities are rapidly increasing [9]. Therefore, the number of accepted data units is limited for increasing offered load and the flow times are bounded. The increase of the flow time for the receiving direction, compared to Fig. 3a, is the result of the processor schedule extension to avoid internal blocking.

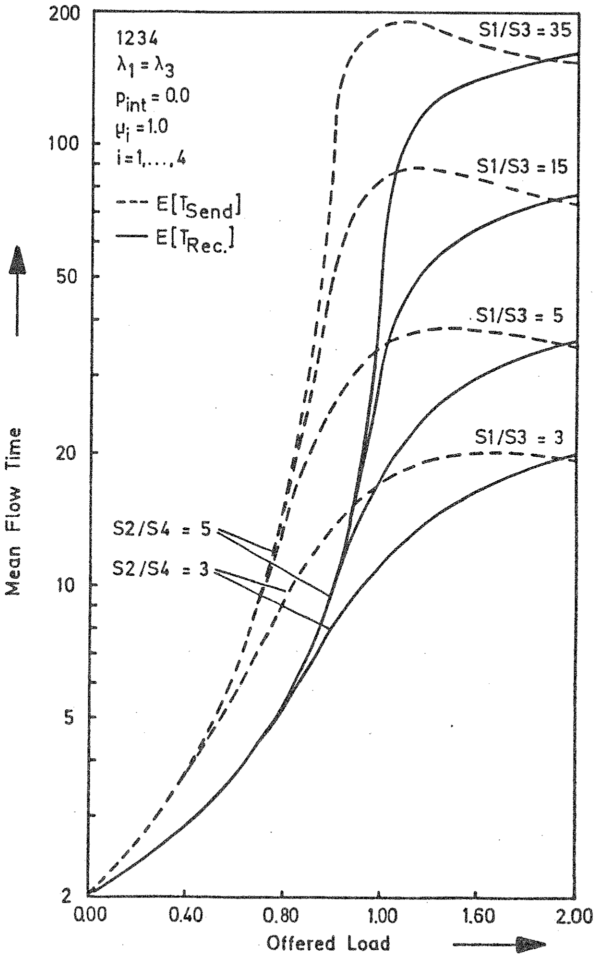

Fig. 5 Flow times vs. offered load Limited NAC-buffer-capacities

3.3 The Channel Access Module

3.3.1 Modelling

Apart from processing the access protocol functions, the channel access module has to buffer incoming or outgoing packets to balance the speed mismatch between network access controller and channel. This is done by a double buffering mechanism for the sending and receiving direction, respectively. To consider the bidirectional behaviour of the channel access module the model shown in Fig. 6 was developed. The NAC is represented by the two transfer phases from and to the CAM-buffers. The common channel is modelled by two server phases standing for the transmission of departing and arriving data-frames.

3.3.2 Analysis

For Markovian arrival and service processes the performance analysis is based on establishing the multi-dimensional state-space and solving the resulting state-equations explicitly.

Results are obtained about the waiting times within the CAM, the flow times through the CAM, and the blocking probabilities of the CAM-buffers for bidirectional traffic assumptions.

Fig. 7 displays the flow times versus the offered channel load for different NAC processor speeds. It is clearly indicated that the speed mismatch between the channel and the NAC is the main factor contributing to the delays within the CAM.

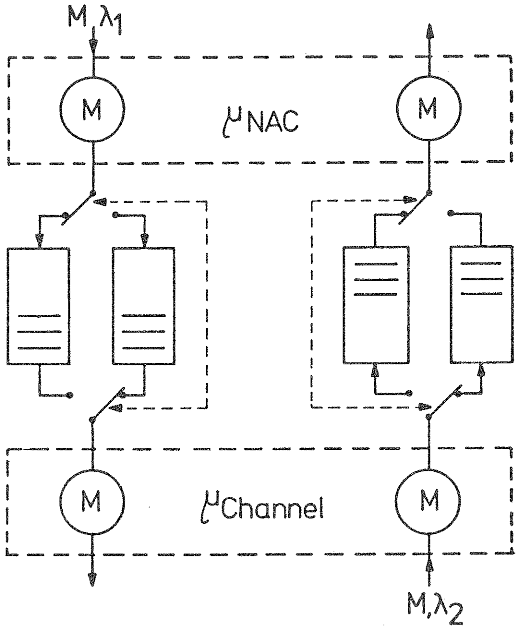

Fig. 6 Queueing model of the channel access module (CAM)

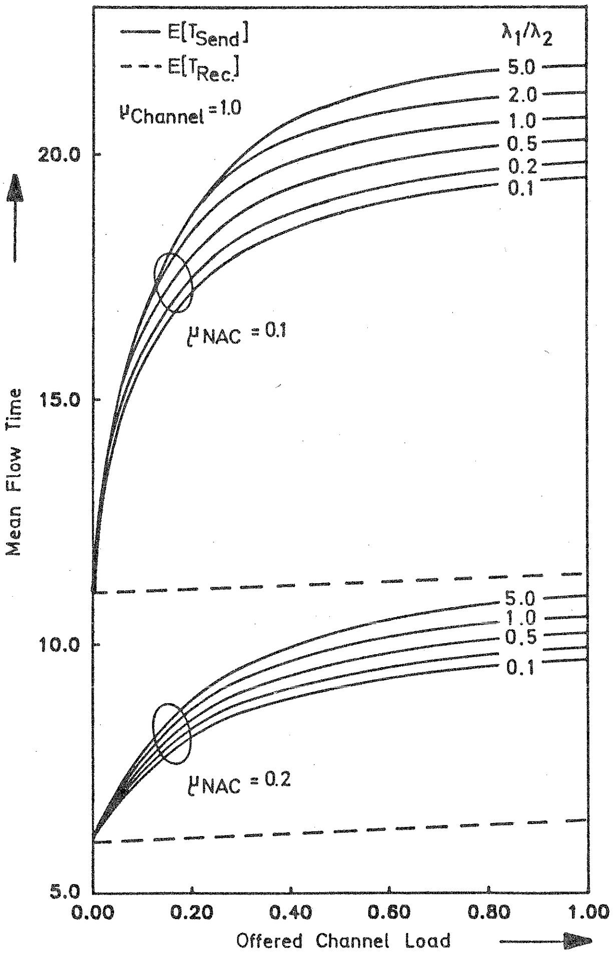

Fig. 7 Flow times vs. offered channel load Bidirectional double buffering model

An increase in the relation of the arrival rates for sending and receiving direction results also in rising flow times, if the NAC processor speed is fixed. The different flow times in sending and receiving direction result from the chosen schedule of the NAC-phases by giving higher priority to the arriving packets. Due to the limitation of the buffers, the number of accepted frames will be limited and, therefore, the waiting times are bounded, too.

3.3.3 Network Influence

As pointed out in [9], the next step in the analysis of the CAM is to consider the influence of the other stations. This can be done by an extension of the model treated in section 3.3.2. by adding a channel server phase for the transmission of packets, sent by other stations. The interaction of the channel phases is then given by a set of transition probabilities, taking into account the channel states, the traffic matrix, and the protocol dependencies (e.g. access right sequence).

3.4 The Access Protocol

The operation of the network underlies an extended CSMA-CD-protocol with dynamic priorities for the channel access using deterministically staggered transmission delays for each station. The transmission delays can be adapted to meet different requirements:

- fair access for all stations through cyclically changing of the transmission delays
- fixed prioritized access by fixed assignment of the transmission delays
- dynamic prioritized access through an adaptive assignment of transmission delays to single stations or a group of stations according to criteria of unbalanced load or overload.

The CSMA-CD-DP-protocol uses an immediate acknowledgement after each packet-transmission. The transmission delays are adjusted in each station after reception of the broadcasted acknowledgement according to the actual schedule of the transmission delays.

3.4.1 Modelling and Performance Analysis

The performance of the protocol has been investigated by means of simulation and mathematical analysis, allowing the study of allmost all cases of system parameters, process characteristics, and protocol options. Results of this analysis are reported in [8], considering especially the different protocol extensions and unbalanced load situations.
The mathematical analysis is based on the idea of collecting all waiting frames into a virtual queue and establishing a virtual service-time, depending on the mean number of waiting packets. Results can then be calculated for the resulting M/G/1-system. This analysis is reported in [8], too.

The results of the access protocol analysis are used in the end-to-end-transport-delay analysis for deriving the channel access delay and for the calculation of the access protocol overhead.

4. END-TO-END-TRANSPORT DELAY

The end-to-end delay of a message in the considered system, sent from one peripheral device to another, is composed of the following components:

- the flow time through the sending NAC
- the waiting time in the sending CAM
- the channel transmission time including the access protocol overhead
- the waiting time in the receiving CAM
- the flow time through the receiving NAC

The most influencing factors contributing to the end-to-end delay have been identified by the specific submodels:

- the processing and waiting times in the NAC depending on the schedule of the processor phases and the data-buffer dimensioning
- the intermediate buffering within the CAM under bidirectional traffic conditions
- the channel access delay and the protocol overhead.

If the parameters of the submodels are chosen in such a way that the interfaces between the submodels are represented adequately, the results of the submodels can be composed together to calculate the total end-to-end-transport delay.

4.1 Analysis Procedure

The calculation of the end-to-end-transport delay proceeds as follows:

STEP 1

Determination of the virtual channel transmission time for a particular activity at access protocol level. This calculation includes the channel characteristics (transmission speed, packet length distribution), and the network configuration (number of NAS's) and is performed by the protocol analysis.

STEP 2

Consideration of the two involved CAM's with respect to the traffic matrix and the resulting sending and receiving arrival rates at CAM level. The influence of the system is taken into account according to the extended CAM analysis [9] or the extended CAM-model, mentioned in Section 3.3.3. This step yields the resulting waiting times within the sending and receiving CAM, respectively.

STEP 3

Calculation of the flow times through the sending and receiving NAC, according to the model given in section 3.2. This step considers the actual processor schedules, the data-buffer-dimensioning and the arrival rates, found from the source-destination traffic matrix at peripheral level. The probability of internal connections for each NAC is determined by this traffic matrix, too.

CONCLUSION

A local area network with a 3-level structure has been presented. The access stations of this network have been analyzed in detail, separating them into two submodels, the network access controller and the channel access module.

The performance of the network access controller has been studied, considering the schedule of the processor phases, the occurence of cluster-internal connections, and buffer limitations.
The analysis of the CAM has been performed by extending the CAM-model to bidirectional traffic conditions.

These models reflect the main factors contributing to the end-to-end-transport delay in a local area network. As shown by the analysis, the structure of the access stations heavily influences the system performance. Therefore the delays within the NAS's have taken carefully into account. The analysis allows the conclusion that in many cases the system performance of a LAN is primarily given by the maximum channel throughput and the end-to-end-transport delay of data.

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