SELF ROUTING BANYAN NETWORKS IN AN ATM-ENVIRONMENT

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Abstract

For the integrated broadband communication networks of the future the asynchronous transfer mode (ATM) has been proposed as a switching principle. To implement such an ATM network, high speed switching nodes with high capacity are needed. One of the most critical points of these switching nodes is the interconnection network, where the basic switching function is done. A possible choice therefor are the so called "self routing Banyan networks". These interconnection networks need no central control and are thus able to switch many packets in parallel. In this paper a short classification of the Banyan networks is presented together with a discussion of some implementation aspects and operation modes. In the second part, an analytic approach for the performance analysis of a special class of self routing Banyan networks, namely the Delta-b networks with multiple buffers, is introduced and some numerical results are shown.

1 Introduction

In addition to the narrowband services, future communication networks will also provide broadband services like video communication, graphic applications and high speed data communications. The flexibility and capacity required for such a broadband network could be provided by a network based on the asynchronous transfer mode (ATM). An ATM network transfers all information in packetized form and is characterized by high speed links, simplified protocols and high capacity switching nodes.

The use of the ATM technique seems to offer some advantages, since only one network is necessary for integrating all kinds of services with their different bandwidth requirements. Due to the inherent flexibility of this technique, new services can be offered within the network in the future, even if the requirements of these services are unknown today.

To achieve the high throughput in the switching nodes that is necessary for this type of network, the basic switching functions have to be implemented in hardware and it should be possible to switch several packets simultaneously and in parallel. Several types of Banyan Networks, which are already known from multiprocessor computer applications, have been proposed for the implementation of such a high speed switching fabric [5,8,10,14].

In the following sections, a short classification of the Banyan networks will be given and some implementation and operation aspects will be discussed. An analytic approximation for the performance evaluation of the general class of Delta-b networks with multiple buffers will be presented in section 4 together with some results.

2 Banyan Networks

Banyan networks belong to the class of multistage interconnection networks and have been defined by Goke and Lipovsky [4] using graph theoretical methods. In a simplifying approach we shall consider a Banyan network as a multistage interconnection network which has the property that there is exactly one path between any input port and any output port (single path network). The general class of Banyan networks can be structured into several subclasses:

A *L-level Banyan* is a Banyan where only adjacent stages are connected by links. This means that each path leads exactly through L stages. The L-level Banyan class can be subdivided into *Regular* and *Irregular Banyans.* Regular Banyans are constructed from a single type of basic elements with F inputs and S outputs, whereas the type of the elements of an Irregular Banyan is varying throughout the network. The Generalized Delta-networks [2] are an example of Irregular Banyans.

Computer Communication Technologies for the 90's
J. Raviv (Editor), Elsevier Science Publishers B.V. (North-Holland)
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Ninth International Conference
on Computer Communication
Tel Aviv, Israel, 30.10 - 4.11.88

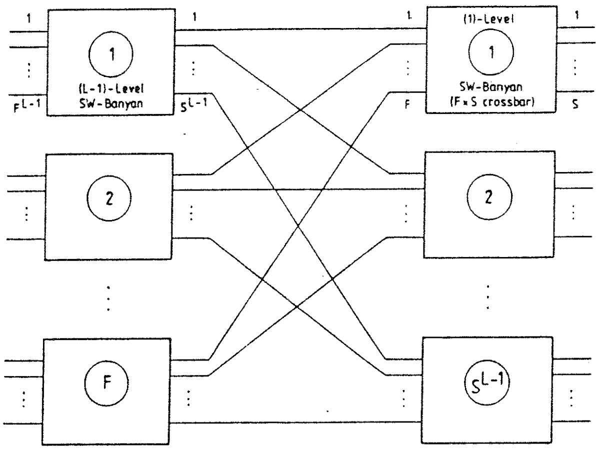

Figure 2: Recursive construction of a (L)-level SW-Banyan

For an economical implementation of switching networks Regular Banyans will be preferred because they are composed of identical elements. Two subclasses of Regular Banyans are the *CC-Banyans* and the *SW-Banyans* . We will restrict our further discussions to the SW-Banyan class, because it includes most of the existing implementations.

A property of the SW-Banyans is, that these structures can be constructed recursively from a crossbar structure with F inputs and S outputs. This basic $(F \times S)$ crossbar element can be considered as a (1)-level SW-Banyan. To get larger SW-Banyan structures with L levels, several $(L-1)$-level SW-Banyans are connected with an extra stage of $(F \times S)$ basic elements as depicted in Figure 2. Each $(L-1)$-level SW-Banyan has F^{L-1} input links and S^{L-1} output links. The additional crossbar switches must be connected to the SW-Banyans in a regular manner, i.e. if a crossbar is connected to output i of SW-Banyan number 1, it must be connected to output i of all other SW-Banyans as well.

Delta networks as defined by Patel [12] have the same topological structure as SW-Banyans. They are constructed of n stages corresponding to the L levels of the SW-Banyan. Analogous to the SW-Banyan, each stage consists of several switching elements with a input ports and b output ports, so the network has a^n input terminals and b^n output terminals.

The definition of Delta networks is including the application of a specific routing scheme called "self routing". Using this scheme, the movement of the packets through a Delta network is controlled by a destination address which must be unique for every output terminal of the network. The destination address is a number of base b with n digits corresponding to the n stages of the network. Each digit directly specifies which output port of a switching element in a specific stage will receive the packet.

This *digit controlled routing* (self routing) mechanism has the advantage that it can be implemented in hardware and that a central control is only needed for the initial setup of a virtual connection. The switching functions are distributed over all switching elements and can be done in parallel.

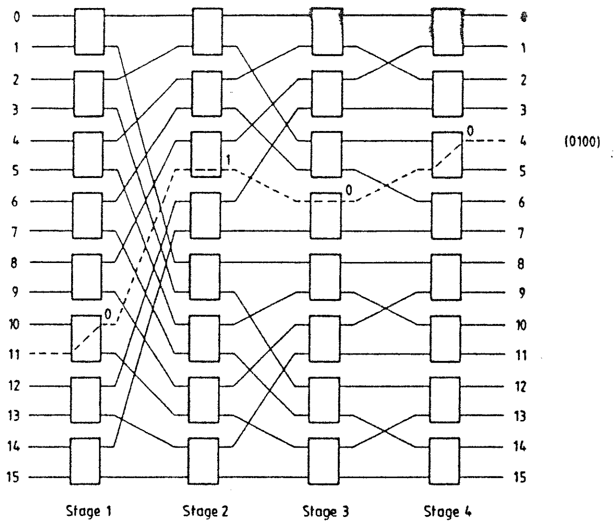

Figure 3: Delta-2 network with 4 stages and 16 inputs

Rectangular Delta networks are constructed from switching elements which have the same number of inputs and outputs $(a = b)$. Consequently, the number of switching elements per stage is constant and the number of network inputs is equal to the number of network outputs. A rectangular Delta network composed of b-input switching elements is called *Delta-b network* .

An example of a Delta-2 network with 4 stages is shown in Figure 3. The dashed line indicates the path of a packet from input terminal 11 to output terminal 4, which has the binary destination address '0100'.

Bidelta networks (Bidirectional Delta networks) have a special topological structure; they remain a Delta network even if the network input links are interpreted as network output links and vice versa. All Bidelta networks are topologically equivalent and can be transformed into each other by relabelling the switching elements and the links [2].

Many of the well known interconnection networks including the Baseline, Reverse Baseline, Omega, Flip, Bit-Reversal and Inverse Bit-Reversal networks belong to the class of Bidelta networks. The network depicted in Figure 3 has the topology of a Baseline network [16].

3 Implementation Aspects

3.1 Operation Modes

There exists a wide variety of choices for the operation of Delta networks, though self routing (digit controlled) operation is implicitly assumed.

The first aspect to be considered here is whether the interconnection network is operated in a *synchronous* or in an *asynchronous* mode. In a synchronous network there is only one clock and the movement of all packets is synchronized to this clock. In an asynchronous network the packets are not synchronized, i.e. they can arrive at any time and the only synchronization is on the bit level. The asynchronous operation requires a handshake protocol between the stages of the network.

Synchronous operation is especially well suited if only fixed length packets have to be switched, whereas the asynchronous operation has advantages for switching packets with variable length.

Another aspect to be considered is the existence and location of buffers. The speed of the transmission links in future ATM networks is expected to approach the technological limits, so that it will be impossible to speed up the interconnection networks enough to obtain an acceptable probability of packet loss without any buffering.

To keep the switching elements of the interconnection network simple, the complete buffering can be done in buffers preceeding the first stage of the network. Each packet is buffered there until the whole path through the network has been found and allocated. Therefore this *unbuffered operation mode* implies an acknowledgement mechanism between the outputs of the network and the input buffer. For structures with many inputs and outputs the blocking probability will be very high in the unbuffered case resulting in a low maximum throughput. On the other hand, the transfer delay at moderate loads will be low since the packets have to pass only one buffer.

In the *buffered mode* every single switching element has its own buffers which are capable of storing at least one complete packet. Using a backpressure mechanism these buffers can be used to delay blocked packets. In this case the transfer delay at moderate loads will be higher because the packets have to pass as many buffers as there are stages. The advantage of the buffered mode is that a higher maximum throughput can be achieved.

A switching element for a buffered network basically consists of a buffer and a switching matrix, where the size and organization of the buffer and its location with respect to the switching matrix (input buffer / output buffer) has considerable influence on the performance of the interconnection network.

An enhancement in the asynchronous, buffered case is the *virtual cut through* mechanism [7,14] where a packet can bypass a buffer if the required output link is available for transmission. This mechanism combines the advantages of the unbuffered network (minimal delay at moderate loads) and of the buffered network (high maximum throughput).

Another enhancement for buffered networks is the *bypass queueing* mode [14]. In this mode the buffer is handled in a modified first-in first-out (FIFO) manner. If the packet at the top of the buffer is blocked, the first packet which is destined for a non-blocked output will be transferred. This means that each input buffer is partitioned into one logical FIFO per output sharing the total buffer capacity in a load dependent manner.

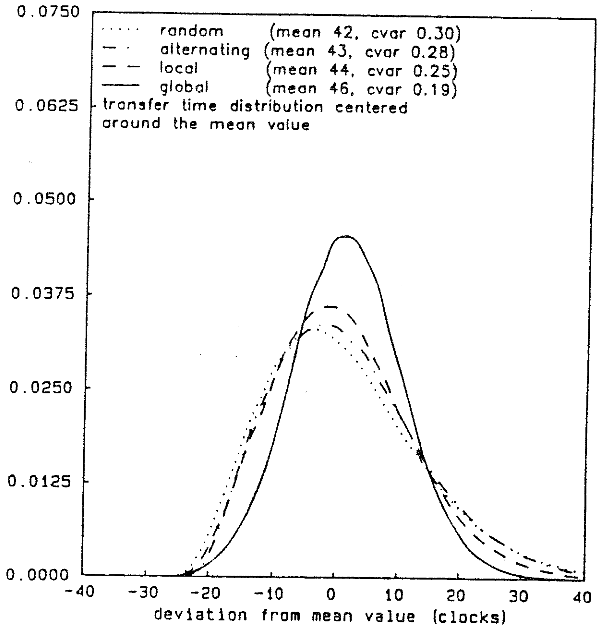

Figure 4: Transfer time distribution of a Delta-2 network with 64 inputs

3.2 Collision resolution strategies

If packets from different inputs want to leave a switching element via the same output in a buffered network, a collision occurs. In the case of such a collision, one packet has to be selected for immediate transfer and all others must be delayed. For the selection of the "winning" packets, several strategies could be applied:

1. **Random:** The input to be served first after the detection of a collision is chosen randomly.
2. **Alternating:** If a collision occurs, the input handicapped by the last collision (the packet of that input was not served immediately) will be served first. This strategy is restricted to switching elements with only two inputs, but analogous extensions to switching elements with more inputs are possible.
3. **Local:** The packet with the highest local waiting time (interval between entering the switching element and the instant of collision) will be served first.
4. **Global:** The packet with the highest global waiting time (interval between entering the interconnection network and the instant of collision) will be served first.

The hardware requirements for the implementation of these strategies are very different. Strategy 1 can be realized using a synchronous or asynchronous clock signal whose state determines the selection of a packet. The *alternating* strategy can be implemented very easily by a Flip-Flop which is toggled each time a collision had occured.

The strategies 3 and 4 lead to an additional overhead, because a time stamp is necessary for every packet. The evaluation of the time stamp is very time critical and must be done as fast as possible. A practical implementation for buffered Delta-2 networks could be a parallel comparator unit which determines the packet to be transmitted.

The collision resolution strategies also have an influence on the delay jitter which results from the statistical switching in the interconnection network. To evaluate this jitter, the coefficient of variation of the transfer time can be used. The variance should be as small as possible to achieve a nearly constant transfer time.

Figure 4 shows the transfer time distribution of a Delta-2 network with 6 stages and buffersize 10 for the strategies described above (simulation results). The mean and the coefficient of variation of the distributions are given in the legend of the diagram. The only strategy which can significantly reduce the jitter is strategy 4 *(global)*, because it delays those packets which have advanced faster than others and prefers those packets which have often been blocked.

Depending on the requirements of the whole communication network an optimal choice among all these alternatives must be made. From an implementation point of view it seems to be practical for an ATM network to have a time-slotted, synchronous operation on the links and therefore also within the switching nodes. This implies more or less a packet format with fixed length for optimal usage of the time slots. For such a scenario a synchronous, buffered Delta network, as analyzed in the next section, would be a feasable choice for an interconnection network.

4 Performance of Delta Networks with Multiple Buffers

4.1 Model of the Network

We consider a Delta network with n stages which is constructed of $b \times b$ switching elements. Each switching element consists of b input buffers with s places and a non-blocking crossbar switch. The model of a Delta-2 network with 2 stages is shown in Figure 5.

Each input of the network is preceeded by a packet processor which does the protocol handling and performs the local routing functions [14]. As the evaluation of the network should be independent of the implementation of the packet processor we restrict our investigations to the analysis of the network without the packet processor. To simplify the analysis we make the following assumptions :

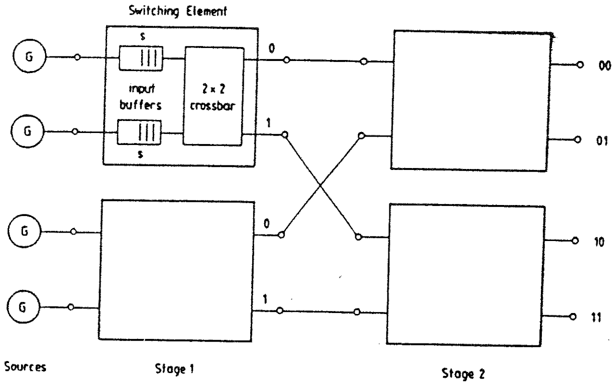

Figure 5: Model of the switching network

1. The network is operated synchronously, that means the packets are transmitted only at the beginning of a time slot given by the packet clock and thus the time axis is considered to be discrete.

2. All packets have a fixed length.

3. Each input link of the network carries the same traffic load.

4. Packets arrive independently at the network input links and the destination addresses are distributed uniformly (at random) over all output links at stage n.

5. The states of the input buffers of a switching element are statistically independent. This is an approximation as the probability for the departure of a packet depends on the states of all other buffers.

6. There is no blocking at the output links of the network. This means that the packet processor at the output is always able to accept a packet.

The load is balanced in the whole switching network as well as in all switching elements. Consequently, the switching elements at a particular stage are statistically indistinguishable and the state of a stage is determined by the state of a switching element. As the buffers of a switching element are assumed to be independent the state of a switching element is represented by the state of any of its buffers.

The analysis of the complete network can be partitioned into the successive analysis of the individual stages. Hereby, the dependencies between the stages are taken into account using the probability that a packet is offered to a buffer at stage k and the probability that a packet is able to leave a buffer at stage k.

The analysis of a switching element as depicted in Figure 5 is done in two steps. First, a relationship between the traffic at the input and the output of the crossbar switch is derived and then the state probabilities of the input buffers are computed.

4.1.1 Analysis of the Crossbar

The analysis of a $b \times b$ crossbar in the clocked operation mode has been presented by Patel [12] and Dias and Jump [1]. Therefore we shall only discuss their results.

At each input link of the crossbar packets are arriving with probability q_{in}. The offered packets are assumed to be independent and their destinations are distributed uniformly over all outputs. Due to the fact that several packets may be destined for the same output link, some packets will be blocked and must remain in their buffers. The transmitted packets are selected randomly (strategy 1).

Consequently, the probability q_{out} that a packet will be forwarded to the next stage is less than q_{in}. The relationship between q_{in} and q_{out} is given by

$$q_{out} = 1 - (1 - \frac{q_{in}}{b})^b \tag{1}$$

Applying eqn. (1) to the crossbar of a switching element we must be aware that we are making an independence assumption here. The arriving packets are not really independent since the blocked packets remain in their buffers. The correlation of the packets in successive clock intervals is increasing with the occurence of blocking. The effects of this simplification will be discussed later on.

4.1.2 Analysis of the Buffer

The state of a buffer is characterized by the number of buffered packets $x, x = 0 \ldots s$. We can model the behaviour of a buffer at stage k as a simple Markov Chain if we assume that packets are arriving independently with probability $q(k)$ and leave the buffer with probability $r(k)$.

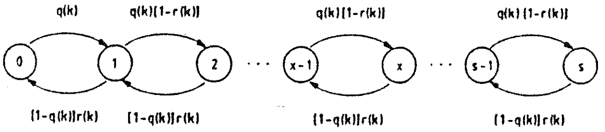

Figure 6: State diagram of the Markov Chain

For the analysis we introduce the following notation :

$X(k)$ random variable for the queue length of a buffer in stage k

$T_f(k)$ random variable for the transfer time of stage k

$p(x,k)$ probability that a buffer at stage k contains x packets

$q(k)$ probability that a packet is offered to a buffer at stage k

$p_a(k)$ probability that a buffer at stage k is ready to accept a packet

$r(k)$ probability that a packet is able to leave a buffer at stage k, given that the buffer is not empty

If the Markov Chain is in the steady state we obtain the following equations :

$$\begin{aligned}
q(k)\, p(0,k) &= [1-q(k)]\, r(k)\, p(1,k) \\
q(k)\, [1-r(k)]\, p(1,k) &= [1-q(k)]\, r(k)\, p(2,k) \\
&\vdots \\
q(k)\, [1-r(k)]\, p(x-1,k) &= [1-q(k)]\, r(k)\, p(x,k) \\
&\vdots \\
q(k)\, [1-r(k)]\, p(s-1,k) &= [1-q(k)]\, r(k)\, p(s,k) \quad (2)
\end{aligned}$$

The state probabilities can be derived from eqn. (2) as

$$p(x,k) = \frac{1}{1-r(k)}\, [Q(k)]^x\, p(0,k) \tag{3}$$

with

$$Q(k) = \frac{q(k)\,[1-r(k)]}{[1-q(k)]\, r(k)} \tag{4}$$

Normalizing eqn. (3) we obtain

$$p(0,k) = \left\{ 1 + \frac{1}{1-r(k)} \sum_{i=1}^{s} [Q(k)]^i \right\}^{-1} \tag{5}$$

Assuming $p(0,k)$ and $r(k)$ to be known, eqn. (5) can be sloved for $Q(k)$ to compute the state probabilities $p(x,k)$ using eqn. (3). The calculation of $Q(k)$ requires the solution of an equation of degree s (s = buffersize). Because for $s > 3$ there is no closed form solution we use a simple numerical algorithm to compute $Q(k)$.

4.2 Analysis of the Network

Considering the synchronous operation we define the normalized throughput ρ as the probability that a packet is transmitted on a link of the network in the current clock cycle. Due to the backpressure mechanism no packets can be lost on the internal links of the network and in the steady state the throughput is constant on any link. A packet is received at an input buffer of stage k if a packet is available and the buffer is ready to accept it :

$$\rho = q(k)\, p_a(k) \tag{6}$$

A packet is transmitted on an output link of stage k if the buffer is not empty and a packet is able to leave the buffer.

$$\rho = [1 - p(0,k)]\, r(k) \tag{7}$$

Assuming that the state probabilities in stage k are known, the probability $p_a(k)$ that a buffer at stage k is ready to accept a packet can be computed as

$$p_a(k) = 1 - p(s,k) + p(s,k)\, r(k) \tag{8}$$

considering that a buffer is able to accept a packet if the buffer is not full or if the buffer is full but one packet is going to leave the buffer during the clock interval. Using eqn. (1) together with eqn. (6) for the switching matrix in stage $k-1$, the probability $p(0,k-1)$ that a buffer in stage $k-1$ is empty can be represented by

$$p(0,k-1) = 1 - b \left\{ 1 - [1 - \frac{\rho}{p_a(k)}]^{\frac{1}{b}} \right\} \tag{9}$$

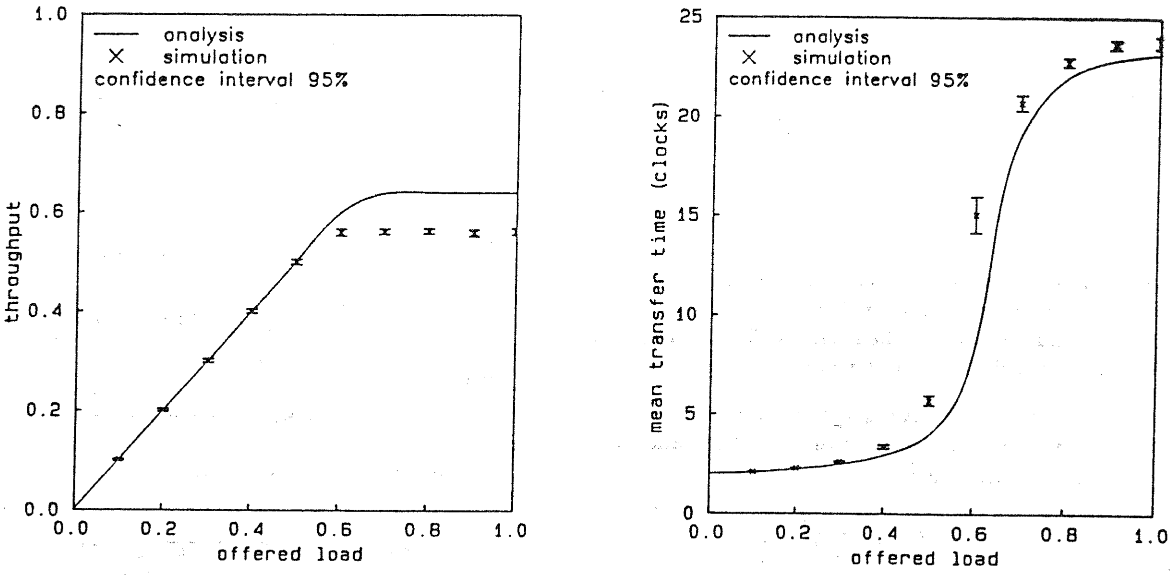

Figure 7: Analysis of a Delta-8 network with 2 stages and buffersize 10

With $p(0, k-1)$ resulting from eqn. (9), the probability $r(k-1)$ that a packet is able to leave a buffer in stage $k-1$ can be calculated from eqn. (7).

$$r(k-1) = \frac{\rho}{1 - p(0, k-1)} \qquad (10)$$

Equations (8), (9) and (10) together with the results of section 4.1.2 allow to compute the state probabilities of stage $k-1$ from the state probabilities in stage k.

With the assumption that the output links of the switching network are always able to accept packets (assumption 6, $p_a(n+1) = 1$) a successive analysis of the complete network, starting at the last stage, can be done without any iterations.

From the state probabilities $p(x, k)$ the mean waiting time of a packet in the buffer can be computed applying Little's law. This waiting time (in clock units) is equal to the transfer time of a packet through the corresponding stage.

$$E[T_f(k)] = \frac{E[X(k)]}{\rho} = \frac{1}{\rho} \sum_{i=1}^{s} i\; p(i, k) \qquad (11)$$

The mean of the total transfer time can be calculated as the sum of the mean transfer times of all stages.

If the given throughput ρ exceeds the maximum possible throughput of the network, the value of $q(k)$ exceeds 1 for those stages which are overloaded. In this case the algorithm is stopped and repeated with a lower throughput.

4.3 Results

In this section we discuss some numerical results of our analysis and compare the performance of several delta networks constructed of 2×2, 4×4 and 8×8 switching elements with varying buffersize.

The analysis of a 64-input Delta-8 network with buffersize 10 is compared with simulation results in Figure 7. The results are very accurate until the network becomes congested and the throughput reaches a saturation. In this case many packets are blocked at the head of the buffers mainly in the first stages of the network and our independence assumption is a rather poor approximation. If the load is increased beyond the saturation point, packets will be lost at the inputs of the switching network or will be buffered in the packet processors depending on the implementation.

Although the analysis is overestimating the maximum possible throughput it is a very simple and useful approximation for comparing the performance of networks constructed of different types of switching elements. It can be used to evaluate the influence of the parameters buffersize and number of inputs per switching element on the network performance and thus to optimize the network structure.

As an example the influence of the buffersize on the performance of the network is shown in Figure 8. It is obvious that the maximum throughput is significantly increasing if the size of the buffers is extended from 1 to 4, but with larger buffers the further improvement is very low. On the other hand, the size of the buffers should be kept as small as possible since at high traffic rates the transfer time of the packets increases linearly with the buffersize. Consequently, a buffersize of 2 or 4 seems to be a reasonable compromise.

Another interesting aspect is the number of inputs and outputs per switching element. Larger switching elements result in a network with fewer stages which has a lower transfer delay. But the performance of a network with large buffers is limited by the maximum throughput of the switching elements in the first stage because the buffers in the succeeding stages are always able to accept a packet.

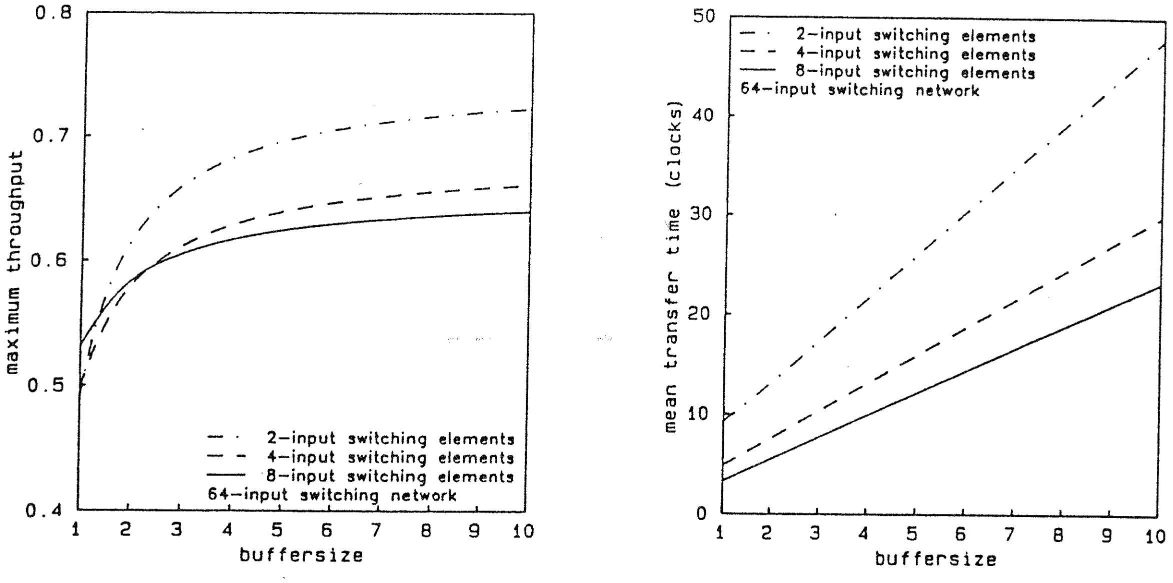

Figure 8: Influence of the buffersize on the performance

In this case Delta-2 networks have the best performance as the maximum throughput of a switching element decreases if the number of its input ports is extended.

As the hardware complexity of the network is dominated by the size of its buffers we shall now compare networks with an equivalent total bufferspace. If we consider a network with 64 input links constructed of single buffered 2 × 2 switching elements, the equivalent network made of 4 × 4 elements (8 × 8 elements) has a buffersize of 2 (3).

With the assumption of an equivalent buffersize the Delta-8 network has the best performance with respect to the throughput as well as the transfer time as shown in Figure 9. However, it should be mentioned here that this result may not be generalized and that for an increased total buffersize the Delta-2 network has the best performance.

For the special case of a Delta-2 network with single buffers an analysis has already been presented by Jenq [6]. In this case our algorithm yields the same results, because the same approximative assumptions have been made in both approaches. However, our approach is completely recursive and there is no need for iterative computations.

5 Conclusion

Banyan networks are a common choice for the implementation of packet switching nodes in ATM-networks. Therefore, we have presented a classification of these networks and discussed different operating modes as well as several collision resolution strategies for the buffered case. For the general class of Delta-b networks with multiple buffers an approximate performance analysis has been developed and the obtained results have been validated by means of simulations. The results for the Delta-2 network with single buffers were compared with those results of the analysis presented by Jenq [6].

The aspects currently under study include some refinements for the analysis described above to get better approximations for heavy loads and some analytic investigations concerning strategies to locate and organize the buffers in the switching elements in a way, that the performance of the interconnection network is optimized.

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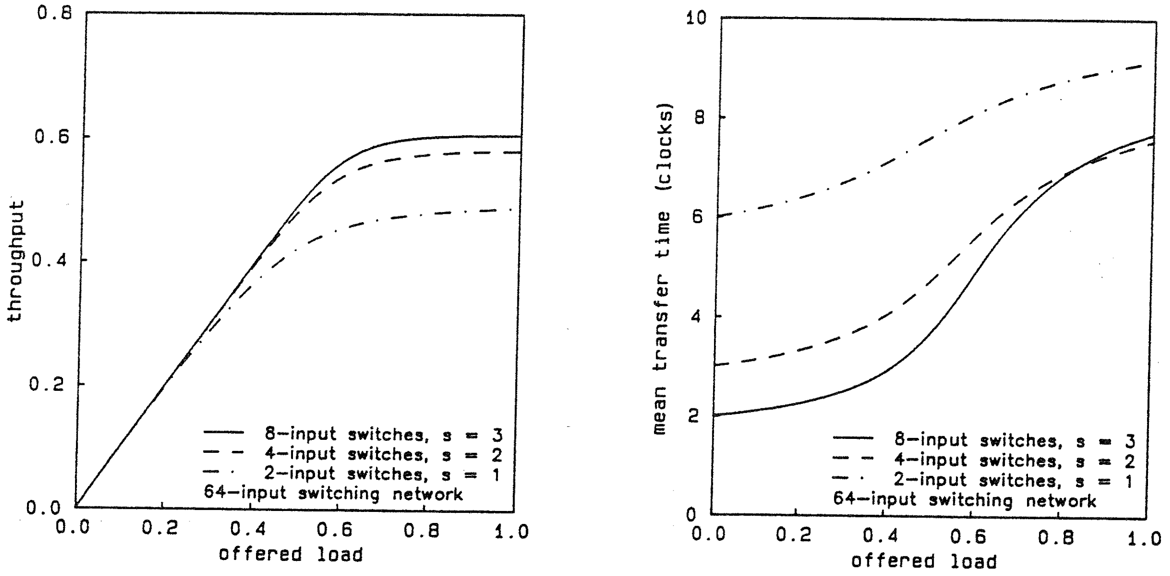

Figure 9: Comparison of networks with equivalent total buffer space

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