An Experimental On-board Multiservice Switch

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1 Introduction

The Internet, especially the World Wide Web (WWW), is currently considered as a particular promising application for the future Ka-Band systems and consequently most of the planned systems shall support Internet applications. However, it is far from clear how the application scenario will develop in future. But for certain there is an increasing requirement to incorporate Quality of Service (QoS) features into the Internet in order to support also applications with stringent timing requirements, e.g. video. Furthermore it can be expected, that the volume of traffic, based on MPEG/DVB technology, will grow.
In most of the projected Ka-Band systems an on-board fast packet switch will be used. Flexible support of the various services with their different QoS requirements is therefore a key requirement for this switch. The Asynchronous Transfer Mode (ATM) is a particular interesting technology since it supports QoS and allows a flexible adaptation to the varying requirements. ATM technology therefore provides an excellent basis for an On-board Multiservice Switch.

Due to fibers, in terrestrial ATM systems the transmission system, i.e. the Physical Layer, in general offers plenty of transmission capacity. This facilitates guaranteeing the required QoS. However, in satellite systems transmission capacity is a more scarce resource. In particular the downlink (D/L) is rather limited and has therefore to be used efficiently. In satellite-based ATM networks an efficient resource management, which implies a neat interworking between the ATM layer and the Physical Layer, is therefore especially important. An On-board ATM switch has to support the resource management.

In chapter 2 we present an experimental On-board Multiservice Switch which supports ATM and allows for a flexible resource allocation in the uplink (U/L) as well as in the D/L. This switch has been developed by Bosch Telecom under a contract of ESA in the framework of the project ESA Experimental Multimedia Switch. The switch is intended to be used with ESA demodulators and is therefore tailored to the requirements of the air interface specified by ESA. This air interface uses Multifrequency Time Division Multiple Access (MF-TDMA) or Time Division Multiplexing (TDM) in the U/L and Time Division Multiplexing (TDM) in the D/L. The switch architecture, however, could be easily adapted to other MF-TDMA/TDM access schemes.

For an efficient operation of the on-board ATM switch, a fexible resource management is particularly important. A central question concerns the number of admissible Virtual Circuits (VC) of a given service category, which, within the physical resources assigned to this special service category, can be established, such that the QoS of this service category is guaranteed. Thus, if a connection is requested, the resource management has to decide, whether the connection can be established without deteriorating the QoS. To get an estimate about the capacity of the switch in terms of connections as a function of the assigned physical resources, extensive simulations were performed. Since WWW is currently the most interesting application, we focused on the communication of the Web server of an Internet Service Provider (ISP) with the Web clients of the customers. A simple WWW application scenario was defined and in particular the stream of replies from the ISP to the customers via the satellite was considered. We determined how many connections from the ISP to the customers via the satellite can be established within the U/L transmission capacity of the ISP´s Satellite Ground Terminal (SGT). Also the impact of the allocated bandwidth in the D/L on the Cell Loss Ratio (CLR) and the Cell Transfer Delay (CTD) has been investigated. The results of these simulations will be presented in chapter 3.

Finally conclusions will be presented in chapter 4.

2 Architecture and Realization of the Multiservice Switch

As mentioned above the switch is intended for use with the ESA demodulators. ESA demodulators, however, are based on the system concept of ESA OBP [1] and are originally specified for use with the ESA OBP circuit switch, but not for use with an ATM switch.
Thus we first devised a simple scheme for the transport of ATM cells within the Frame Units (FU) of the U/L frame resp. D/L frame, assuming that 14 contiguous FUs in a frame are used to carry 1 ATM cell. The ATM cells are mapped into the Frame Units (FU) of the U/L frame by the SGT resp. to the FUs of the D/L frame by the On-Board Switch.

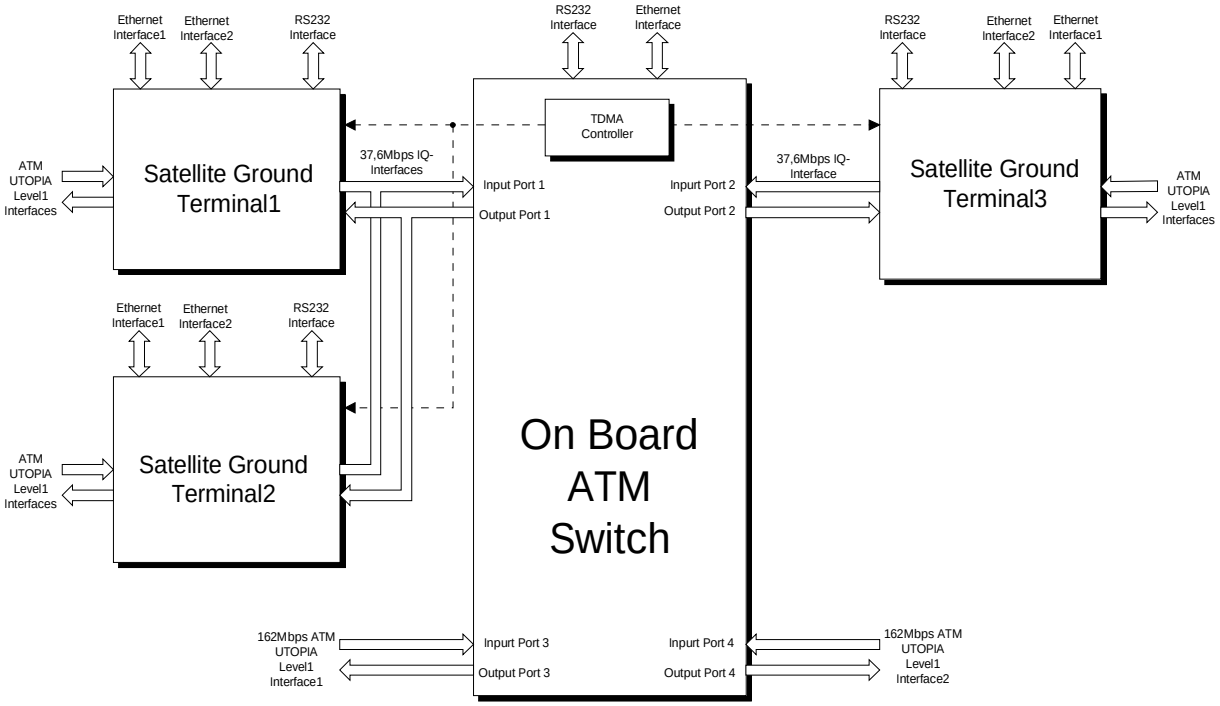

Figure 1 System Overview

In case of Multi Carrier Demodulators (MCD) the FUs of up to 64 U/L frames are multiplexed by the on-board demodulator, such that every 0.871 msec one output frame, consisting of 1024 FUs, is generated by the MCD. Since each FU carries 32 bits an ESA demodulator transmits a 37.617 Mbps bit stream over a 2-bit parallel interface to the On-Board Switch. However due to the multiplexing of FUs of different U/L frames, in general the FUs carrying an ATM cell will not be contiguous in the output frame.

2.1 Architecture

Figure 1 shows a block diagramm of the Experimental On-Board ATM Switch and the corresponding test environment. The On-Board ATM switch features 4 input resp. output ports and provides a throughput of 800 Mbps. Two of the input resp. output ports support the 2-bit parallel interface and can therefore be used to connect the switch to demodulators resp. modulators or to the SGT simulators of the test environment. The remaining 2 input resp. output ports support the Level 1 Universal Test And Operational Interfaces for ATM (UTOPIA) and can be used to put an additional background load on the switch, i.e. to simulate the traffic of additional ground terminals. The On-Board ATM Switch supports different ATM service categories like for example Constant Bit Rate (CBR), non-real time Variable Bit Rate (nrt-VBR) and Unspecified Bit Rate (UBR) traffic and can handle point-to-point connections as well as point-to-multipoint connections. The separation of connections belonging to different service categories is achieved by a complex cell buffer management within the switch, which will be described below.

A SGT simulator features one 2-bit parallel baseband interface for sending resp. receiving frames. At this interface the SGT simulator is connected to the switch. A SGT simulator generates a frame of 1024 FUs according to the format of the output frame of an ESA MCD. It is also possible that several SGTs are used to generate a frame. In addition each SGT Simulator has standard interfaces like Ethernet and RS232, as well as a cell interface according to UTOPIA Level 1 standard. Thus by a software upgrade the SGT simulator could be enhanced to act as a simple IP router.

The test environment comprises three Satellite Ground Terminal (SGT) Simulators. As shown in figure 1, SGT1 and SGT2 could share e.g. input port 1 and output port 1, while SGT3 uses input port 2 and output port 2. In this scenario SGT Simulator 3 could represent the large SGT connected to the WWW server of an ISP, while SGT Simulators 1 and 2 could be considered as small SGTs, connected to the WWW clients of the customers. This scenario is the basis of the simulations, which are described in chapter 3.
To synchronise the SGT simulators and the switch, the On-Board ATM Switch comprises a TDMA controller, which provides all necessary clock signals (e.g. start of frame).

2.2 Hardware Realization

Only one type of hardware platform has been developed for the On-Board ATM Switch and for the SGT Simulators. This hardware is of modular design to meet the functional requirements of both the ATM Switch and the SGT simulators. The common hardware platform consists of a Resource Controller Assembly and a Cell Processor Assembly.

2.2.1 Resource Controller Assembly

The main task of the Resource Controller Assembly is to configure and control the devices of the Cell Processor Assembly. An off-the-shelf microprocessor board, developed within another project at Bosch Telecom, is used as Resource Controller Assembly. This board features an

UTOPIA interface and can therefore be connected to an UTOPIA level 2 bus, where it acts as a physical device.

2.2.2 Cell Processor Assembly

Figure 2 shows a block diagramm of the Cell Processor Assembly. The main functional units of the Cell Processor Assembly are:

- IQ – Receive Cell Processor
- Hybrid ATM Bus Access Controller (HABAC)
- Waveform Adaptation Units (WAU)
- Bypass Unit

The **IQ-Receive Cell Processor** implements the receive functions of the Physical Layer. It accepts a frame from the demodulator every 0.871 msec. Frames are stored in a ping-pong buffer. While an incoming frame is written to one of the buffers, the FUs of the preceeding frame are read form the other buffer under the control of a driving memory. The ATM cells are reassembled from the FUs and header error detection/correction is performed. Idle cells are discarded, valid cells are forwarded to the HABAC via the UTOPIA level 2 interface. In communication with the HABAC the Cell Processor acts as a physical layer device. The Cell Processor is able to insert a receive timestamp in dedicated test cells. The functions of the IQ-Receive Cell Processor are implemented in a XILINX 4020 FPGA. Total equivalent gate count is about 11500.

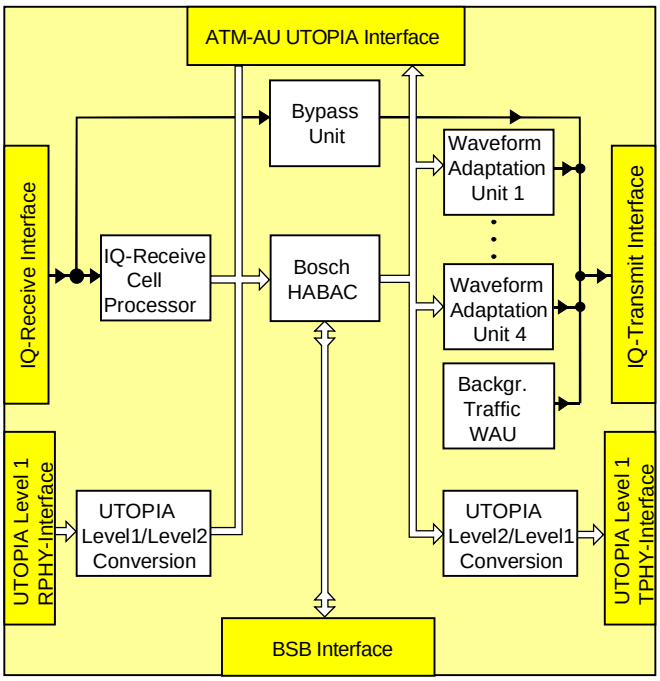

Figure 2: Cell Processor Assembly

The **HABAC** is an ATM chip developed by Bosch Telecom. It is used to build ATM switches with a shared bus architecture. The HABAC implements all functions of the ATM layer. A cell received from the IQ-Receive Cell Processor will be forwarded to the Broadband Switch Bus (BSB). Cells read from the BSB will be passed to the Waveform Adaptation Units via the UTOPIA level 2 interface. The main features of the HABAC are:

- internal cell buffer up to 26 cells for cells received at the UTOPIA interface
- additional external RAMs for buffering of ABR and UBR traffic (up to 2k cells) are possible
- internal cell buffer up to 100 cells, supporting 3 service category specific queues with dynamic buffer size, for cells received from the BSB
- UTOPIA level 2 interface with throughput up to 200 Mbps bi-directional
- redundant 16 or 32 bit wide folded BSB
- BSB send and receive access rate up to 800 Mbps.
- supports 32 bit address range (16 bit VPI, 12 bit VCI, 4 bit port number) without restrictions
- path (=VPI only) or connection (=VPI+VCI) remapping
- support of multicast
- port-related translation, i.e. in case of multi-cast connections, different header values can be defined for each destination port

The HABAC is currently implemented with a commercial 0.5 µm CMOS process. However, during the design of the HABAC care has been taken to facilitate the implementation of the HABAC on other (e.g. rad-tolerant) CMOS processes. We expect that space qualified ATM switches with througput of up to 1 Gbps can be built with radiation hard HABACs.

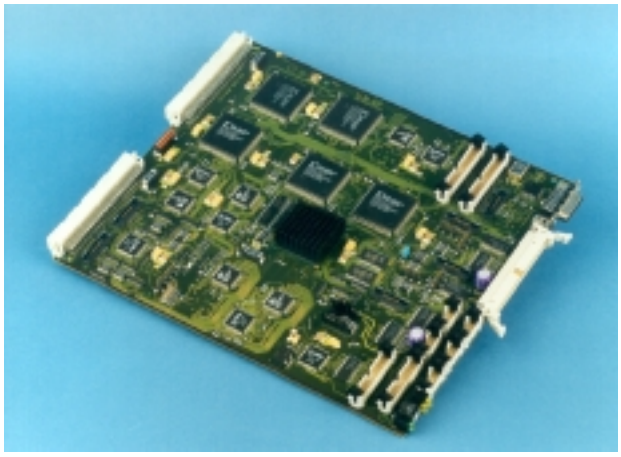

Figure 3: Cell Processor Assembly (Printed Circuit Board)

The **Waveform Adaptation Units (WAU)** implement the transmit functions of the Physical Layer. Each of the 4 WAUs acts as a physical layer device and can be adressed individually on the UTOPIA level 2 bus. A WAU receives an ATM cell from the HABAC via its UTOPIA interface and stores the cell in a buffer, where it waits for transmission. This buffer has a capacity of 64 cells. A WAU performs parallel to serial conversion and maps the cells to the frame units of the D/L frame. Each WAU can be assigned a dedicated bandwidth by assigning specific FUs in the frame to this WAU. Thus ATM service categories can be separated by assigning the service categories to different WAUs. For example one WAU could be used for CBR, one for rt-VBR traffic, one for nrt-VBR and one for UBR-traffic. The assignment of FUs to the individual WAUs can be modified on a frame by frame basis. This allows for a very flexible adjustment of the assigned transmission capacity per service category by a resource manager. The resource manager could e.g. monitor the cell buffers and assign FUs depending on service category and number of cells waiting

in the buffer. A WAU is able to insert a transmit timestamp in dedicated test cells.
There is one special WAU, called Background Traffic WAU, which can be used by the Resource Control Assembly to write data to specific FUs (e.g. timing information or a burst frequency time plan for the SGTs) .
The functions of a WAU are implemented in a XILINX 4013 FPGA. Total equivalent gate count is about 7100.
We implemented only 4 WAUs, although the HABAC could independently address up to 16 WAUs. Thus the support of more service categories per D/L would be possible. It would also be feasible to generate in parallel several D/L frames (up to 16) with one Cell Processor Assembly.

The MCD generates synchronization information for the SGT, which is mapped into specific FUs of the frame, generated by the MCD. These data cannot be routed by the HABAC. The task of the **Bypass Unit** is to map the contents of these FUs to the corresponding FUs in the D/L frame.

Figure 3 shows the printed circuit board which has been developed for the Cell Processor Assembly.

2.2.3 Realization of the On-Board ATM Switch

For the On-Board ATM Switch 2 Cell Processor Assemblies and 2 Resource Controller Assemblies are required. The Cell Processor Assemblies are interconnected by the BSB. ATM cells received by an HABAC are forwarded to the BSB. Each HABAC connected to the BSB reads the cells from the BSB. Depending on the routing information stored in the HABAC, the cells will be routed to the WAUs via the UTOPIA interface or will be discarded.

2.2.4 Realization of the SGT Simulator

One Cell Processor Assembly is used in an SGT Simulator. An ATM cell generator can be connected to the UTOPIA level 1 RPHY interface of the Cell Processor Assembly. The generated cell stream is multiplexed through the UTOPIA Level 2 MPHY Interface with management or user traffic cells from the Resource Controller Assembly. The cells are routed to the 4 Waveform Adaptation Units (WAUs) by the HABAC and mapped to the corresponding FUs. Additional traffic could be generated by the Resource Controller in conjunction with the Background Traffic WAU. So it would be possible to have a task running on the Resource Controller Assembly which models complex traffic sources.
A downlink frame received at the IQ-Receive Interface is processed by the IQ-Receive Cell Processor. The cells are reassembled, evaluted and passed to the HABAC, which routes the cells to their destination ports. These ports could be the Resource Controller or a cell analyzer, connected to the UTOPIA Level 1 TPHY Interface.

3 Simulations

As mentioned in the introduction the questions addressed here concern the number of VCs of a service category with given QoS requirements, which can be simultaneously handled by the satellite system within the resources assigned to this service category. Also dependence of the CLR and the transfer time on the size of the on-board buffers and on the allocated bandwidth in the D/L is investigated.

3.1 System Model

The simulation model shown in figure 4 represents the satellite system. A set of N sources send traffic to the ISP site where it awaits transmission in the U/L, that is denoted as a server with a constant service rate R_u. On-board, the arriving cells are splitted in two virtual output queues[1] where they await transmission in the D/L, which is also modelled as a constant server. In this model, the number N of sources, the branching probability p, the size S_d of the on-board buffers and the allocated downlink rate R_d are parameters that are varied during the simulation study. With the depicted time meter, the transfer time distribution that is discussed in Chapter 3.3.4 is measured.

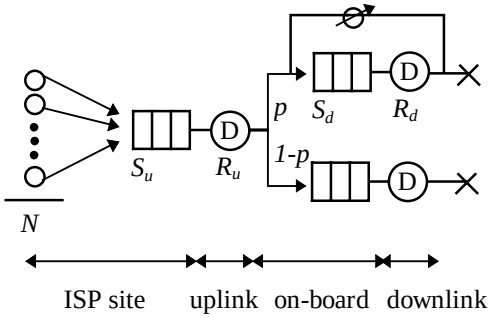

Figure 4: Simulation model of the satellite system

3.2 Traffic Model

Since WWW traffic is very asymmetric with short requests from the users to the ISP and long replies from the ISP to the users, the forward link from the ISP to the user terminal via the on-board switch is analysed particularly.

	type 1	type 2
average rate	17.6 Kbps	128 Kbps
maximum rate	2.048 Mbps	2.048 Mbps
burstiness	116	16
mean burst size	625 ATM cells	63 ATM cells

Table 1: Source characteristics

Table 1 summarises the characteristic parameters of two ON/OFF source types taken from two published Internet traffic measurements [2],[3]. Both source types send a

[1] The limitation on 2 virtual output queues is done to show the effects of bandwidth allocation in the presented satellite system.

shifted geometrically distributed number of constantly spaced ATM cells in the ON phase followed by a negative exponentially distributed OFF phase[2].

3.3 Performance Evaluation

The simulations to dimension the on-board buffers and allocated D/L capacity are carried out with a homogeneous traffic scenario, where only sources of one source type are involved. In order to offer a load of 0.8 in the U/L, either 1709 type 1 sources or 235 type 2 sources have to be enabled. To be able to easily compare the simulation results, the ratio *r* between the maximum service rate of an on-board buffer and the averagely maximum offered rate to this on-board buffer is introduced.

$$r = \frac{R_d}{p \cdot R_u}$$

3.3.1 CLR of the On-ground Buffer

As the dimensioning of the on-ground buffer has a strong impact on the characteristics of the traffic arriving on-board, the CLR of the on-ground buffer is analysed first. With a simple approximation that can be found in [4], the CLR ε of N independent and identically distributed (iid) ON/OFF sources can be calculated as follows:

$$\varepsilon = \beta \cdot \exp\left| -\frac{N(c - N\rho h)X}{b(1-\rho)(Nh - c)c} \right|$$

where β is the CLR in the bufferless case[3], c the service rate (37.6 Mbps), X the buffer size and ρ, h and b the workload, the peak rate and the mean burst duration of one ON/OFF source.

From the above formula it can be observed that a large on-ground buffer is needed to reach a workload of 0.8 with a reasonable CLR. This is certainly only applicable for non-real time traffic to fill the system with background traffic. Real-time applications have to be isolated in small buffers and a scheduler has to provide fair service of these different queues [5]. As the focus of this study is on non-real time applications to load the system, the on-ground buffer size is chosen to 10000 ATM cells for all further simulations.

3.3.2 CLR of the On-Board Buffers

Figure 5 shows the CLR of an on-board buffer depicted over its buffer size. The parameter of the curves is the ratio *r*, whereas for each value of *r* the splitting probability *p* and the allocated D/L rate are varied in that way that *r* remains constant. It can be observed that the curves with different branching probabilities and D/L rates, but equal *r* have a similar behaviour. This leads to the first conclusion that the CLR of the on-board buffer can be roughly dimensioned with this ratio *r*.

The second interesting observation that can be made from figure 5 is the constant progression of the curves with the ratio r smaller than 1. Even if additional buffer space is provided, the CLR does not decrease any more. This phenomenon can be explained with long-term overload situations when the filled on-ground buffer at the ISP site sends ATM cells with the maximum rate of the U/L.

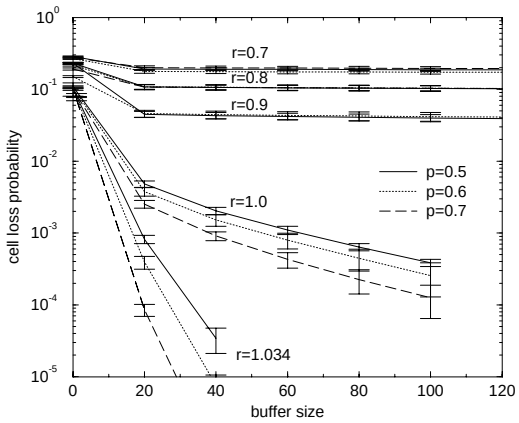

Figure 5: CLR of type 1 sources

Due to the large on-ground buffer size (that is necessary to accept many flows), these bursts can comprise several thousand ATM cells. Because of the allocated D/L rate that is too small, these bursts cannot be served fast enough and because of the small on-board buffers, only a vanishing part of the arriving cells can be stored. In fact, even an on-board buffer comprising several thousand ATM cells – which is not realistic due to its size and weight – a CLR in reasonable regions could not be measured.

If *r* is chosen to 1, or even just above, overload situations can only be caused by load fluctuations between virtual output queues. These are short-term overload situations that can be handled by the small on-board buffers.

3.3.3 Comparison of Different Source Types

The so far stated conclusions are based on simulations which are all carried out with a homogeneous traffic scenario of type 1 sources. To prove that the presented results are not dependent on that source type, simulations with sources of a different publication of Internet traffic measurement were carried out. These sources of type 2 have the same maximum sending rate but a much smaller burstiness and thus are expected to produce a smaller CLR.

The simulation results in figure 6 prove the expected result that the sources of type 2 produce a somewhat smaller CLR but behave principally similar to the sources of type 1. The dependence of the on-board CLR on the source model is however only weak due to the effects of the ground buffer. This observation together with the results from chapter 3.3.1 show that the on-ground buffer has to be dimensioned according to the traffic characteristics of the applications while the CLR of the on-board buffers is only dependent on the parameter r.

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[2] In [2] and [3] mean values of the burst size and silence time are published which we mapped on the ON/OFF model with markovian distributed phases.

[3] The CLR in the bufferless case can be easily computed with a binomial distribution.

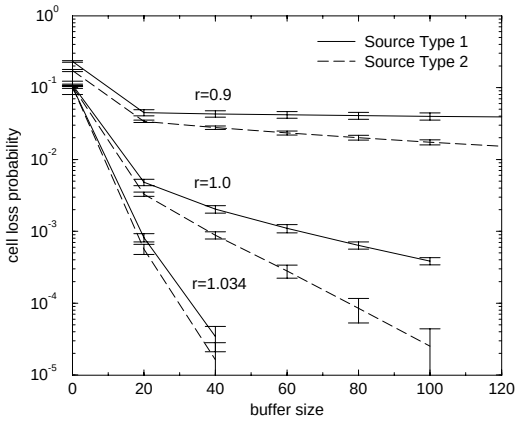

Figure 6:Comparison of the CLR of two source types with different traffic characteristics

3.3.4 Transfer Time Distribution

A closer look at the distribution of the transfer time further supports the conclusions of the previous chapters, that long-term overload situations occur if *r* is chosen smaller than 1, and that short-term overload situations occur for values of r greater than 1. Figure 7 shows the measured transfer time complementary cumulative distribution function (ccdf) of an on-board buffer of the size of 100 ATM cells that is – comparable to the simulations carried out in chapter 3.3.2 – fed with 1709 type 1 sources.

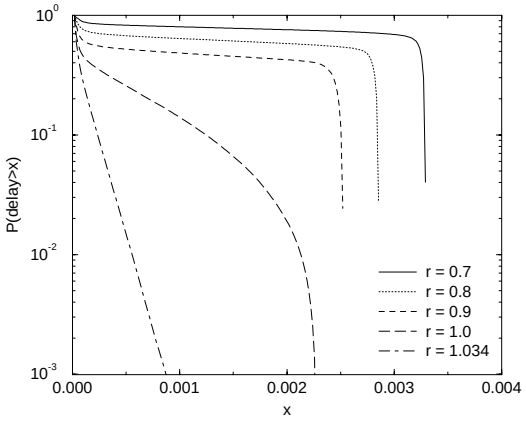

Figure 7: Transfer time ccdf of type 1 traffic

Figure 7 confirms the earlier stated conclusions of a long-term overload situation in the on-board buffer. If an ATM cell reaches an on-board buffer and has to wait, there is a significant probability that the buffer is filled and the cell has to wait almost the maximum possible waiting time until a slot in the downlink is available.

On the other hand it can be seen that if *r* is chosen equal to 1 or even larger, the distribution functions decrease rapidly and thus indicate that these short term overload situations can be handled by the on-board buffers.

4 Conclusions

For a simple scenario we have estimated the capacity of a satellite system with regard to the number of non-real time connections, that can be accepted with a given QoS. We have shown, that due to the bursty nature of the WWW replies a large number of connections has to be multiplexed in order to achieve a load of 0.8 in the U/L. At this load a tolerable on-ground CLR can be achieved only by providing a very large on-ground buffer. Due to the large on-ground buffer very long bursts of some thousand cells will occasionally hit the on-board buffers. But the on-board buffers are comparatively small and can only buffer short-term overload situations. Nevertheless the simulations show, that, in spite of the small on-board buffers, a tolerable on-board CLR can be achieved by a allocating a sufficient D/L transmission capacity per buffer. Thus by a suitable traffic engineering the shortcomings of the on-board hardware can be overcome.

The experimental On-Board Multiservice Switch presented in chapter 2 supports a flexible assignment of U/L and D/L transmission capacity to the various ATM service categories. It can be used to demonstrate and test different resource management algorithms, e.g. CF-DAMA, in a real-time environment. The architecture of this experimental switch provides the basis for the development of a space qualified switch. The HABAC ASIC used in the switch has been designed by Bosch Telecom for terrestrial applications but can be modified for space applications. A rad-tolerant version of the HABAC could be realized with currently available 0.5 or 0.35 µm rad-tolerant CMOS processes. Due to this development Bosch Telecom is prepared to realize a space qualified, medium-sized on-board ATM switch within a short time frame.

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