

A SIMULATION STUDY OF CCITT X.25: THROUGHPUT CLASSES AND WINDOW FLOW CONTROL

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ABSTRACT

This paper deals with a simulation study of the CCITT interface X.25. The simulation is based on a detailed model of X.25, which takes the three levels of the interface and their individual procedures as recommended by the CCITT into consideration. As pointed out in the recommendation there exist some so-called optional user facilities, such as flow control parameter negotiation, throughput class negotiation, and nonstandard packet size. Therefore, a relationship exists between throughput class and several other parameters, as number of handled virtual circuits, window size, packet size, etc.

A description of the model and some simplifying assumptions are explained and form the basis of a simulation program. The derived results allow a fast and accurate determination of the performance of X.25 enabling a quantitative judgement of those relationships.

1. INTRODUCTION

The CCITT Recommendation X.25 defines the "interface between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) for terminals operating in the packet mode on public data networks". X.25 is thus a local interface between an intelligent terminal or a computer and the network. This paper addresses the determination of the performance of X.25. The approach is based on an event-by-event simulation in which the procedures, as recommended by X.25, are implemented. With the help of this simulation program accurate performance results can be obtained as maximum throughput, and mean transfer time.

2. CCITT RECOMMENDATION X.25

In this chapter a brief review of the main features of CCITT X.25 will be given. For further details the reader is referred to the X.25 documents /1,2/ as well as to /3/.

2.1 Structure of CCITT X.25

The CCITT X.25 interface is structured in such a manner that three distinct and independent levels are defined (see Fig.1).

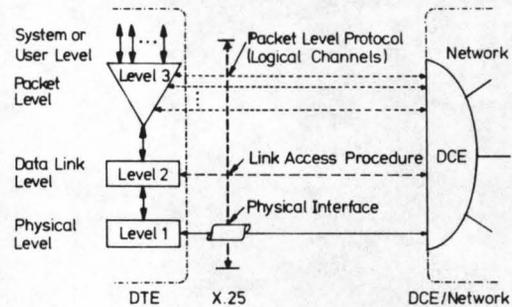


Fig.1: Structure of the X.25 interface

The procedures of one level use the functions offered by the next lower level, but they are independent of the way in which this neighbour level is actually implemented. Hence, the levels could be replaced by completely different ones which provide the same overall functions. X.25 specifies rules, the so-called protocols how information between correspondent levels in the DTE as well as in the DCE have to be exchanged.

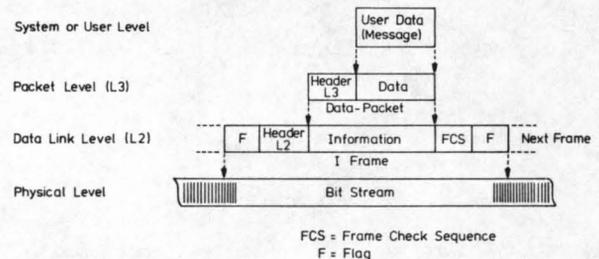


Fig.2: Transfer of information through the levels

Fig.2 shows the transfer of information through the levels in that each level accepts the information from the higher level and adds a header (e.g. header L3, header L2) and a trailer (i.e. FCS) before passing the completed information to the next lower level.

The main tasks of the three levels are:

- level 1: - physical level - this level specifies electrical and physical characteristics of the interface. It provides a bit-serial, synchronous, full-duplex, point-to-point circuit for digital transmission.
- level 2: - link level - it specifies a data link control procedure, the so-called link access

procedure (LAP) for converting the error-prone physical link into a relatively error-free one. It includes methods for avoiding link-congestion during the information exchange between the DTE and the DCE. This LAP corresponds to the Balanced Class of HDLC procedures.

- level 3: - packet level - this is the highest level of X.25. It defines the rules how the user-data is to be encapsulated into packets. It also performs a concentrator function in that it multiplexes a number of so-called logical channels onto the physical link by interleaving packets from various logical channels. Level 3 provides facilities for establishing so-called virtual circuits (VC) which are the bidirectional associations or liaisons between a pair of DTEs over which packets are exchanged end-to-end. Furthermore, each logical channel established at the interface has its own and independent control exerted on the flow of packets.

2.2 Window Flow Control Mechanism

The use of sequence numbers at level 2 is primarily for the error control, whereas the use of sequence numbers at level 3, the so-called packet send sequence number P(S) and the packet receive sequence number P(R) is to control the flow of packets. This is achieved by limiting the number of packets accepted by the network. Therefore, an independent window flow control mechanism is used for each established virtual circuit and for each direction to prevent VC-congestion. In this context the window size w is defined as the number of unacknowledged packets that a DTE or DCE can have outstanding at any time for a particular virtual circuit. The value of w can range between 1 and 7 (or 1 and 127 if extended numbering, Modulo = 128 is used).

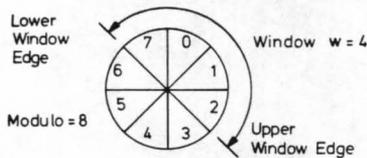


Fig.3: Window flow control mechanism

The mechanism of the flow control, illustrated in Fig.3, is as follows: the value of the so-called lower window edge (LWE) is that one of the last received P(R), here e.g. last received P(R)=7, whereas the value of the upper window edge (UWE) is given by: $UWE = (LWE + w - 1) \text{mod} 8$, here: $UWE = (7 + 4 - 1) \text{mod} 8 = 2$, with: $w=4$ and $\text{Modulo}=8$. Hence, the allowed range of P(S) which could be used for packets to be transmitted is bounded by $LWE \leq P(S) \leq UWE$.

If the P(S) of the last transmitted packet has already reached the upper window edge a so-called "window stop" occurs, in that the flow of packets stops due to the lack of free values for P(S). The flow of data continues only when a newly received P(R) acknowledges an outstanding packet.

2.3 Optional User Facilities

CCITT X.25 distinguishes between several user facilities that may be implemented in a packet-switched network as for example:

- nonstandard default window size w; this facility provides for the selection of default window sizes from the list of sizes supported by the administration. In the absence of this facility the default window sizes are 2.
- nonstandard default packet size; it provides for the selection of default packet sizes from the list of sizes supported by the administration. In absence of this facility the default packet sizes are 128 bytes.
- default throughput class assignment; this facility provides for the selection of default throughput classes. It should be notified that the default throughput classes are the maximum throughput classes which may be associated with any VC at the interface.
- throughput class negotiation; this facility permits negotiation of the throughput classes on a per call basis. This means that a particular throughput class for a VC can be requested if both DTEs, the calling as well as the called one, have been subscribed to this facility. If particular throughput classes are not requested the default values will be assumed.

3. MODELLING AND SIMULATION

Accurate values of performance for the X.25 interface will be obtained by the aid of extensive simulation studies. Base for the simulation is a detailed queuing model (see Fig.4) which takes the three levels and their individual procedures in the DTE and in the DCE into account.

3.1 Description of the Queuing Model of X.25

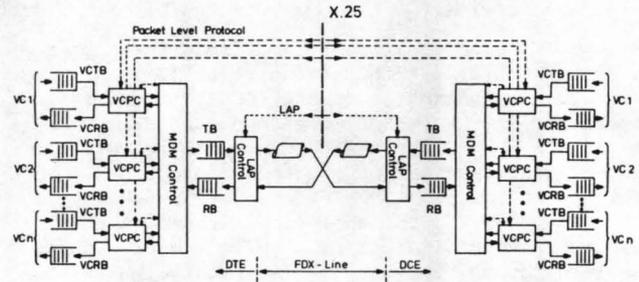


Fig.4: Detailed queuing model of X.25

Fig.4 shows the structure of the queuing model. It consists of two stations, the DTE and the DCE, connected by a full-duplex circuit. This FDX-line represents the physical level, characterized by the transmission rate and the one-way propagation delay. The link level in the DTE as well as in the DCE consists of a link access procedure control (LAP-control) and two queues, the transmit and receive buffers (TB, RB). As mentioned above, the LAP-control handles the error-recovery and takes care of avoiding link-congestion during the information exchange with the other equipment. Packets to be transmitted across the interface are offered by level 3. These packets are stored in the transmit

buffer where they have to wait for further transmission. The transmission is according to first-come, first-served, one packet per information frame. Before transmission finally occurs the LAP-control adds the necessary overhead bits and passes this complete I-frame to level 1 for coding, signal adaptation, and for the definite transmission in case of a free channel. On the other hand, received I-frames which have been successfully transmitted from the other equipment will be treated as follows: the included packet is taken out of the information field and stored in the receive buffer to wait for further treatment by level 3.

Last not least the model consists of several queues, controllers and multiplexers which represent the components of level 3. These modules handle up to n virtual circuits (VC). The implementation takes into account that each of the n virtual circuits will have an individual flow control. Consequently, each VC has its own VC-procedure control (VCPC). Main tasks of each of the VC-procedure controllers are:

- packetizing of messages which are waiting in the VC transmit buffer (VCTB), sequencing of the packets by the packet send sequence number $P(S)$ and offering them to the multiplex-demultiplex control (MDM-control)
- receiving of packets from the MDM-control, de-packetizing and storing the messages into the VC receive buffer (VCRB)
- controlling of the flow of information for the appropriate VC by $P(S)$ and $P(R)$ numbers according to the window flow control mechanism.

The MDM-controllers perform the asynchronous time division multiplex and demultiplex functions by scheduling the n VC-procedure controllers and directing the packets to the transmit buffers of level 2. Vice versa, packets waiting in the receive buffers of level 2 are lead to that VC-procedure control belonging to the appropriate VC of the packet.

3.2 Assumptions

For reasons of simple implementation of the model simplifying assumptions were made. The main one is that all levels are already initialized. That means level 2 is in the so-called active channel state and all n virtual circuits are in the data transfer phase. Hence, the dynamics given by the set-up and clear phases can be neglected. Furthermore, the bit-error probability of the FDX-line can be neglected and the receive buffers of level 2 are infinite. Therefore, there is no constraint to implement the link access procedure control in full detail. The last point which should be notified in this context is that for all investigations the one-way propagation delay and the processing delays of the LAP-control as well as of level 1 are added to one total propagation delay.

3.3 Simulation

This queuing model and the procedures recommended by X.25 are implemented in an event-by-event simulation program in full detail with regard to the assumptions mentioned above.

The program allows the free choice of a number of parameters, namely:

- number n of active virtual circuits
- window size w of each of the n virtual circuits
- mean value and type of distribution of inter-arrival time of user-data (messages) for each of the n virtual circuits
- mean value and type of distribution of message length l of the user-data for each of the n virtual circuits
- total one-way propagation delay t_p
- transmission rate v of the FDX-line
- buffer sizes of the VC-transmit and receive buffers as well as of the transmit buffer of level 2
- processing delays in level 3, i.e. time t_s for passing a message to the transmit buffer, including packetizing of a message, and time t_r to transfer the packet from the receive buffer to the VC-receive buffer, including the extraction of the message.

4. SIMULATION RESULTS

This chapter deals with the derived simulation results which allow a fast and accurate determination of performance characteristics of CCITT X.25, such as: maximum throughput, mean transfer time, and throughput class.

4.1 Maximum Throughput

As first interesting performance characteristics the outcomes of a study on the maximum throughput will be presented.

Fig.5 and 6 show the maximum throughput behavior as a function of the essential parameters: message length l , total propagation delay t_p , number n of handled active virtual circuits, and window size w .

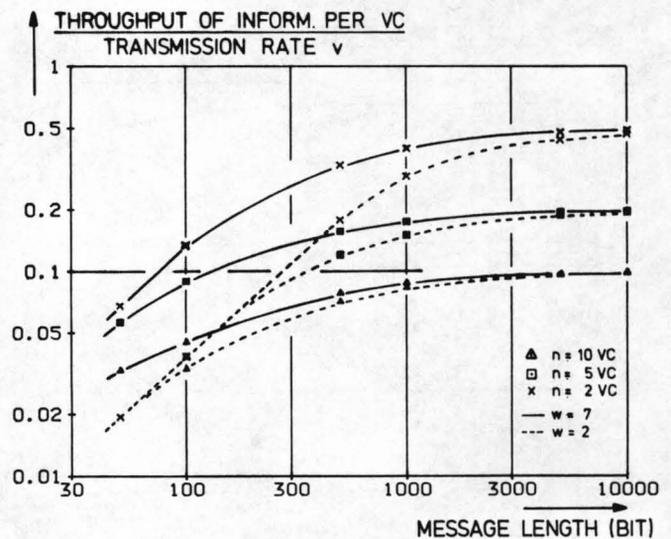


Fig.5: Throughput efficiency vs message length
Global parameters:
transmission rate $v = 48\ 000$ bit/s
total propagation delay $t_p = 50$ ms
L3-processing delay $t_s = t_r = 1$ ms

In Fig.5 the maximum throughput for each virtual circuit is depicted as a function of the message

length l , i.e. the data field length of a data-packet (see Fig.2). For reasons of simple presentation the throughput, defined as information bits per second, is normalized by the transmission rate v .

The curves show the typical throughput behavior as they reach the absolute possible maximum throughput asymptotically with increasing message length which is, obviously, the channel capacity divided by the number n of virtual circuits. For smaller message lengths, the increase of the throughput is quite linear to the message length for a number of active virtual circuits $n \leq 5$ and a window size $w=2$ (see dashed lines with cross and square marks). This is due to the high transmission rate.

Large message lengths enforce waiting times in the transmit buffer due to the greater offered load. This effect manifests itself in a beginning crookedness of the curve. For $n=10, w=2$ (dashed line with triangle marks) the offered load to the channel is high enough for the whole range of message lengths to cause waiting times which stop the linear increase of the throughput.

The explanation of the throughput behavior for the interface with a window size $w=7$ is virtually the same (see bold lines in Fig.5). Increasing the window size w from 2 to 7 yields a substantial improvement of the throughput. However, it can be seen from the reference curves with $w=2$ that the impact of $w=7$ is more distinct for smaller message lengths. In Fig.5 it can also be seen that for $n=2$ and message lengths $l \leq 200$ bit the improvement of the throughput is of the same factor 3.5 as the increase of the window size from 2 to 7. Therefore, it is obvious that in this range of message lengths the window mechanism of level 3 will be the bottleneck of the system.

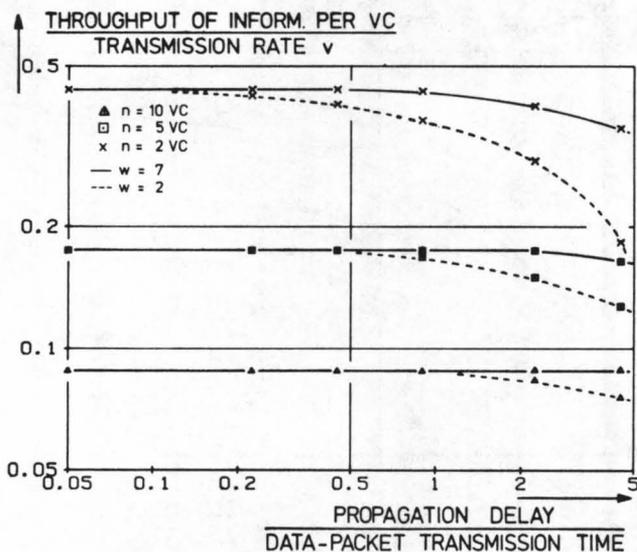


Fig.6: Throughput efficiency vs propagation delay relative to data-packet transmission time
 Global parameters:
 transmission rate $v = 48\ 000$ bit/s
 message length $l = 1\ 000$ bit
 data-packet transm.time $t_i = 22.3$ ms
 L3-processing delay $t_s = t_r = 1$ ms

Fig.6 shows the maximum throughput of information bits per second for each virtual circuit as a function of the total propagation delay t_p relative to the data-packet transmission time t_i . For reasons of clarity the message length l and the number of overhead bits of the data-packets are held constant at 1000 bit and 72 bit, respectively.

Considering first the case window size $w=2$ (dashed lines) one can see that the throughput reduction increases with growing propagation delay t_p . The reason for this effect is that, due to the longer propagation delays, lack of acknowledgments for proceeding the upper window edge occurs, and, therefore, the window-stops happen more often resulting in a throughput reduction.

The bold lines in Fig.6 reflect the improvement of the throughput in the case window size $w=7$. As depicted in the diagram, the values of maximum throughput do not become better when enlarging w from 2 to 7 in the range of $t_p/t_i < 0.2$. In this range even for a window size $w=2$ acknowledgments are received right in time to proceed the upper window edge just before window-stops occur. Therefore, increasing of w does not improve the throughput.

In contrast to this, the choice of $w=7$ effects a great enlargement of the throughput for propagation delays within the range of $t_p/t_i \geq 0.2$. Because of the greater window the probability to receive an acknowledgment before a window-stop happens is greater as in the case $w=2$. A little throughput reduction increases only in the range of $t_p/t_i > 1$ for $n=2$ and for $t_p/t_i > 2$ in the case $n=5$. In case of $n=10$ and $w=7$ the increase of t_p/t_i has generally no influence on the behavior of the throughput.

4.2 Mean Transfer Time

Further characteristic performance results are the outcomes for the mean transfer time which is defined as time a message spends in the system between arrival at the VC send buffer of the DTE (DCE) and departure at the correspondent VC receive buffer of the DTE (DTE).

In Fig.7 and 8 the behavior of X.25 with respect to the total channel load as well as to the mean transfer time is plotted as a function of message length l , number n of virtual circuits, window size w , for a constant offered load.

Fig.7 shows the total channel load, defined as bits per second transmitted over the physical channel of level 1, relative to the transmission rate v as a function of the message length l on condition that the total offered load to the system is held constant at $\rho = 0.6$. The offered load is defined by $\rho = (n \cdot \lambda \cdot l) / v$, where λ is the arrival rate of messages for each virtual circuit. For reasons of clarity it should be emphasized that all bits, such as bits of a data-packet, bits of a supervisory-packet as well as overhead bits, contribute to the total channel load.

As shown in the diagram, the curves intersect in wide ranges the line of 0.6 in all cases, except $n=2, w=2$ (dashed line with cross marks). Only for this case the curve will be close to the value of 0.6 for all message lengths $l \geq 1000$ bit. This behavior is enforced by the small window size $w=2$. In all other cases the intersection of the curves with line 0.6 is due to the enlarged number n of

virtual circuits and/or window size w as well as to the effect that on the average one additional supervisory-packet will be transmitted over the channel per data-packet. This means that 72 overhead bits and 72 bits of a supervisory-packet are transmitted per message, additionally. It is obvious that for small message lengths the offered load of information bits is low due to the relatively large total overhead (144 bits). Hence, the curves cross the line 0.6 necessarily. For greater message lengths the relative total overhead decreases and all curves reach the line 0.6 asymptotically. Therefore, the curves have a maximum in between.

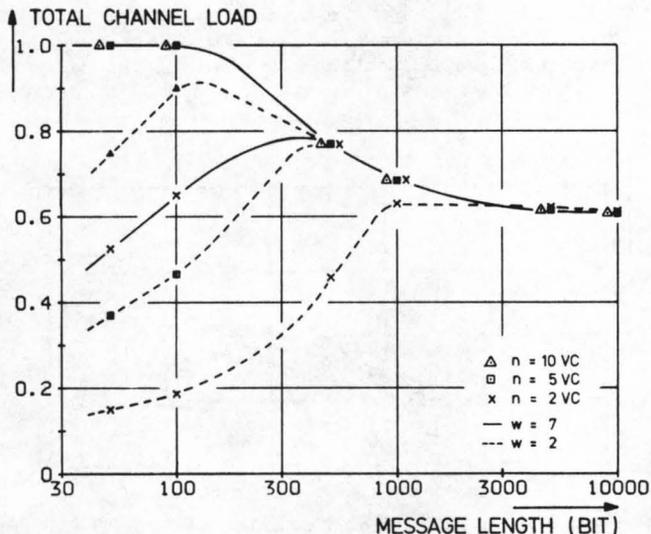


Fig. 7: Total channel load vs message length
Global parameters:
transmission rate $v = 48\ 000$ bit/s
constant offered load $\rho = 0.6$
total propagation delay $t_p = 50$ ms
L3-processing delay $t_s = t_r = 1$ ms

Further two effects can be read off from Fig. 7. First, as it is demonstrated by the curve of $n=5$, $w=7$ and $n=10$, $w=7$ (bold line with square and triangle marks) the channel will be saturated, i.e. total channel load = 1.0, for smaller message lengths. This is due to the relatively high total overheads of each of the n virtual circuits. Secondly, the diagram shows the bottlenecks of the system X.25: for smaller packets ($l \leq 100$ bit) the window mechanism will be the bottleneck in the case of $n=2$. Enlarging the window size w by the factor of 3.5, i.e. from 2 to 7, the total channel load also increases by the same factor. In the cases of $n > 2$ and $w=7$ the physical channel will be the bottleneck. This is shown by the curves for $n=5$, $w=7$ and $n=10$, $w=7$, as they reach the value of 1.0 for message lengths $l \leq 100$ bit.

In Fig. 8 the mean transfer time is depicted as a function of the message length l on condition that the total offered load is held constant at $\rho=0.6$. In case of $w=2$ and with increasing message lengths up to 100 bit the mean transfer time remains nearly constant. When still enlarging the message length the curves show characteristic minima.

This behavior could be explained from the results of Fig. 7: when enlarging the message length the total channel load decreases for $n=10$ virtual circuits, whereas the channel load still increases for the cases $n=5$ and $n=2$. Therefore, the mean transfer time for $n=10$ yields to values essentially below those belonging to smaller message lengths.

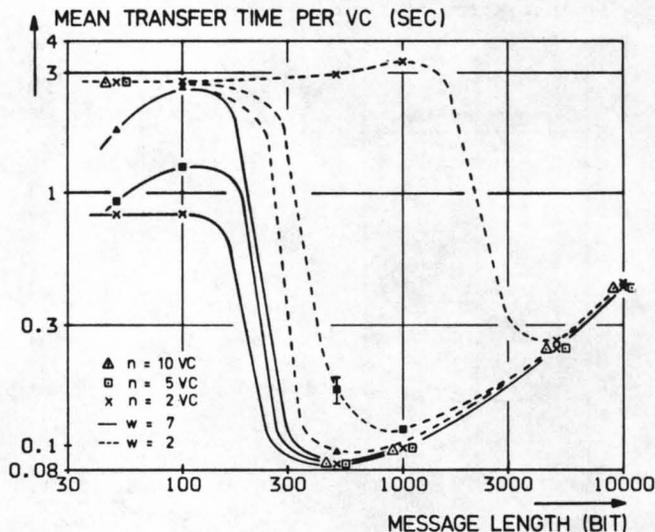


Fig. 8: Mean transfer time vs message length
Global parameters:
transmission rate $v = 48\ 000$ bit/s
constant offered load $\rho = 0.6$
total propagation delay $t_p = 50$ ms
L3-processing delay $t_s = t_r = 1$ ms

The same behavior can be seen from the curve of $n=5$, $w=2$ as well as $n=2$, $w=2$. The mean transfer time for these cases will decrease for values $l > 300$ bit and $l > 1000$ bit, respectively. When still enlarging the message length all curves will increase once more. This effect is due to waiting times which now appear in the send buffers. Hence, the curves with $w=2$ will have a minimum.

The behavior of the mean transfer time for the case $w=7$ is principally the same (see bold lines). When regarding Fig. 7, one can see that in the range $l \leq 100$ bit the total channel load for $n=2$, $w=7$ is quite below the curve of $n=5$, $w=7$ and $n=10$, $w=7$. With respect to this result it is clear that the mean transfer time for $n=2$, $w=7$ has lower values than in the cases $n=5$ and $n=10$. By means of the facts that both cases $n=5$ and $n=10$ yield to a total channel load equal to 1.0 as well as that the arrival rate for $n=5$ is twice the arrival rate for $n=10$ it is obvious that the mean transfer time for $n=5$ is half the time for $n=10$. Enlarging of the message length yields to a decrease of the channel load and, therefore, the mean transfer time begins to drop in the same manner as mentioned above. The reasons of the second increase of the transfer time are the same as described in the case $w=2$. Hence, in case of $w=7$, the curves show characteristic maxima as well as minima.

The next plot, Fig. 9, shows the behavior of the mean transfer time as a function of total offered load ρ , number n of virtual circuits and window

size w . Contrary to Fig.7 and 8, the message length l is held constant at 1000 bit, and the offered load ranges from 0.1 up to 1.0. For reasons of simple presentation, only the cases $n=2$ with $w=2$ and $w=7$ as well as $n=5, w=2$ have been plotted. The other cases show negligible deviations to the curve of $n=5, w=2$.

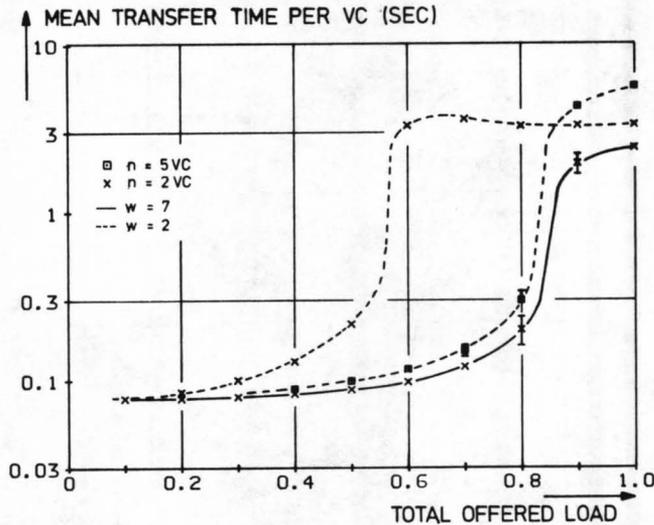


Fig.9: Mean transfer time vs total offered load
Global parameters:
transmission rate $v = 48\ 000$ bit/s
message length $l = 1\ 000$ bit
total propagation delay $t_p = 50$ ms
L3-processing delay $t_s = t_r = 1$ ms

The curve of the mean transfer time for the case $n=2, w=2$ (dashed line with cross marks) shows only small rise when increasing the offered load up to a value of 0.5. This effect is due to waiting times in the VC send buffer enforced by the small window size $w=2$. When choosing a value for the offered load of about 0.6 the curve shows a characteristic increase. The reason for this effect is that for offered loads in range ≥ 0.6 the window mechanism will be the bottleneck which means that in this range loss of messages will occur. Therefore, a message being accepted by the VC send buffer has to wait very long before it is transmitted across the interface. These long waiting times lead to the sharp bent.

Opposite to case $n=2, w=2$, the sharp increase at point 0.874 in the case of $n=5, w=2$ is due to a saturated channel. The value of this boundary can easily be found taking the total overhead (see notes to Fig.7) into consideration: one message of 1000 bit leads to 1144 bit on the channel on the average. Hence, the offered load will be enlarged by the factor 1.144. With respect to a saturated channel it follows: $\rho_{max} = 1.0 / 1.144 = 0.874$. Values of ρ higher than this margin will lead to loss of data which is reflected in the sharp bent of the mean transfer time.

The last curve of the diagram to be discussed is that of $n=2, w=7$ (bold line). These results reflect the real improvement for the mean transfer time in the case of a greater window size. The global behavior of the transfer time is just the same as in

the case $n=5, w=2$: small increase for enlarged offered loads as well as the sharp bent at point 0.874.

4.3 Throughput Classes

The two diagrams in this part of the paper, Fig.10 and 11, are dedicated to administrations and users as a tool for the default throughput class assignment or for the throughput class negotiation, respectively.

With the help of these plots the maximum throughput and hence, the appropriate throughput class can be determined easily as a function of the specified parameters, or vice versa. These two graphs show the typical results for the throughput characteristics (for comparison see Fig.5 and 6) as a function of the essential parameters such as message length l , propagation delay t_p , number n of virtual circuits and window size w .

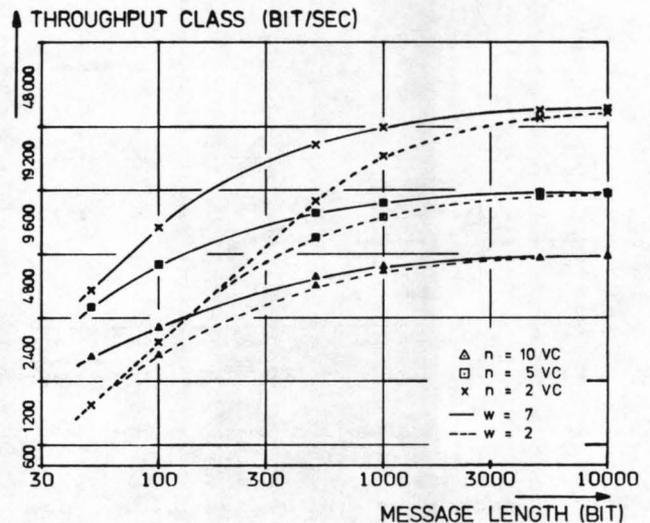


Fig.10: Throughput class as a function of message length, number of virtual circuits and window size
Global parameters:
transmission rate $v = 48\ 000$ bit/s
total propagation delay $t_p = 50$ ms
L3-processing delay $t_s = t_r = 1$ ms

In Fig.10 the maximum throughput of information bits per second for each virtual circuit is depicted as a function of the message length l . Opposite to Fig.5 the throughput is not relative to the transmission rate. Hence, the results are of dimension bit/s. For reasons of simple interpretation and easy determination, the ranges of the throughput classes as recommended by CCITT X.25 are drawn on the vertical axis of the diagram. Some examples are to underline the advantage of this presentation.

If $n=2$ virtual circuits with window size $w=2$ (see dashed line with cross marks) and message lengths l of about 1000 bit should be handled the throughput class 19 200 bit/s must be established at the interface. Even if transmitting only messages with lengths $l=500$ bit, the throughput class 9 600 bit/s has to be set up. For larger message lengths, $l > 3\ 000$ bit, even the highest throughput class

48 000 bit/s must be established.

The determination of the correspondent throughput class to all other possible combinations of n , l and w follows the same line.

On the other hand, if the throughput class is given, e.g. 4 800 bit/s, the interface could handle $n=10$ virtual circuits with $l=1000$ bit and $w=2$ or 7 without any reduction of the possible throughput. If only 5 or 2 virtual circuits were to be set up in this case, a sharp throughput reduction were the consequence if there is no possibility to change the throughput class to 9 600 bit/s or 19 200 bit/s, respectively.

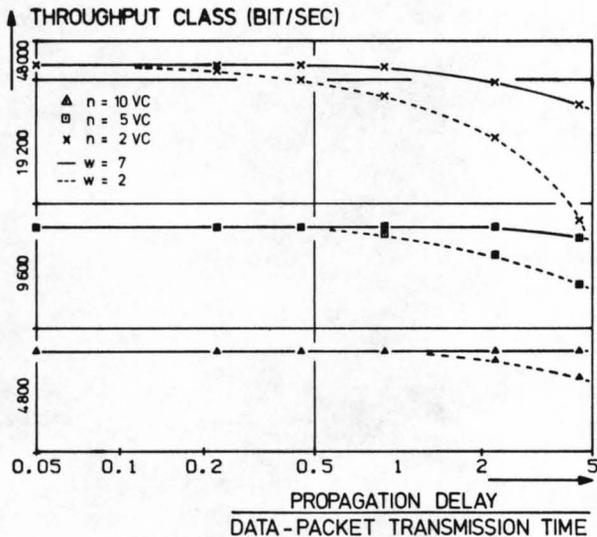


Fig.11: Throughput class as a function of propagation delay relative to data-packet transmission time, number of virtual circuits and window size

Global parameters:

transmission rate $v = 48\ 000$ bit/s
 message length $l = 1\ 000$ bit
 data-packet transm.time $t_i = 22.3$ ms
 L3-processing delay $t_s = t_r = 1$ ms

Fig.11 shows the maximum throughput of information bits per second for each virtual circuit as a function of the propagation delay t_p , relative to the data-packet transmission time t_i . The main difference to Fig.6 is that the throughput is not relative to the transmission rate. For the same reasons as mentioned to Fig.10, the vertical axis is intersected by the ranges of the correspondent throughput classes. Hence, throughput classes could be determined easily for given parameters, or vice versa.

Some concluding examples shall demonstrate the use of this diagram.

In case of handling $n=2$ virtual circuits with window size $w=2$ (dashed line, cross marks) and total propagation delay $t_p=22.3$ ms, i.e. $t_p/t_i=1.0$, there is a need to establish the throughput class 19 200 bit/s at the interface. In case of shorter delays, e.g. $t_p/t_i < 0.2$, the highest class 48 000 bit/s has to be set up. For very long delays, i.e. $t_p/t_i > 4$, it will be expedient to establish the next lower throughput class 9 600 bit/s.

Appropriate throughput classes to all other possible constellations of the parameters n , w and t_p/t_i can be determined easily in the same manner.

5. CONCLUSION

The main contribution of this paper is to show coherences between essential performance characteristics of CCITT X.25 such as maximum throughput as well as mean transfer time and the window flow control mechanism with variable window size w . It has been demonstrated that the implementation of a higher value of w leads to obvious improvements of the performance in the following cases:

- number of active virtual circuits $n < 10$
- mean message length $l \leq 1000$ bit
- propagation delay t_p relative to data-packet transmission time t_i in the range of $t_p/t_i > 0.5$
- total offered load $\rho > 0.5$

A second major intention was to give administrations and users an easy and usable tool for the throughput class assignment and for the throughput class negotiation. Some examples were shown how to determine the correspondent throughput class to a given combination of n , l , w and t_p/t_i and vice versa.

ACKNOWLEDGMENT

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REFERENCES

Due to the lack of space the following references represent only a few publications out of numerous valuable and interesting studies published in the recent years.

- /1/ CCITT-Recommendation X.25. CCITT Study Group VII, Doc. AP VII-No.7-E, June 1980.
- /2/ CCITT-Recommendation X.25. CCITT Yellow Book, Vol.VIII-2, Geneva, 1980.
- /3/ Sloman, M.S.: X.25 explained. Computer Communications, Vol.1, No.6, December 1980.
- /4/ Benutzerhandbuch DATEX-P. Fernmeldetechnisches Zentralamt der Deutschen Bundespost, 6/82.

Summary of Questions/Answers

Date: 13 June 1983

Session: 3.3

Paper: 6

Q.1 (P. Pawlita)

1. What distribution types are supposed for message-length and interarrival times of user data.
2. Does a single virtual circuit in your model permit simultaneous message transfer in both directions?

A.1 (W. Dieterle)

To the first part of your questions I shall mention that all published results are obtained with constant message length distributions as well as constant interarrival times distributions. Of course, there is the possibility to obtain results with all other standard distributions for message length and interarrival time such as, exponential, evlaupial and hyper exponential.

The answer to the second part of your question will be: in my simulation model all handled and active virtual circuits are bidirectional associations which means that for each virtual circuit a full-duplex message transfer occurs.

In addition to your question let me give the following remark: All results published in my paper are obtained with full-duplex virtual circuit connections with independent distributions for message lengths and interarrival times at the DTE as well as at the DCE.