ITC '88, 1.-8.6.88, Torino, Italy

Modelling and Performance Comparison of two Application Layer Protocols for Manufacturing Automation

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The performance of multi layered protocol architectures is evaluated with analytical and simulative methods by use of hierarchical modelling and repeated aggregation of submodels. Simulation results of the MAP (Manufacturing Automation Protocol) architecture are compared with these of a vendor specific protocol architecture. A simplified model of the MAP architecture is analysed and the results are compared with simulation results.

1. Problem Statement

Since the ISO (International Organization for Standardization) reference model for Open Systems Interconnection (OSI) [4] has been introduced, communication is structured into layers. The protocols form a multi layered protocol architecture like e.g. TOP (Technical and Office Protocol) and MAP (Manufacturing Automation Protocol) [15]. Besides the normal transparent data exchange, each protocol has different mechanisms like error control, window flow control, multiplexing or splitting. With the distributed implementation of such mechanisms a complexity is reached for which neither an overall closed analytic nor a simulative solution is possible.

Therefore, new ways to reduce the complexity are necessary like decomposition of loosely coupled systems and partly aggregation of subsystems and sublayers not being under study. After making the model accessible to an analytic or simulative solution without dropping the interesting parameters of the model, performance evaluation is done. If the submodel under study is the Transport Layer then the submodels to be aggregated are the Network and the Data Link Layer. Furthermore it is desirable to decompose the different connections.

This paper shows a way to evaluate the performace of whole protocol architectures used in Local Area Networks (LANs) for manufacturing automation (see Figure 1). The performance evaluation of the Media Access Control (MAC) sublayer Carrier Sense Multiple Access with Collision Detection [10] (CSMA/CD) can be done by simulation or by mathematical analysis using known solutions. The Logical Link Layer [9] and the Transport Layer [5] are jointly analysed, decomposing common processors to get separated connections. Network Layer has null functionality in these architectures. The flow controlled connection is analysed as a closed queueing network, which gives a flow equivalent service center, with enclosure of the flow control afterwards. The achieved message delays form an infinite server which represents the whole transport system. In a final step, one association within the Application Layer protocol between two users is simulated. For the MAP architecture a simplified analysis is performed, using a method similar to the method of Cobham [2] for a preemptive priority processor model and enclosure of the flow control as a M/GI/w analysis.

Layer	Automation Protocol Hierarchy	Manufacturing Automation Protocol Hierarchy
User	Numeric Control | Robot Control | ... | Process Control	Numeric Control | Robot Control | ... | Process Control
7b	Automation Protocol (AP) Monitor	ISO Manufacturing Message Specification (MMS) Monitor
7a	·	ISO Association Control Service Element (ACSE)
6	·	ISO Presentation Kernel (ASN.1 Encoder / Decoder)
5	·	ISO Session Kernel
4	ISO Transport Class 4	ISO Transport Class 4
3	·	·
2b	ISO Logical Link Control Type 1, Class 1	ISO Logical Link Control Type 1, Class 1
2a	ISO CSMA/CD | ISO Token Passing Bus	ISO CSMA/CD | ISO Token Passing Bus
1	Baseband | Broadband | Carrier Band	Baseband | Broadband | Carrier Band

Figure 1 : Protocol architectures

Section 2 shows the modelling of the whole protocol architectures, sections 3 and 4 show the simulation results and the analysis of the higher layers with results, respectively.

2. Modelling

The modelling is based on a hardware structure of a station as shown in Figure 2. There are two real processors at each station, one at the LAN board processing the LLC and Transport protocol, and one processing the higher layers and the application itself. The media access is realized by hardware and can be seen as a third processor. Following this structure, modelling and performance evaluation are divided into three steps as shown in the next sections.

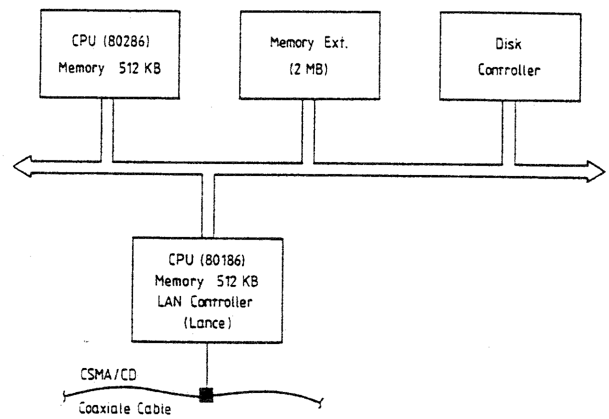

Figure 2 : Hardware structure of a station

2.1 Media Access Control

All stations are multiplexing their traffic on the common coaxial cable using the CSMA/CD protocol. Knowing the load (intensity and packet length) of each station and assuming marcovian arrival processes, the performace measures can be taken by simulation or approximative analysis [1,14]. The mean delay times are used to aggregate this sublayer to a packet length dependent infinite server for each communication path.

2.2 Logical Link Control and Transport

These two protocols are handled by the LAN board processor and therefore modelled and analysed together. At the LLC sublayer the connectionless type 1 procedure is used and modelled as a processing phase in sending and receiving direction. At the Transport Layer, the powerful ISO Transport protocol class 4 [5] is used. From the whole set of functionalities, transparent data exchange and flow control are modelled. In Figure 3 the situation of a communication from one server to multiple clients is shown [16]. The processor which handles the phases with preemptive priorities is approximately decomposed assuming marcovian conditions [18]. The mean admission delay is calculated by aggregating the whole chain without the flow control to a *Flow Equivalent Service Center* (FESC) [17]. The admission delay and the pure transfer time form again an infinite server to represent the transport subsystem.

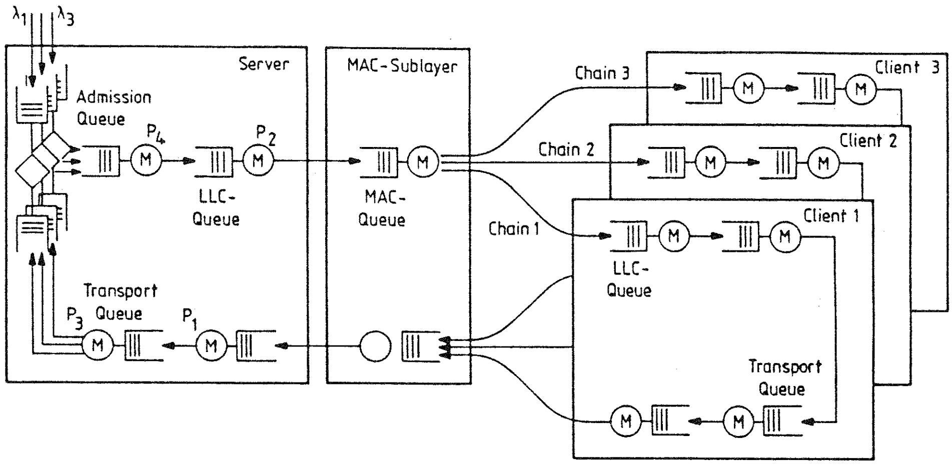

Figure 3 : Model of Logical Link Control and Transport Layer

2.3 Higher Layers

Two different Application Layer protocols are considered. One is a vendor specific Automation Protocol (AP) [3,19] and the other is the standardized protocol MMS (Manufacturing Message Specification) [15] in connection with ACSE (Association Control Service Element) [8], Presentation Kernel [11,12] and Session Kernel [6] for MAP. In Figures 4 and 5 the simulation models are shown. On the left hand side the client or requestor and on the right hand side the server or responder are depicted, with the parts necessary for this configuration. The complete model for one station is obtained, if the two parts of each figure are connected in mind. One common processor handles the higher layers and the application itself. The Transport system, which includes all layers below the *Transport Service Access Point* (TSAP) can be seen as infinite servers at the bottom of the model. We will consider exactly one transport connection. The parameters for the infinite servers are obtained from section 2.2.

A window flow control mechanism is modelled as a rhombus. The horizontal queue contains the credits. Each message takes with it a credit when it passes the rhombus. We consider the following flow controls:

1) Connection individual flow controls A and E (in Figure 5 additionally subdivided for unconfirmed and confirmed messages),
2) Window flow control B for segmented messages and
3) Flow controls C and D because of limited common resources.

On top of the Application Layer the user sends and receives messages. In Figure 4 each generator G_i refers to a multiplex channel. In Figure 5 only one context is depicted with different generators for unconfirmed and confirmed messages. The generators refer to one or more users.

Implementation details of the MAP architecture are taken from the Communications Network for Manufacturing Applications (CNMA) [20], which is a project within the European Strategic Program for Research and Development in Information Technology (ESPRIT).

In both models, all messages enter the monitor over a distribution phase V. This phase has the lowest priority of the processor to keep out further load if saturation is reached. The type of the message is recognized and the message is routed to a special queue according to its type.

In Figure 4 there are two different actions to be done after reception of the transport confirmation. In case of an unconfirmed message, a local confirmation has to be returned to the user in order to release occupied resources. In case of confirmed messages a timer has to be started in order to control the arrival of the confirmation (phase T_1). In Figure 4 there is

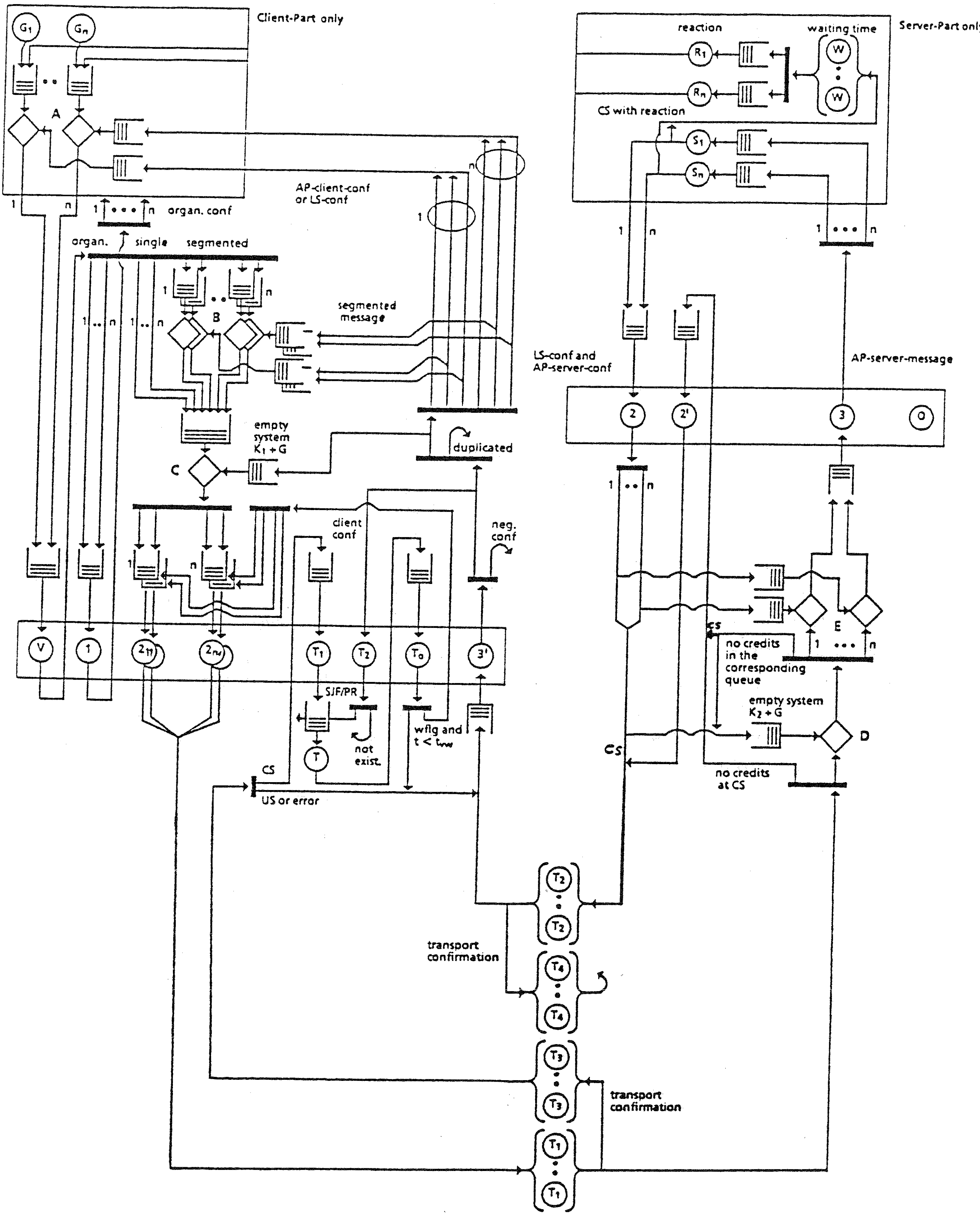

Figure 4 : Simulation model of the higher layers of the AP architecture

	Symbol	Legend	AP Param.	MMS Param.
Explanations	1 .. n	n Logical Multiplex Channels	1/2/10	1
		Decision		
		Duplication		
		Merging		
Flow Controls	A	Individual for the Channel (Client)		
		or for the Context (Requestor)		
		Amount of Credits (for US)	1/2/5/10	3/10/1000
		Amount of Credits (for CS)	1/2/5/10	1/2/5/10
	B	Segmented Message (Window)		
		Window Size	2	
	C	Limitation of Common Resources		
		(Client or Reqestor)		
		K_1 Credits only for C	10	10
		G Credits for C and D	30	30
	D	Limitation of Resources		
		(Server or Responder)		
		K_2 Credits only for D	10	10
		G Credits for C and D (see C)	30	30
	E	Individuell for the Channel (Server)		
		or for the Context (Responder)		
		Amount of Credits	1/2/5/10	10
Abbreviations	ACSE	Association Control Service Element		
	AP	Automation Protocol		
	conf	Confirmation		
	CS	Confirmed Service		
	LS	Local Interface		
	SJF/PR	Special Service Discipline		
	T	Hardware Timer		
	t	Time since the Message Generation		
	tvw	Administration Time		
	US	Unconfirmed Service		
	wflg	Retransmission Flag		
Monitor Phases	O	Overhead Phase	1 ms	1 ms
	1	For Organisatory Messages or M-Open	3 ms	1 ms
	2	For Positive Confirmations from the User	2.5 ms	3 ms
	$2'$	For Negative Confirmations from the User	2.5 ms	3 ms
	2_i	For Messages from the User	5 ms	3.5 ms
	3	For Messages to the User	7.5 ms	3 ms
	$3'$	For Confirmations to the User	4 ms	3 ms
	$3''$	For Transport Confirmations to the User		0.5 ms
	I	For M-Await Initiate		5.5 ms
	T_1	To Start a Timer	1.5 ms	
	T_2	To Stop a Timer	3.5 ms	
	T_0	For Timeouts of a Timer	1.5 ms	
	V	Distribution Phase	1.5 ms	1.5 ms
Other Phases	O	Overhead Phases		1 ms
	A_i	ACSE Phases		1.5 ms
	P_i	Presentation Phases		5 ms
	R	Responder Phase		5 ms
	R_i	Reaction Phases	5 ms	
	S_i	Server Phases or Session Phases	5 ms	3.5 ms
	T_1	Transport Delay (Message)	10.5 ms	10.5 ms
	T_2	Transport Delay (Confirmation)	7.5 ms	7.5 ms
	T_3	Transport Delay (T-Confirmation)	7.5 ms	7.5 ms
	W	Waiting Time until Reaction	500 ms	

Table 1 : Parameters of the simulation and legend to Figures 4 and 5

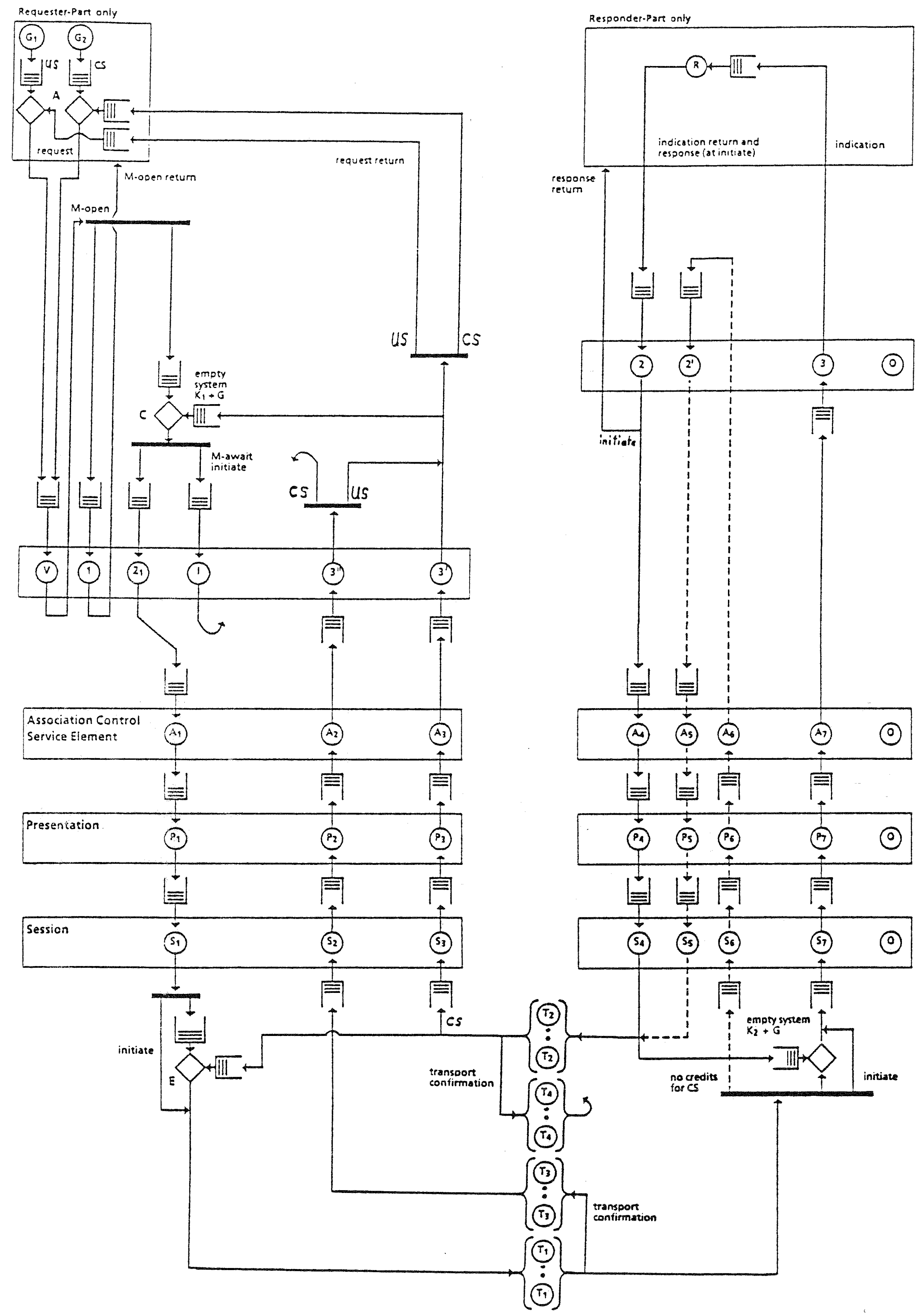

Figure 5 : Simulation model of the higher layers of the MAP architecture

also the possibility of having segmented messages or a reaction to a message after a waiting time W, which again is modelled as an infinite server.

In Figure 5 no timer is necessary because MMS assumes a reliable transport connection which, in case of error, at least creates a negative confirmation. Flow control E blocks the messages in Figure 5, in contrast to Figure 4, in front of the transport system if there is no credit available.

3 Simulation Results

Some simulation results, obtained by event by event simulation with confidence intervals of 90%, are depicted in Figures 6 – 9. Figures 6 and 7 refer to the AP architecture and Figure 8 and 9 to the MAP architecture. The priorities of the phases in Figure 4 decrease in the following direction: T_1, T_0, $3'$, 3, $2'$, 2, 2_i, 1, V. Each phase is followed by an overhead phase to consider the influence of the operating system. Only phase $3'$ is followed immediately by phase T_2. In order to avoid retransmissions we consider large timeout values. In Figure 5 the lower layers have a higher priority than higher layers and the receiving direction has a higher priority than the sending direction. Therefore, the MMS–Monitor has the lowest priority and priorities within the MMS–Monitor decrease in the direction $3''$, $3'$, 3, I, $2'$, 2, 2_1, 1, V.

In all figures the buffer occupation time of the sending station and the transfer time from the generation of a message at the sending user to the arrival of the message at the peer user are depicted for a different amount of credits in flow control A versus the offered load. The parameter constellation is typical and taken from real implementations (see Table 1). The generators produce traffic according to a marcovian interarrival time distribution. The curves are depicted in the stable range of the system.

The main part of the transfer times comes from passing through the sending station. All other parts are, because of the considered parameter constellation, constant and significantly smaller.

Figures 6 and 8 show the behaviour of unconfirmed services, whereas Figures 7 and 9 refer to confirmed services. The higher buffer occupation time of confirmed services compared to unconfirmed services result from the waiting time for the confirmation to release the buffer. For unconfirmed services the buffer at the sending user is released after the arrival of the transport confirmation.

With an increasing amount of credits the bottleneck in the considered configurations moves from flow control A to the processor phase V, which has the lowest priority. An interesting effect can be observed in Figure 8. Although the bottleneck moves as described above with an increasing amount of credits in flow control A, the buffer occupation time, as well as the transfer time are always the same for all numbers of credits in flow control A.

Because of much more processor phases at the MAP architecture compared to the AP architecture, all transfer and buffer occupation times are significantly larger and the border of stationarity is reached earlier.

4 Analysis

For the MAP architecture, an analysis with the simplified model of Figure 10, derived from the more detailled simulation model of Figure 5, is peformed. Because of the deterministic processor phases, the analysis can no longer be done with product form solution as at the Transport Layer. Therefore, the mean performace measures of the inner system without the flow control are taken according to a modified method of Cobham [2] for preemptive priorities assuming no losses and marcovian arrival conditions.

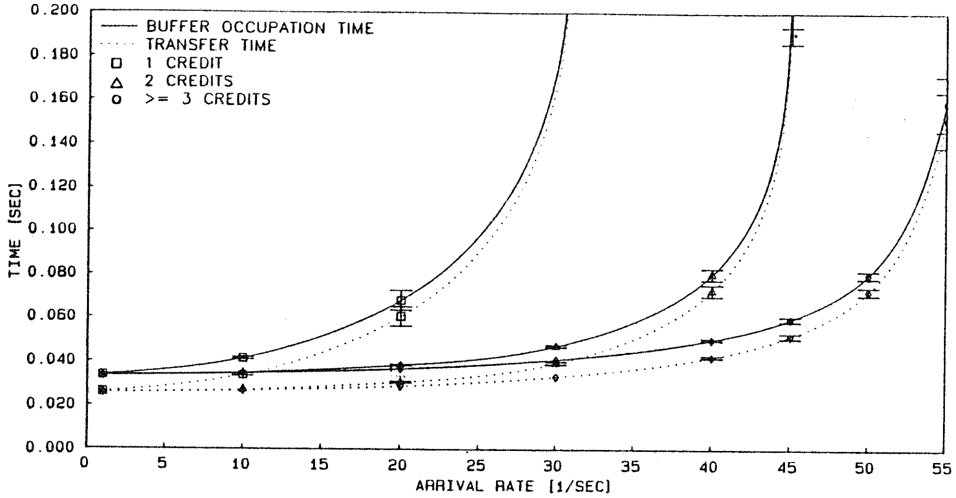

Figure 6 : Simulation results of the AP architecture for unconfirmed services

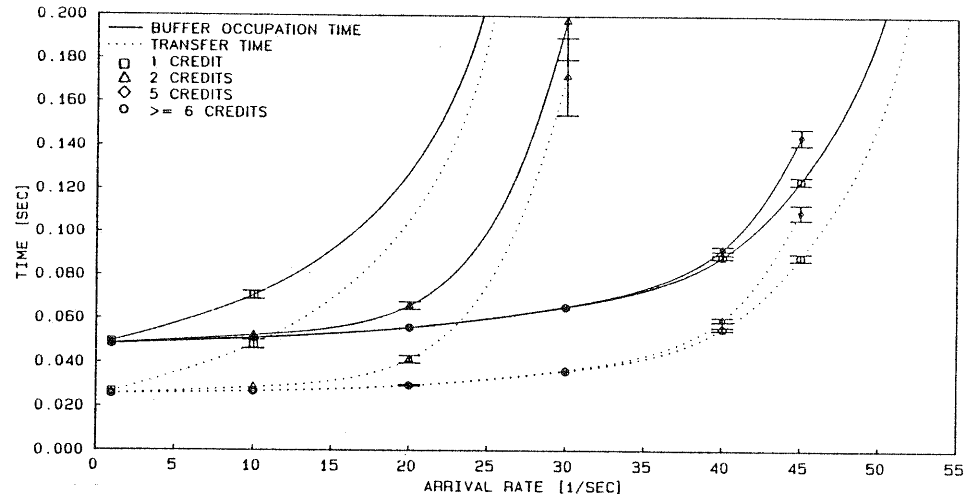

Figure 7 : Simulation results of the AP architecture for confirmed services

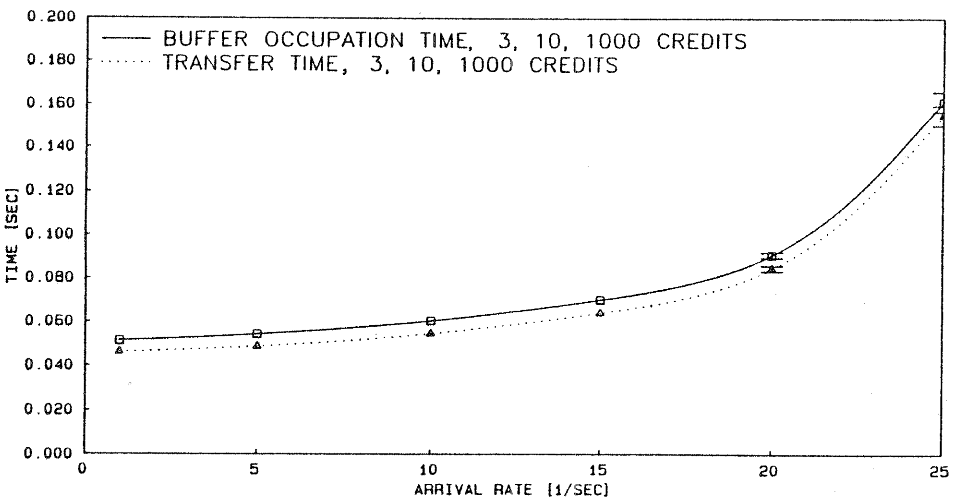

Figure 8 : Simulation results of the MAP architecture for unconfirmed services

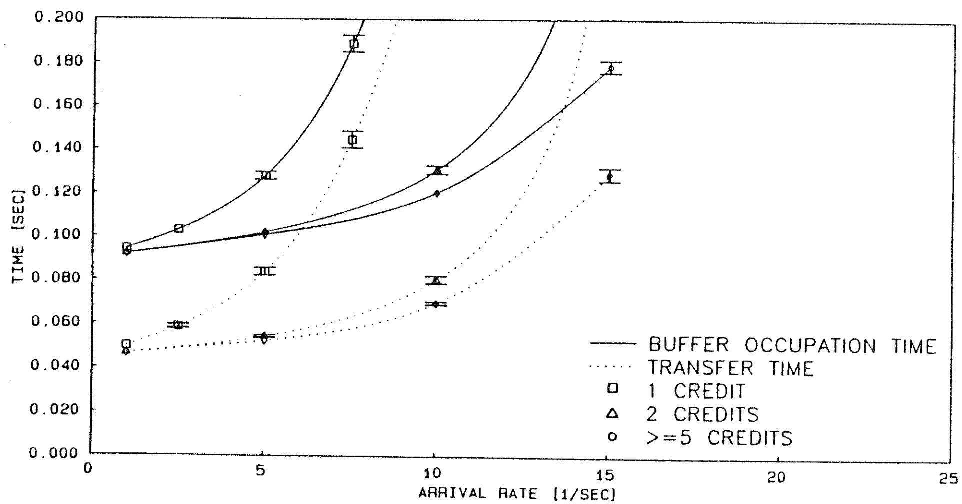

Figure 9 : Simulation results of the MAP architecture for confirmed services

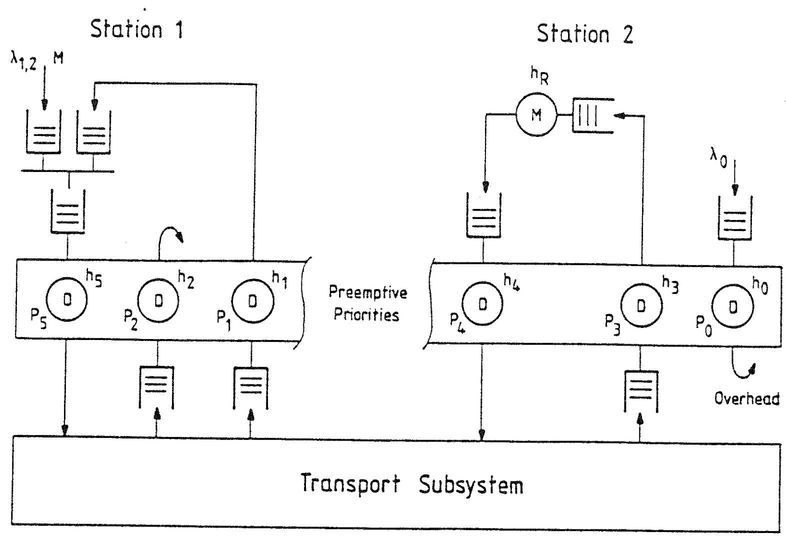

Figure 10 : Analytical model of the higher layers of the MAP architecture

For the various window sizes (w) the analysis is slighly different :

w=1: assuming only processing times (no waiting times),

w=2: assuming processing times and rest service times (no other waiting times) and

w>2: assuming processing and waiting times.

The addition of the waiting and processing times in the chain of the inner system gives the round trip delay and the inner system transfer time. The window flow control is taken into consideration by a following M/GI/w analysis with w as the window size. The GI distribution is composed of a D and M phase with the following parameters:

D : d = Round Trip Delay of the empty inner system and

M : h = Round Trip Delay of the inner system under load *minus* d.

The admission delay (t_{AD}) is given as the approximate waiting time of the M/GI/w system :

$$t_{AD} = \frac{1+c^2}{2} * T(M/M/w).$$

c : Coefficient of Variation of the GI distribution and

$T(M/M/w)$: Waiting time of the M/M/w system.

Addition of admission time and inner system transfer time gives the overall transfer time. The results are compared in Figure 11 with the simulation results obtained in section 3. Good accurancy is obtained for all window sizes under small load conditions. For heavy load, the results for window size 2 becomes a little less accurate.

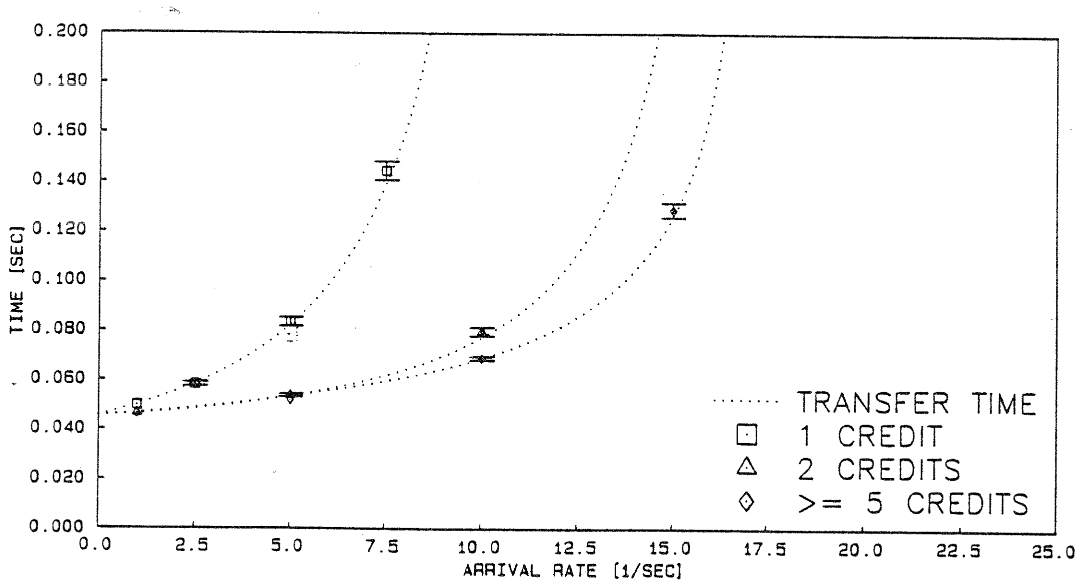

Figure 11 : Comparison of analytical and simulation results of the MAP architecture

5 Conclusion

We showed the modelling of multi layered protocol architectures and a concept to evaluate the performace predictions by use of repeatedly aggregated subsystems. Simulation results were given for a vendor specific protocol architecture as well as for the standardized MAP architecture. The modularity and higher functionality of the MAP architecture result in higher transfer times and lower throughput. Analytical results were obtained for a simplified model of the MAP architecture and the comparison with simulation results have shown good accurancy.

Acknowledgement

The authors would like to thank Hans–Hubert Hemberger and Waldemar Hersacher for the implementation of the simulation programs and for obtaining the simulation results.

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