Integrated 100-Gb/s ETDM Receiver

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***Abstract*—Ethernet in backbone networks has the potential to provide high-performance and cost-efficient networking solutions. Driven by the rapid growth of Ethernet traffic, it is likely that, in the transport network, the next step in terms of the data rate will be 100 Gb/s. In this paper, we report on an integrated electrical-time-division-multiplexing (ETDM) receiver for 100/107 Gb/s, which comprises 1 : 2 demultiplexing and clock-and-data recovery on a single chip. The ETDM receiver was tested successfully in 100- and 107-Gb/s transmission experiments over 480-km dispersion-managed fiber.**

***Index Terms*—Electrical-signal processing, Ethernet over wavelength division multiplexing (WDM), high-speed integrated SiGe circuits, optical communication, optical signal processing, 100-gigabit Ethernet (100 GbE).**

I. Introduction

CORE AND METRO networks provide the infrastructure for traffic aggregation in the metropolitan area and the interconnection of regions and countries at the top level of the carriers' network hierarchy.

Rising bandwidth demands—resulting from triple-play applications, storage area networks, peer-to-peer traffic, and grid computing—put network operators into a dilemma: Both the increasing share of packet traffic [1] and the request for high performance (Quality-of-Service, network resilience) require huge new investments in switching and transport technologies. Additionally, the complexity of these technologies imposes substantial financial burdens on network operators in the area of operational expenditures. At the same time, the revenues per-bandwidth unit are shrinking as flat-rate contract models prevail in the internet-access markets. Thus, economically efficient network architectures and new operation models are needed.

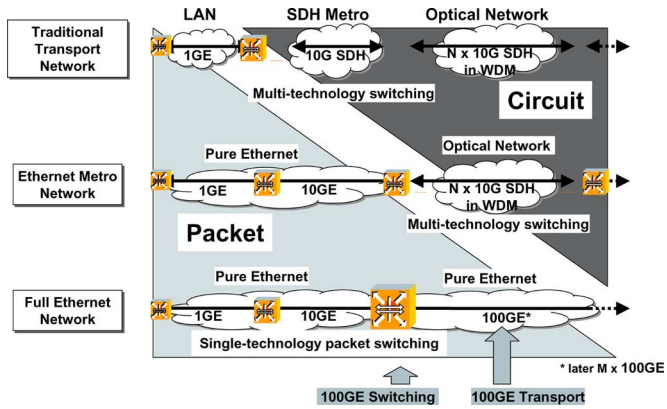

Fig. 1. Migration of Ethernet into MAN and core networks [4].

The usage of pure and possibly end-to-end Ethernet networks is a viable solution to this scenario. The industry-wide efforts and standardization activities [2], [3] to cover remaining challenges also confirm this outlook. Ethernet is generally characterized by simplicity, flexibility, interoperability, and low cost.

While Ethernet is traditionally a technology of local-area networks (LANs), continuous developments already enabled its deployment in metropolitan-area networks (MANs) Fig. 1. Recent research and standardization efforts aim at speeding up Ethernet to 100 Gb/s (100 GbE), resolving scalability issues, and supplying Ethernet with carrier-grade features. For this reason, in the near future, Ethernet might become an attractive choice and serious competitor in the market of backbone networks.

In order to be suited for core networks, Ethernet needs carrier-grade features, i.e., it has to offer and implement the correct Quality-of-Service, resilience, and network-management functions. Moreover, the scalability in terms of address space and maximum transmission distance (MTD) becomes an important issue for the next Ethernet generation. In [5], it was shown that the possibility to bypass Ethernet core nodes on the wavelength-division-multiplexing (WDM) layer might lead to huge port-count savings if MTD is large enough (e.g., 15% at an MTD of 300 km and 30% at an MTD of 600 km).

At the same time, the operational expenditures of the network architecture have to be as low as possible. This normally correlates with a small number of operated/managed objects in the network (elements and ports) and, in turn, makes high integration level and, thus, high port bandwidths indispensable. An in-depth analysis [6] demonstrated a considerable cost

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advantage of 100 GbE in comparison to synchronous-digital-hierarchy-based solutions. The superior capital-expenditure performance results from a huge cost advantage of Ethernet devices and their fast price decline. The reduced switch and line card count in 100-GbE networks and the efficient economics of Ethernet services will be responsible for a superior operational-cost performance. For such systems, 100-Gb/s serial transmission will be preferable and installed—once electrical components are available.

It is well known that data rates above 100 Gb/s can be transmitted over large distances (see, e.g., [6] and [7]) for 160-Gb/s transmission over deployed fiber and [8] for 160-Gb/s transmission over 4000 km in a ring experiment. However, the main challenge for 100 GbE is the development of cost-efficient solutions to decrease the cost per bit and kilometer below that of lower bit-rate systems. Here, the usage of ultrafast electronic circuits instead of elaborate optical methods is a promising approach for high-capacity optical-transmission systems [9], [10]. Electronic circuitry for 40 Gb/s is already commercially available. Transmission systems based on electrical-time-division-multiplexing (ETDM) operating above 80 Gb/s were reported recently [11]–[14]. In [11] and [12], the data rate was limited to 85 Gb/s and the electrical receiver comprised a number of small single circuits requiring an additional photo diode for the clock recovery. In [13] and [14], the data rate was 107 Gb/s, but the receiver included an optical time division demultiplexer and the clock was transmitted on a separate wavelength channel. To really exploit the cost advantage of an electrical receiver compared to optical solutions, a compact integrated device is needed—preferably a single chip.

As an important step toward 100 GbE, we present in this paper an integrated ETDM receiver, comprising 1 : 2 demultiplexing (DEMUX) and clock-and-data recovery (CDR) on a single chip. The integrated ETDM receiver will be described in detail in Section II. In [15], we demonstrated this integrated ETDM receiver in a transmission experiment at a data rate of 100 Gb/s using a return-to-zero ON-OFF-keying (RZ-OOK) optical-time-division-multiplexing (OTDM) transmitter. In Section III, we will describe this experiment in detail. In addition to [15], we also show here that the same chip is capable of operating at an increased data rate of 107 Gb/s—the rate expected for future 100-Gb/s Ethernet-transport networks including forward error correction (FEC). Error-free performance after 480-km dispersion-managed fiber (DMF) was achieved. This is the first demonstration of a single-chip ETDM receiver at 107 Gb/s in a transmission experiment. Finally, this paper will be summarized in the concluding Section IV.

II. Integrated ETDM Receiver

A. Circuit Description

The development of the integrated ETDM receiver chip is based on the results of a similar receiver already successfully operated in a 40-Gb/s system [16] but without on-chip phase-locked loop (PLL). A block diagram of the chip is shown in Fig. 2. It was designed for 80-Gb/s operation with FEC (86 Gb/s) and successfully operated in transmission experiments with 86 Gb/s and 100 Gb/s [15]. The receiver chip was fabricated in a SiGe-bipolar process (180-GHz transit frequency, 200-GHz maximum oscillation frequency), a predecessor of Infineon Technologies' B7HF200 technology [17]. A more detailed description of the circuit including its electrical characterization is given in [18]. In addition to the information given there, it should be mentioned that the chip also incorporates a 1/2 static-frequency divider, which provides half of the output clock frequency (e.g., 21.5 GHz in the case of 86-Gb/s data signals). This function is used to simplify sampling-scope triggering and half-rate demultiplexing application.

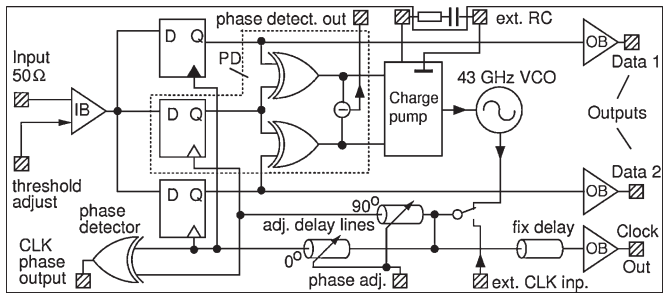

Fig. 2. Block diagram of the integrated ETDM receiver chip.

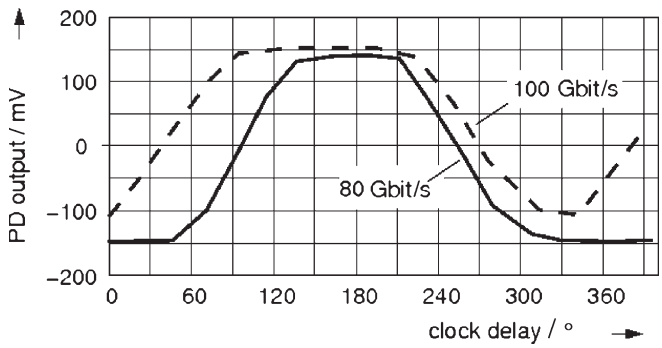

Fig. 3. PD output voltage versus clock-to-data delay in degrees for operation with 80 and 100 Gb/s.

Despite the fact that the chip was designed for 86 Gb/s, the design methodology applied enabled operation at more than 100 Gb/s. Only the internal voltage-controlled oscillator (VCO) could not be used as it was not designed for such an extremely large tuning range. However, the ETDM receiver-chip design offers the opportunity to insert an external 50-GHz VCO into the PLL. The VCO output is connected to the external clock input ("ext. CLK inp." in Fig. 2) of the chip. The feedback signal to the VCO is derived from the chip internally generated phase-detector (PD) signal via an external control circuit, which replaces the charge-pump circuit on the chip.

A measurement result of the PD output signal for 100 Gb/s as well as for 80 Gb/s is shown in Fig. 3. At 100 Gb/s, the clock-delay range in the "high" state of the curve is significantly longer than that in the low state. This asymmetry is mainly caused by a frequency-dependent difference in delay between the 90° and 0° delay line. While the adjusted delay causes a phase shift of approximately 90° at 43-GHz clock frequency, the phase shift increase to $50/43 \times 90^\circ \approx 105^\circ$ at 50 GHz. A symmetrical PD curve can be obtained by decreasing the difference in delay between the 90° and the 0° delay line, using

the phase-adjustment input of the chip. Please note that the curve for 100 Gb/s is not strictly repeating after 360°. This is due to a limited setting accuracy of the clock delay, since a delay of 30° (one scale division on the x-axis) for the 100-Gb/s curve corresponds to 833 fs only.

For upcoming 107-Gb/s designs, the integration of a complete PLL with 53.5-GHz VCO appears feasible, since proper VCO operation at even higher frequencies has been reported for the same semiconductor process as used for the receiver chip [19].

B. Design Concept

In the high-speed part of the receiver, there are 44 cells running with speeds greater or equal 50 Gb/s, respectively, 50 GHz. The cells with basic functions are input amplifier, master–slave-D-flipflop (MS-D-FF), exclusive-OR, intermediate and output buffer, as well as VCO. Except VCO and input amplifier, all the other cells are used several times in the design. This holds especially for the intermediate amplifier cell (not shown in Fig. 2), which is used as a repeater amplifier (buffer) along longer transmission lines, as well as five times in each delay element (cf. [18]).

In order to minimize design time and risk, a standard cell-based design approach was used, which was also successfully applied to the design of a 100-Gb/s 2 : 1 MUX [18]. In principle, in this approach, the complete design was build up from verified standard cells taken from a cell library. While this design concept is very common to high-integration designs at comparably low speed, it needs to be adapted to high-speed requirements. This is achieved by differential operation of all cells and their routing, following the design rules given in [20]. In the standard cell-based design concept applied, major areas of concern are the power level and interfaces of the cells, as described below.

C. Cell Power Level

Low power consumption is essential, since the transistor speed decreases if the transistor enters the region of the high-current effect due to a high junction temperature (cf. [20]). Also, for the sake of reliability, the width of metallization at the points of maximum current density needs to be increased significantly if the temperature rises above 110 °C, . . . , 120 °C. This increases the parasitic capacitance and, therefore, reduces the maximum speed. Therefore, already in the development phase of the library cells, the adequate power level (driving capability) of the cells needs to be determined. It is a tradeoff between the required speed and the rise in chip temperature due to power dissipation of the cells (cf. [20]). The ability of the chip to operate above 100 Gb/s indicates that the cell power level for the originally intended operation at 86 Gb/s could be decreased in favor of a lower power density, which is currently as high as 1.3 W/mm^2.

D. Cell Interfaces

Regardless of its function, in principle, each cell on the chip consists of a succession of load resistors (R_L), emitter followers (EF), and current switches or transadmittance stages (both referred to as CS) [20]. The load resistor is the simplest form of a transimpedance stage (TIS). In this design, it was preferred to an active TIS because, in combination with the driving CS, it shows the lower total power consumption at a comparable high cutoff frequency and output voltage swing. For the design, a source current of 4.4 mA for the driving CS and a load resistance of $R_L = 65\ \Omega$ was chosen.

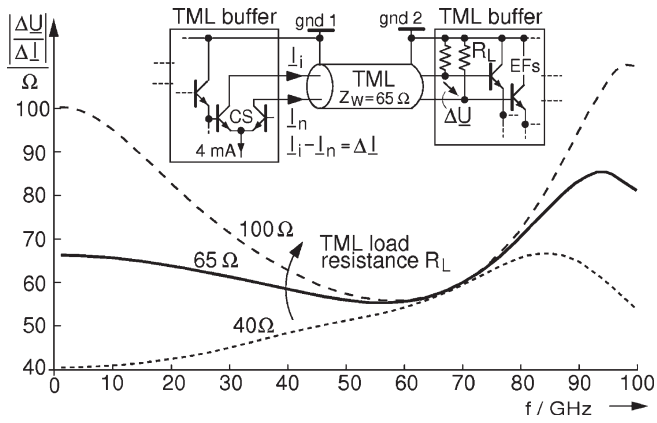

Fig. 4. Simulation result for an odd-mode transfer function of a 500-μm TML, loaded by a TML buffer with input resistors $R_L = 40, 65$, and $100\ \Omega$.

Owing to the high output impedance of the CS in relation to R_L, this interface shows the best mismatch between source and load impedance compared to the other possible interfaces (i.e., R_L–EF, EF–EF, or EF–CS). For the cell-based design approach, a mismatch is essential for decoupling the electrical properties of adjacent cells at the interface. It enables a cell to keep its electrical properties and performance, independent of the driving or loading cell type. Therefore, the CS–R_L interface is used as a general I/O interface for all cells in the cell library. The same considerations—but at a higher power consumption—would apply if an active TIS instead of R_L were used.

E. Transmission-Line Routing

For signal routing between the cells, microstrip transmission lines (TML) are used. In order to save driver power, TMLs with the highest characteristic impedance possible in the technology are realized. From the four metallization levels available (M1 to M4), thick upper metal M4 was used to realize two low-ohmic weakly coupled conductors with 12-μm spacing and $2.4 \times 2.5\ \mu$m^2 cross section each. For the current-return path, layer M2 is used, which is realized together with M1 as large global ground/power supply plane. Three-dimensonal electromagnetic simulations on this TML configuration, considering mandatory voids introduced to the supply plane due to the metal-density rules, show a characteristic odd-mode impedance of $Z_W = 65\ \Omega$. In combination with the load resistor $R_L = 65\ \Omega$ at a cell input, this yields a TML match at the far end.

The maximum line lengths are 280 μm for each 100-Gb/s TML between input buffer (IB) and MS-D-FFs (cf. Fig. 2) and 500 μm between two succeeding TML-buffers in the 50-GHz clock distribution. Fig. 4 shows a simulation result for the odd-mode transfer function of a 500-μm TML, terminated with a

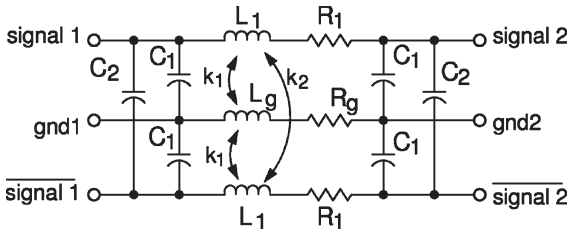

Fig. 5. TML segment model used for line lengths up to 50 μm.

TML buffer with input-load resistances R_L smaller (40 Ω), equal (65 Ω), and larger (100 Ω) than Z_W.

For the design $R_L = Z_W = 65\ \Omega$ was chosen because of the best compromise between flat-frequency response, high cutoff frequency, and low source current for the driving CS. Furthermore, this configuration shows nearly the same group delay for data (broadband) and clock (single frequency) signals. This allows matching of TML delays based on physical rather than on electrical TML lengths.

F. Even/Odd-Mode-Signal Considerations

In principle, a differential circuit can propagate a signal in the even as well as in the odd mode. In order to benefit from the advantages of differential operation [20], the signal is propagated throughout the entire chip in the odd mode only. Noise (e.g., switching noise or ground bounce) or fractions of the signal (e.g., due to single-ended operation at the receiver I/Os or unbalanced circuitry) in even mode are prevented from interfering the signal in odd mode by balancing the circuitry. This is obtained by a highly symmetrical layout of the library cells and signal paths.

However, for data signals [nonreturn-to-zero (NRZ)], a balanced circuit like the receiver becomes unbalanced during transients (ΔI-noise) as well as in any "digital" high or low state. Thus, signal and noise in even mode can convert to odd mode and vice versa throughout the entire chip. This may have a major influence on circuit performance or even cause unstable behavior of the circuit. Considerable simulation and optimization work was carried out in order to address the aforementioned issues adequately.

In the circuit simulation, the physical TML model of Fig. 5 was used for line lengths up to 50 μm. Longer lines were modeled by using this model for a sectional approximation. The model structure corresponds to the physical representation of the TML and, therefore, considers odd as well as even mode adequately.

It accounts for inductive and capacitive coupling between both conductors as well as between each conductor and the ground plane. Skin effects, as well as proximity effects, are not considered in order to reduce model complexity. Instead, the influence of these effects is considered in simulation by a simple parameter variation in the above model.

Owing to the small spacing between the signal-conductors and their high coupling to the return path (ground plane), the return path can be modeled as one conductor considering its inductive and resistive nature by the elements L_g and R_g. This model separates ground at TML input from that at the output. This separation is mandatory to insert the model into the global ground and power-supply plane model, which consists of two large C-coupled R–L meshes. With that global ground/supply-plane model, even-mode behavior of the entire chip including assembly parasitics (e.g., ground / power-supply bond wires) can be simulated adequately.

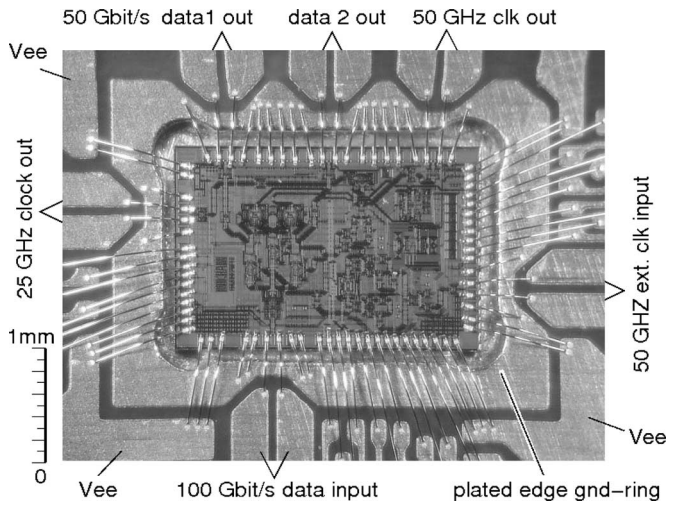

Fig. 6. Micrograph of chip assembly.

G. Chip Assembly

Details of the chip and module assembly were already presented in [18]. Fig. 6 shows a micrograph of the receiver chip. Conventional wedge–wedge ultrasonic bonding using 17.5-μm Al bond-wires was used to connect the chip to the TMLs on the polytetrafluoroethylene (PTFE) substrate. Bond-wire length at the 100-Gb/s input is approximately 0.5 mm with a spacing of 100 μm. Shorter wires of about 250 μm can be realized if the ground ring is left out at the data input (cf. Fig. 6).

On the other hand, in this kind of assembly technique, the ground ring is mandatory to keep the parasitic inductance to ground as small as possible. Therefore, the ground-ring metal on top of the PTFE substrate allows for multiple short ground bonds in parallel (four bonds in Fig. 6). This reduces the effective ground-bond inductance and also the effective inductance of the input bond wires via inductive coupling to the ground bonds. Furthermore, as a part of the ground ring, the edge metallization of the chip cavity provides a low-inductive current-return path from the ground bond wires on top of the substrate to the input TML ground at the substrate backside.

Thus, leaving out the ground ring at the input would increase the parasitic inductance to ground and, therefore, reduce the improvement gained by shorter signal bond wires. In addition, as a particular problem due to the single-ended interface to the photodiode (PDi), a higher inductance to ground is expected to reduce the common-mode noise-rejection ratio of the input buffer (IB) and is prone to cause stability problems.

Therefore, we decided to keep the ground ring with the long signal bond wires at the 100-Gb/s input. Measurement results at the receiver-module input, including TML and V-connectors,

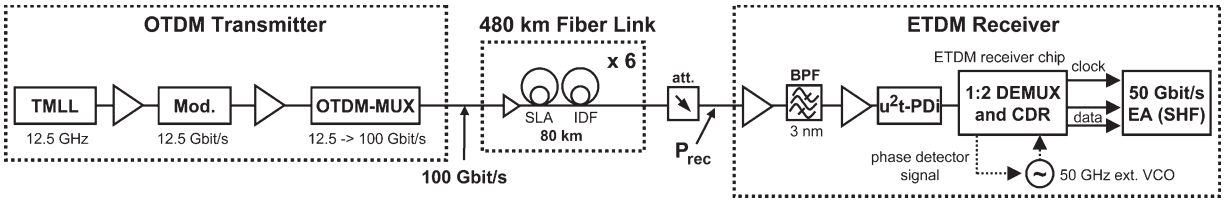

Fig. 7. Schematic depiction of the experimental setup for 100-Gb/s transmission.

show a single-ended input-return loss of $S_{11} \leq -8$ dB up to 50 GHz. This result is subject to further optimization, applying advanced even/odd-mode-compensation techniques [21]. However, results of the transmission experiments in the next section show that even the conventional bonding technique with moderate bond-wire lengths used in this first approach is suitable for operation at 100 Gb/s.

III. Transmission Experiments

The integrated ETDM receiver described in Section II was tested in transmission experiments at 100 Gb/s and 107 Gb/s. A special transmitter based on OTDM was used to generate a high-quality RZ-OOK data signal at these high bit rates. In this section, the experimental setup and the achieved results are discussed.

A. Experimental Setup

A schematic of the experimental setup is shown in Fig. 7. It comprised an OTDM transmitter, a 480-km fiber link, and an ETDM receiver. In the transmitter, a 12.5-GHz semiconductor mode-locked pulse source (TMLL) emitted optical pulses (pulsewidth of 1.3 ps and center wavelength of 1551.5 nm), which were amplified and intensity modulated at 12.5 Gb/s with a $LiNbO_3$ Mach–Zehnder modulator. The data signal was amplified and multiplexed in an OTDM-MUX from 12.5 to 100 Gb/s. The duty cycle of the OTDM transmitter was only 13%, which is significantly shorter compared to a standard RZ transmitter.

The fiber link consisted of six 80-km spans of DMF (53-km superlarge-area (SLA) fiber with $D = 20$ ps/nm/km, 27-km inverse-dispersion fiber (IDF) with $D = -40$ ps/nm/km, provided by OFS Denmark). The fiber link was 100% dispersion and dispersion-slope compensated. The span input power was +7 dBm. The use of SLA–IDF allowed a higher span input power compared to standard single-mode fiber and, thus, a longer transmission distance. The average differential group delay (DGD) of the link was 1.0 ps. Due to the high bit rate, even such low DGD values would require schemes for mitigation of polarization-mode dispersion or additional system margin.

In the receiver, the data signal was optically preamplified to +12-dBm average power using two erbium-doped fiber amplifiers with a 3-nm bandpass filter in between and detected with a high-speed PDi provided by u^2t photonics. The electrical 100-Gb/s signal was fed into the integrated ETDM receiver chip presented in Section II, comprising the 1 : 2 DEMUX and the CDR. As aforementioned in Section II, the internal VCO on the ETDM receiver chip was designed for 86 Gb/s and, therefore, could not be used. For operation at 100 Gb/s and above, an external VCO (provided by Agilent Technologies) was used instead with a control circuit driven by the PD signal generated in the receiver chip. The demultiplexed 50-Gb/s tributaries were detected with an error analyzer [(EA) provided by SHF technologies] synchronized by the recovered 25-GHz clock signal from the receiver chip. An optical attenuator in conjunction with the preamplifier was used to vary the received power (P_{rec}, as indicated in Fig. 7).

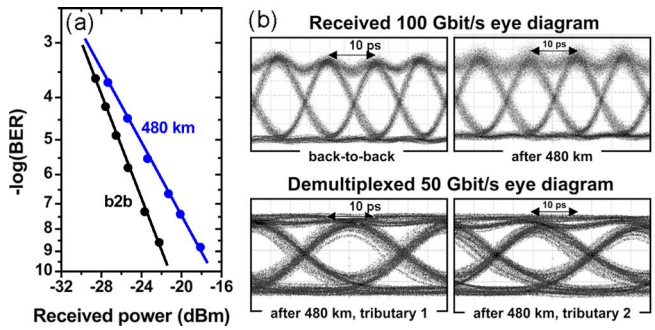

Fig. 8. (a) Bit-error measurements at 100 Gb/s back-to-back (b2b) and after transmission over 480-km DMF, using a word length of $2^7 - 1$. (b) Top: 100-Gb/s eye diagrams at the receiver back-to-back and after 480-km DMF. Bottom: 50-Gb/s eye diagrams after the electrical demultiplexer for both tributaries.

B. 100-Gb/s Transmission Experiment

The experimental results at 100 Gb/s are shown in Fig. 8. On the left-hand side [Fig. 8(a)], the bit-error ratio (BER) measured for the 100-Gb/s data signal is shown as a function of the optical power P_{rec}. Error-free performance $(\mathrm{BER} < 10^{-9})$ was achieved back-to-back and after transmission over the 480-km fiber link. The receiver sensitivity was −22 dBm back-to-back for a BER of 10^{-9}. The required optical signal-to-noise ratio (OSNR, 0.1 nm) for a BER of 10^{-9} was 28.6 dB back-to-back.

Both demultiplexed 50-Gb/s tributaries after the ETDM receiver chip were measured and the results were identical. The corresponding 50-Gb/s eye diagrams are shown in Fig. 8(b). Also, the eye diagrams of the 100-Gb/s data-signal back-to-back and after transmission at the input of the receiver are plotted in Fig. 8(b). The eye diagrams at 100 Gb/s were measured with a high-bandwidth PDi and a fast-electrical-sampling oscilloscope (70-GHz bandwidth).

Note that the OTDM-MUX in the transmitter was designed for standard synchronous-transport-module base rates and did

not preserve the pseudorandom bit sequence at 100 Gb/s. Therefore, the EA was programmed to the expected bit pattern at a word length of 508 bit $(4 \times 2^7 - 1)$. However, the delay in the OTDM-MUX was about 47 bit at 100 Gb/s, which is sufficient to decorrelate the data pattern.

A test of the receiver chip at a longer word length of $2^{31} - 1$ was not possible, because the EA could not be programmed for such a long word length. However, for the experiments at 107 Gb/s, the setup was modified and measurements at longer word lengths were possible. The experiments at 107 Gb/s are described in the next paragraph.

C. 107-Gb/s Transmission Experiment

The ETDM receiver chip was also tested at an increased data rate of 107 Gb/s, which corresponds to a 100-Gb/s transmission with 7% FEC overhead. For this experiment, the setup was slightly changed.

In the transmitter, the repetition rate of the TMLL was increased to 13.375 GHz and the intensity modulator operated at 13.375 Gb/s. Also, the delays in the OTDM-MUX were adapted to enable multiplexing from 13.375 to 107 Gb/s. Please note also that at 107 Gb/s, the pseudorandom-bit sequence was not preserved. However, the delay in the OTDM-MUX at 107 Gb/s was about 42 bit, which is still sufficient to decorrelate the data pattern.

The fiber link was unchanged compared to the 100-Gb/s experiment. The span input power was increased to +9 dBm. Using this input power, an OSNR of 32 dB was achieved at the output of the transmission link. No effects from fiber nonlinearities were observed due to the use of SLA fiber and the relatively short overall transmission distance.

In the receiver, the center frequency of the external VCO was increased to 53.5 GHz and the 50-Gb/s EA was replaced by an electrical 1 : 4 ETDM DEMUX with subsequent 13.375-Gb/s EA. This means that the bit-error rate at 107 Gb/s was determined by measuring all subchannels at 13.375 Gb/s, which corresponds to the OTDM base rate in the transmitter. By measuring the bit-error rate at the OTDM base rate, programming of the EA was not necessary and longer word lengths could be used.

For optimum performance of the ETDM receiver at 107 Gb/s, the frequency-dependent delay between the 90° and 0° delay line on the receiver chip had to be adjusted by applying an external control voltage, as was explained in Section II-A.

The experimental results for 107 Gb/s are shown in Figs. 9 and 10. In the upper part of Fig. 9, eye diagrams are plotted for the 107-Gb/s data-signal back-to-back and after transmission. They were measured with a high-bandwidth PDi and a 70-GHz electrical-sampling oscilloscope at the input of the receiver. The lower part of Fig. 9 shows eye diagrams of both 53.5-Gb/s tributaries, measured at the outputs of the integrated ETDM receiver.

In Fig. 10, the BER is plotted as a function of the received optical power P_{rec} for 107 Gb/s at a word length of $2^7 - 1$ and $2^{31} - 1$. Each BER curve was obtained by measuring and averaging over all eight ETDM subchannels. Error-free performance $(\mathrm{BER} < 10^{-9})$ was achieved back-to-back and

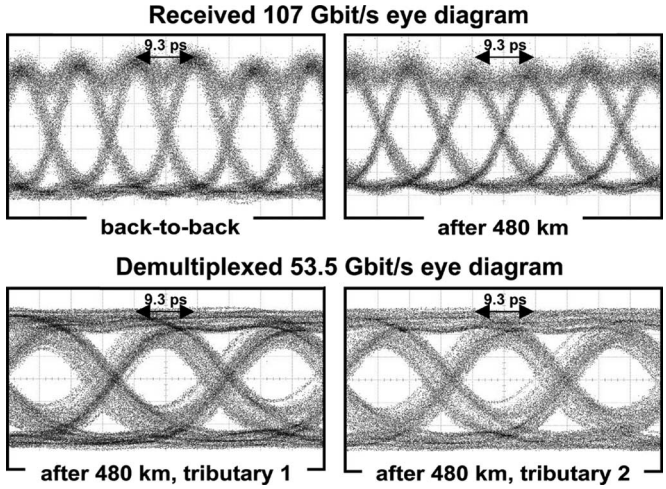

Fig. 9. Received eye diagrams at 107 Gb/s.

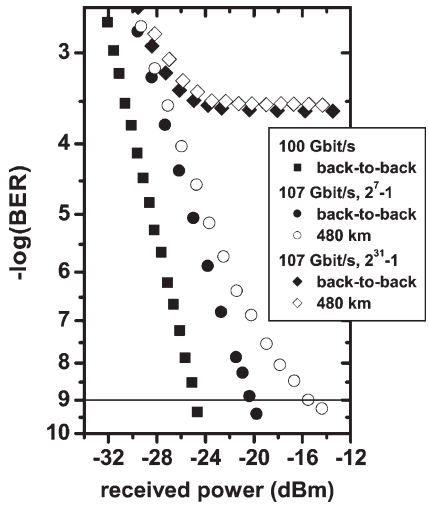

Fig. 10. Bit-error-rate measurements at 100 (word length $2^7 - 1$) and at 107 Gb/s (word length $2^7 - 1$ and $2^{31} - 1$).

over the transmission link for a word length of $2^7 - 1$. The required OSNR was 32 dB and 24 dB for a BER of 10^{-9} and 10^{-3} at 107 Gb/s, respectively. The relationship between OSNR and received power was linear within the plotted power range in the back-to-back case. The available OSNR after the transmission link was around 33 dB, which explains the indication of an error floor in the BER measurement after the transmission link and indicates that no OSNR penalty due to transmission was present.

The receiver chip was also tested at a longer word length of $2^{31} - 1$ and a performance degradation is observed (see Fig. 10) with a clear error floor around a BER of 3×10^{-4} back-to-back and after transmission. This indicates that the chip also has bandwidth limitations toward the lower frequencies. However, a BER below 10^{-3} is generally regarded as the limit correctable by standard FEC circuits. Thus, an error-free transmission $(\mathrm{BER} < 10^{-9})$ of 100 Gb/s at $2^{31} - 1$ can be expected if 7% overhead is used for FEC. The variation between the eight ETDM subchannels was almost identical for

the two different word lengths and ranged from 8.3×10^{-4} to 2.1×10^{-3} for an average BER of 1×10^{-3}.

To compare the results at 107 Gb/s and 100 Gb/s, we remeasured the back-to-back performance using the ETDM receiver chip with an optimized delay between the 90° and 0° delay line. The curve is also plotted in Fig. 10 for a word length of $2^7 - 1$. The back-to-back receiver sensitivity at 100 Gb/s improved to -25 dBm (BER $= 10^{-9}$). This means a penalty of 4.6 dB at a BER of 10^{-9} for 107 Gb/s compared to 100 Gb/s. This penalty is mainly attributed to bandwidth limitations in the ETDM receiver chip.

The experimental results presented in this paper were limited to investigations of the ETDM receiver using low duty-cycle RZ OTDM data signals. However, due to the limited bandwidth of the PDi in the receiver (about 70 GHz), the data pulses at the input of the ETDM receiver will be significantly broadened and more comparable to RZ data signals from standard ETDM transmitters. The results are, therefore, of high relevance to real-system application. First tests using a full ETDM transmitter indicate that the performance will degrade for NRZ signals, but an error-free performance at 100 Gb/s for a short word length $(2^7 - 1)$ can still be expected. We would like to emphasize again that the receiver chip originally was designed for 86 Gb/s, so that an even better performance can be expected after a redesign for 107-Gb/s operation.

IV. Conclusion

The 100-Gb/s Ethernet will be the key enabler for future high-performance and cost-efficient backbone-network architectures. However, the main challenge for 100-Gb/s Ethernet is the development of cost-efficient solutions to decrease the cost per bit and kilometer below that of lower bit-rate systems. This target can only be reached via ultrafast electronic circuits.

We have shown the feasibility of an integrated 100-Gb/s ETDM receiver for optical transmission. The ETDM receiver was tested in optical transmission experiments at data rates of 100 Gb/s and 107 Gb/s. The transmitter was based on OTDM and generated an RZ-OOK data signal with a duty cycle of 13%, which is significantly lower compared to a standard RZ-ETDM transmitter. Error-free performance (BER $< 10^{-9}$) was obtained back-to-back and after transmission over 480 km of DMF for a word length of $2^7 - 1$. At a longer word length of $2^{31} - 1$, a performance degradation is observed. An error-free transmission of 100 Gb/s can still be expected if 7% overhead is used for FEC. The ETDM receiver, which was initially designed for 80-Gb/s operation, comprised the $1:2$ DEMUX and the CDR on a single chip. This is, to the best of our knowledge, the first demonstration of a single-chip ETDM receiver at 107 Gb/s in a transmission experiment. A redesign of the receiver chip is expected to enable an even better performance and operation at even higher bit rates.

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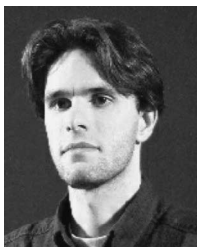

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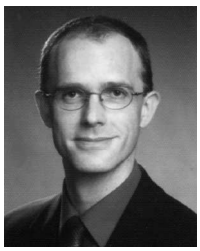

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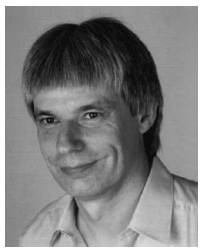

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