FDDI on SONET/SDH Links

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Abstract

This article discusses different possibilities for an interconnection of FDDI-networks over high-speed transmission facilities. A hardware solution for a FDDI to SDH STM-1 repeater is presented implementing the Super-Rate Mapping protocol of ANSI T1.105 in a new, parallel manner. Furthermore, jitter aspects of the designed circuit and possible applications of the repeater are examined.

I. Introduction: Possibilities for Interconnecting FDDI Rings

Interconnecting FDDI-networks between different customer premises has to use public transmission services and facilities. A detailed discussion is given in [1].

- An interconnection over moderate distances using "dark fibers" [2] is sometimes used but obviously quite inflexible. The Single-Mode Fiber Physical Medium Dependent standard of FDDI [3] can be used for this purpose but this tends to be costly as the carrier facilities cannot be shared with other users [1].

- A second method is to connect the FDDI-rings at the data link layer via bridges. Backbone MANs with an adequate transmission capacity are not yet broadly available. Therefore the usage of multiport bridges has been proposed. This method is not further discussed in this paper.

- A third possibility is connecting the FDDI-rings at the physical layer level over high-speed transmission services. This requires a minimum transmission capacity of 125 Mbit/s because of the 4B5B coding scheme used in the physical layer protocol of FDDI for the signalling of linestates, frame delimiters etc. [4]. The Synchronous Transport Module 1 (STM-1), of the Synchronous Digital Hierarchy (SDH) [5], which is equivalent to STS-3c of SONET, offers enough transmission capacity for this purpose. A solution based on the usage of remote repeaters which convert the FDDI physical layer signal with a data rate of 125 Mbit/s into a SDH STM-1 signal with a data rate of 155.52 Mbit/s is shown in figure 1:

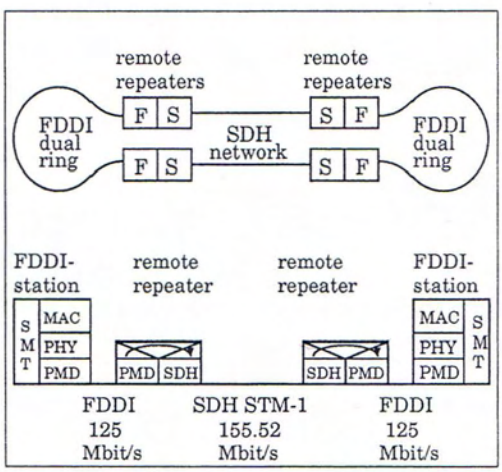

Fig. 1: Topology and Protocol-Structure of an Interconnection at the Physical Layer via Remote Repeaters

The basic problem of the last possibility is how to synchronize an asynchronous FDDI bit stream with the SDH bit stream. This paper presents a novel hardware solution based on a Super-Rate Mapping technique explained in sections III. and IV. In section V. the influence of the jitter generated is discussed. Applications of the designed circuit are given in section VI.

II. Advantages of a Repeater Solution

The proposed, remote repeater solution maps the FDDI physical layer signal into an STM-1 synchronous payload envelope (SPE) so that no changes in the existing FDDI stations are necessary. This method offers all the advantages of a standardized public transmission service, e.g.:

- the opportunity to share the transmission capacity with other applications, e.g. circuit switched ISDN as described in section IV.2.
- a high flexibility in changing the interconnection topology: SDH cross connects allow fast merging and switching of the involved rings as explained in section VI.
- The opportunity to use off-the-shelf SONET/SDH components for the implementation.

Unlike a bridging solution, a physical layer interconnection does not need filtering and routing processes which lower the possible throughput and increase transmission delays.
The SDH link behaves like a part of a normal FDDI station to station link. Therefore a physical layer solution does not require extra circuitry to gather and translate information about the SDH link-status for the FDDI station management.
Last but not least a physical layer connection has obvious advantages if the amount of inter-network traffic is dominant and FDDI-rings with small numbers of stations are connected. The latter is typical for most of todays FDDI networks.

III. Super-Rate Mapping

The 125 Mbit/s FDDI physical layer signal is mapped into an STM-1 synchronous payload envelope (SPE) using the Super-Rate Mapping protocol [6].
The STM-1 signal can be structured into frames containing 9 rows of 270 bytes as shown in figure 2. These frames are repeated every 125 microseconds resulting in a transmission rate of 155.52 Mbit/s.

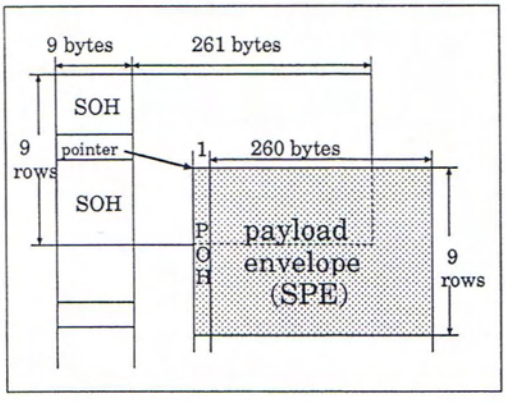

Fig. 2: STM-1 Frame

Each frame comprises a Section Overhead (SOH, nine byte columns) and a SPE which may consist of virtual containers of different sizes. Here only the virtual container VC-4 is considered. The position of the first byte of the SPE within the STM-1 frame is referenced by a pointer located in the SOH.
The SPE consists of one column (nine bytes) of Path Overhead (POH) plus a nine row by 260 column payload structure resulting in a maximum payload rate of 149.76 Mbit/s.
For the Super-Rate Mapping, each row of 260 bytes is partitioned into 20 blocks of 13 bytes each. The detailed structure of the rows, blocks,and bytes is shown in figure 3.
The 15,621 information bits (i) and a part of the nine justification opportunity bits (s) within this structure carry the FDDI physical layer bits. In order to accomodate the asynchronous FDDI payload (125 Mbit/s +/- 50 ppm, equivalent to approx. 15621 +/- 1 bits per SPE) a bit justification mechanism is utilized for stuffing purposes. In each row of the payload structure, five justification control bits (c) are used to control the corresponding justification opportunity bit (s) of that row. If the s bit is used to carry information, the five c bits are set to

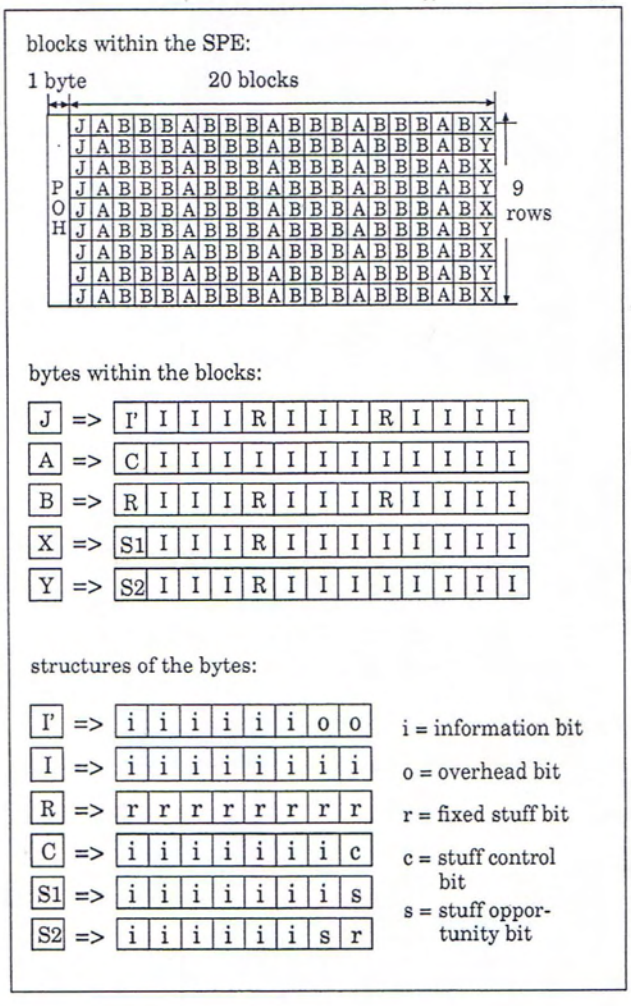

Fig. 3: Super-Rate Mapping

zero. The usage of the s bit as a justification bit is indicated by five c bits set to one (majority vote for protection against bit errors).
The value contained in the s bit when used as a justification bit (no significant FDDI information) is not defined. The overhead bits (o) are reserved for future overhead communications purposes while the remaining r bits are fixed stuff bits that can be used for the transport of additional data channels (especially those contained in the R bytes).

IV. Hardware Design

1. Repeater

On the FDDI side the repeater shown in figure 4 interfaces to the dual ring via the optical signal of the physical medium dependent sublayer. The SDH side uses electrical STM-1 signals and receives a synchronization signal of 2.048 MHz from the SDH network (used for generating the SDH data clock of 155.52 Mbit/s).

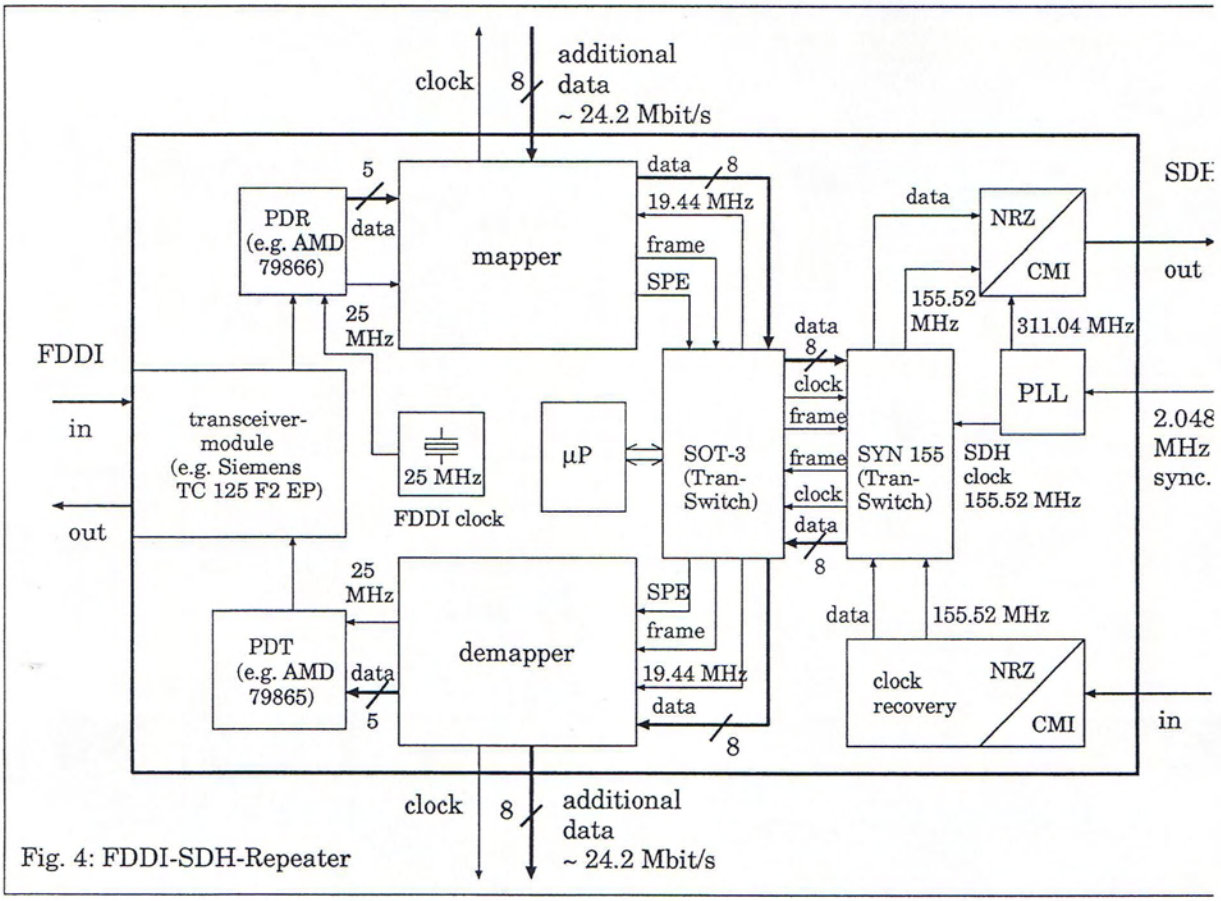

Fig. 4: FDDI-SDH-Repeater

After the FDDI transceiver module, the incoming FDDI bit stream of 125 Mbit/s is transformed by the FDDI Physical Data Receiver to symbols of 5 bit at a symbol clock rate of 25 MHz and fed into the mapper circuit.

This mapper is an especially designed circuit that transforms the FDDI symbols to bytes needed by the SDH components, inserts additional data channels, and performs the above mentioned bit rate adaption. A "frame" and a Synchronous Payload Envelope (SPE) signal are also provided by the mapper to the Synchronous Overhead Terminator SOT-3 controlled by a single-chip-processor. The SOT-3 does the complete SDH overhead and pointer processing and delivers the SDH data bytes containing also path and section overhead, clock and "frame" signals to the synchronizer SYN 155. Here the data is serialized and a byte interleaved parity is calculated. After changing the line code from NRZ to CMI the complete SDH signal is available at the STM-1 electrical interface.

In the opposite direction, the byte-parallel STM-1 payload, the byte clock of 19.44 MHz, and the detected "frame" and SPE signals are fed into the demapper circuit. It extracts the FDDI symbols (5 bits), their clock, and the additional data channels. The FDDI symbols are then transmitted via the Physical Data Transmitter and the transceiver module into the outgoing fiber. SDH clock recovery and NRZ/CMI en-/decoding are done by standard SDH components.

2. Mapper

The mapper shown in figure 5 receives the FDDI symb bit in parallel and the corresponding FDDI symbol cloc MHz. A 19.44 MHz read clock derived from the SDI mission rate is used to read the SDH bytes out of the r A "frame" and SPE signal are also generated marking

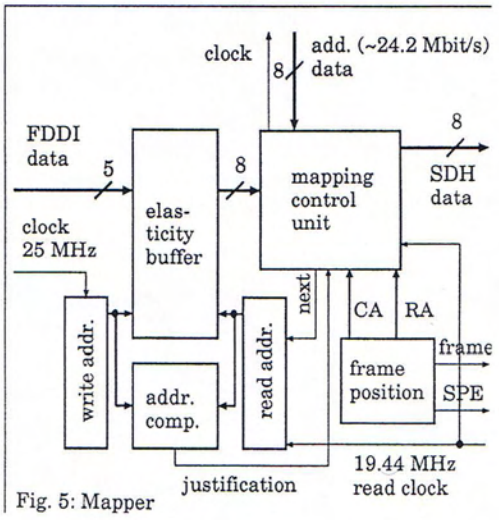

Fig. 5: Mapper

ginning of a new frame and the position of the payload bytes within the STM-1 frame.
The incoming FDDI symbols are written continuously with the FDDI symbol clock rate into an elasticity buffer. It compensates mainly for the periods of POH and SOH during the STM-1 frame when no FDDI information can be transmitted.
The access to the elasticity buffer is controlled by cyclically moving read and write pointers.
According to the position within the SDH frame, the stuffing control requests "fresh" bytes via its "next"-signal from the read control of the elasticity buffer.
This elasticity buffer has to be longer than 80 bits to avoid running empty during the SOH and POH gaps (9 resp. 1 byte each) of the SDH signal. Here a length of 120 bits has been chosen because a structure of blocks consisting of 5 * 8 bits is necessary for the conversion of the five bit FDDI symbols into SDH bytes.
For the fine alignment of the asynchronous FDDI data rate with the SDH signal, a justification signal is derived by comparing the read and write addresses of the elasticity buffer: a slightly increasing FDDI data rate, for example, increases the difference between write and read pointer. In this case the justification signal is set to zero and one or more s bits are not used for the transport of FDDI data.
The position of the current SDH byte with in the STM-1 frame is evaluated by a frame position counter running with the SDH byte clock of 19.44 MHz:
- row (RA) and column (CA) addresses identify the position of the current byte within the payload envelope,
- the signal "frame" markes the beginning of a STM-1 frame,
- and the signal SPE is set to zero during the SOH and POH of the frame.

3. Mapping Control Unit (MCU)

The MCU itself is shown more detailed in figure 6. It requests data bytes from the elasticity buffer depending on the position within the STM-1 frame and is clocked by the SDH byte clock. The necessary informations are supplied by the signals CA, RA, and justification.
Additional information channels e.g. circuit switched ISDN for data, voice or video transmission with a maximum aggregate capacity of 24.192 Mbit/s) can also be multiplexed into the SDH data bytes. This usage of the R bytes of the Super-Rate Mapping thus allows the forming of a hybrid communications system.
The incoming data bytes are written into a so called "assembly buffer" which is 24 bits long. The write pointer is always incremented by eight as the input only consists of significant FDDI data bits. The next position of the read pointer depends on the number of FDDI bits (six, seven, eight, or zero) that are loaded into the current SDH byte corresponding to the Super-Rate Mapping protocol:
An I' byte for example (containing only six significant FDDI bits) causes eight FDDI bits to be read out of the assembly buffer starting at the current position of the read pointer. This pointer then is incremented only by six and the last two bits of

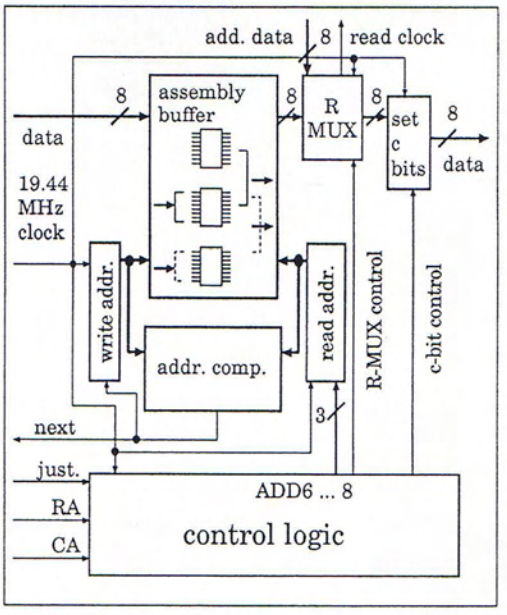

Fig. 6: Mapping Control Unit

the I' byte will thus be read out once again into the next SDH byte. The last two bits of the I' byte are not evaluated in the demapper and can therefore be filled with redundant FDDI information.
An R byte is read out of the assembly buffer without incrementing the read pointer.
In figure 7 the read and write windows of the assembly buffer are represented by eight bit wide brackets that are shifted cyclically around the 24 bits of the buffer.
The position of the read pointer is controlled (via the signals ADD6, ADD7, and ADD8) by a logic block that evaluates the position of the current byte within the STM-1 frame (RA and CA).
This completely parallel implementation of the Super-Rate Mapping protocol through the simple shifting of read and write windows at the assembly buffer prevents clock rates of more than 25 MHz. The whole mapper (and demapper as well) can therefore be build using only low-cost off-the-shelf components (e.g. programmable logic devices).
Depending on the position of the read and write pointers an address comparator arranges the transfer of "fresh" FDDI bytes from the elasticity buffer to the assembly buffer. Additionally it increments the write pointer by one byte.
The justification signal supplied by the address comparator of the elasticity buffer controls the insertion of a significant FDDI bit into the s bit (S1 or S2 bytes in the X resp. Y blocks of the Super-Rate Mapping).
In the case of a significant s bit (i.e. no justification bit in that row) the read pointer of the assembly buffer is incremented by eight (S1 byte) or by seven (S2 byte) instead of seven resp. six when no information is transmitted in the s bit.
The five c bits (in the C bytes of the A blocks) are set by an eight bit register called "set c-bits" at the end of the MCU marking the use of the s bit for justification in that row. In the assembly buffer these c bits had been filled with redundant FDDI bits.

Additional data channels are multiplexed into the positions of the R bytes as mentioned above and a corresponding read clock is generated.

Thus two control paths in the mapper circuit can be identified as shown in figure 7:

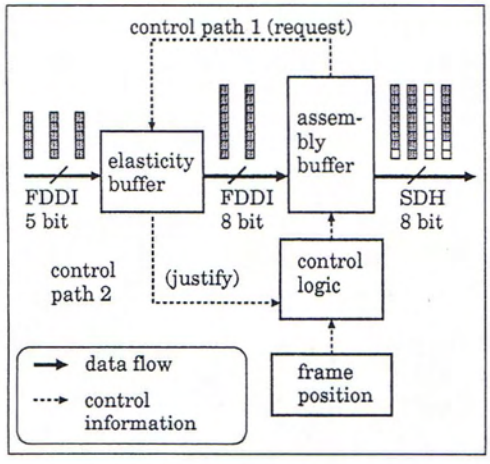

Fig. 7: Control Paths in the Mapper

1) The rough alignment of the FDDI data rate to the SDH data rate corresponding to the Super-Rate Mapping protocol is done in the assembly buffer. This assembly unit itself requests the FDDI data bytes from the elasticity buffer without the need for any higher level control.
2) The fine justification of the independent FDDI and SDH clock sources is done by an outer control loop. It evaluates the number of bits in the elasticity buffer and controls the usage of s bits in the assembly buffer for information transfer.

4. Demapper

Figure 8 shows the demapper circuit in the opposite direction of the repeater. It contains a demapping control unit (DCU) with a structure symmetrical to the mapping control unit. The DCU strips the non-FDDI bits, collects the valid FDDI bits to bytes, and feeds them into a second elasticity buffer where they are converted to five bit FDDI symbols.

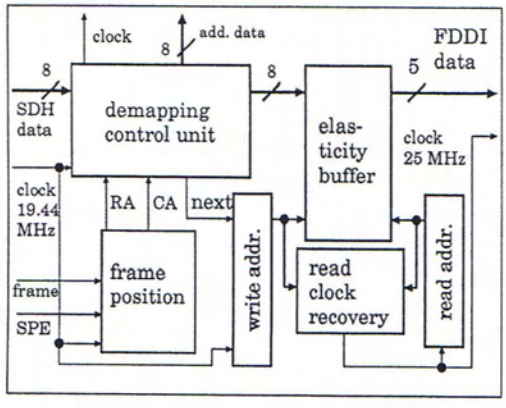

Fig. 8: Demapper

Each time the DCU has extracted and collected eight significant FDDI bits out of the SDH bytes, it activates its "next" signal and the FDDI byte is written into the elasticity buffer. The write pointer of the elasticity buffer always is incremented by one byte.

The FDDI symbol clock (25 MHz) is generated by a voltage controlled oscillator (VCO) whose control voltage is derived from the difference between the read and write pointers of the elasticity buffer:

A reduction of the VCO frequency prevents the elasticity buffer from running empty in the case of a SOH in the received SDH signal.

Therefore the regenerated FDDI clock rate at the output of the demapper equals the FDDI clock rate at the input of the corresponding mapper of the remote FDDI-network.

V. Jitter

The above mentioned control mechanism for regenerating the FDDI clock at the elasticity buffer of the demapper leads inevitably to the generation of jitter within the repeater:

During a SOH gap within the SDH bit stream no FDDI data is being written into the elasticity buffer and the regenerated read clock tends to be somewhat lower than during the SPE parts of the STM-1 frame. When the read clock is accelerating again at the beginning of the next SPE train the transitions of the read clock will be moving compared with the input clock rate of the remote mapper at the site of the other FDDI network.

It can be shown that due to the packet structure of the FDDI protocol only spectral parts of the jitter below ca. 690 Hz are critical:

A FDDI packet has a maximum length of 45000 bits. At a data rate of 125 Mbit/s this corresponds to t_packet = 0.288 milliseconds. During this time a maximum jitter of 0.2 unit intervalls (UI) is tolerated [4], [8].

A sinusoidal jitter with the frequency f_jitter produces the following phase deviation PD (t) over time:

$$PD(t) = 2\,Pi * f\_jitter * t$$

For the maximum tolerable f_jitter_max follows:

$$0.2\ UI = 0.2 * 2\,Pi = 2\,Pi * f\_jitter\_max * t\_packet$$

and:

$$f\_jitter\_max = 0.2 / t\_packet = 694\ Hz.$$

Jitter components below 694 Hz therefore cause no errors in the decision circuit of the subsequent FDDI station.

The control loop consisting of VCO and read/write pointers at the elasticity buffer can be designed to have an upper cut-off frequency in the order of 10 to 100 Hz. Thus the generation of jitter components above f_jitter_max can easily be prevented and the connected FDDI networks won't be disturbed by any kind of jitter produced by the regeneration of the FDDI clock.

VI. Applications

As mentioned in the introduction, the use of SDH Cross Connects (CC) for switching the lines to the involved FDDI rings makes the interconnection of these rings much more flexible. A possible topology is shown in figure 9 where ring 3 can be connected on demand to the three other FDDI-networks. Thus a ring with predominant intra-network traffic may stay undisturbed as long as no need for inter-network communication arises. This results in high performance in terms of throughput and access delay. In the other case a connection of this isolated ring to one or more of the others can quickly be established by merging the relevant rings.

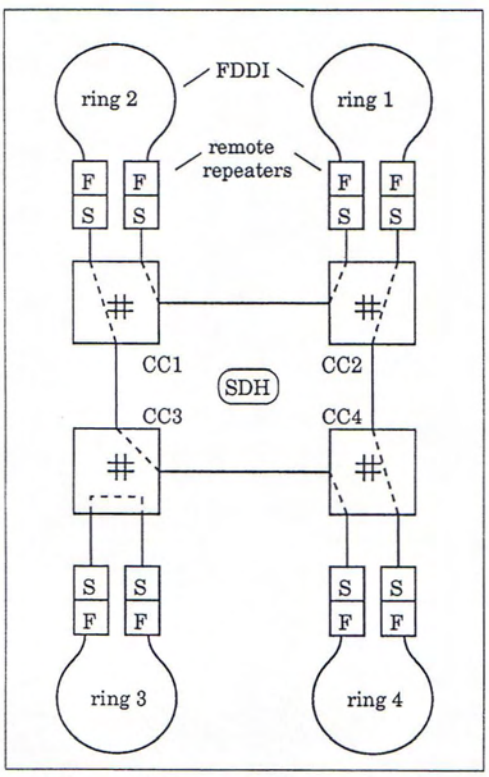

Fig. 9: Flexible Interconnection via SDH Cross Connects (CC)

An important fact in this context is the fast reconfiguration mechanism of FDDI (in the order of 100 milliseconds) which is leading to low down times of the involved rings during and after the switching [7].

In a further step, identical repeaters and the existing topology of SDH-links and cross connects can be used to implement a backbone solution: The only change necessary here is the insertion of FDDI to FDDI bridges at the same points where the FDDI to SDH repeaters were connected to the FDDI rings. The SDH-network with its cross connects is thus converted to a SDH-based FDDI backbone.

Summary:

In order to preserve the excellent performance characteristics of FDDI the usage of high-speed transmission facilities for interconnecting remote FDDI-networks is very important.
In this paper a FDDI to SDH repeater has been proposed using a Super-Rate Mapping technique to adapt the asynchronous FDDI physical layer signal to the SDH STM-1 signal.
Because of a novel parallel implementation of this mapping algorithm the maximum clock rate in the whole circuit is 25 MHz. Therefore only off-the-shelf components are necessary to build the repeater avoiding any specially designed high-speed circuitry.
The described repeater is part of a theoretical design study. We are planning to build a prototype for further evaluation of the proposed concept and design.

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