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# Evaluation of Packet Delay in OBS Edge Nodes

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## ABSTRACT

In OBS networks, packets are aggregated into bursts in the edge nodes and then send through the all-optical network to the destination node. Most of the delay phenomenon (variable delay) occurs in the edge node, which is an important issue for the QoS provisioning. The paper characterizes the packet delay in the edge node, which is mainly determined by the burst assembly, transmission queuing as well as the characteristic of the incoming IP traffic.

**Keywords:** optical transport networks, burst assembly, queuing analysis, performance evaluation

## 1. INTRODUCTION

Optical Burst Switching (OBS) has been proposed as an efficient and flexible switching paradigm for a highly dynamic future optical data plane [1]-[2]. In OBS networks, the dynamics of traffic can be supported by edge nodes, which aggregate traffic and assemble IP packets into variable length optical bursts as well as by core nodes, which asynchronously switch these bursts.

To be suitable for backbone transport networks, several criteria must be fulfilled with respect to service quality. For classical best effort services almost only the loss probability is relevant, which inherently reflects packet loss probabilities. Beyond this, for real time services also the delay and especially the delay jitter must be bounded. According to [3], the delay jitter can be defined as upper bound on the  $1-10^{-3}$  quantile of the difference between maximum and minimum delay. This delay and delay jitter of a packet is influenced in OBS networks directly or even indirectly through the burst delay and delay jitter by functional components in the edge nodes as well as in the core network (e. g., propagation delay, contention resolution mechanisms [4], ... ). In this paper, we limit ourselves to the evaluation and investigation of the delay and especially the delay jitter in the edge node.

During the burst assembly, the packets are collected in the assembly queues and assembled into burst according to the following principles. Basically, either the time is limited between the arrival of the first packet in the assembly queue and the delivery of the corresponding burst (time-out based approach) or the maximum length of the burst is limited (size based approach). Also a combination of both can be applied [5]. It can be easily seen that each packet is delayed by a different time. While the last packet of a burst is only delayed for the processing time of the final burst assembly, the first packet has to be delayed up to the timeout in a timeout based burst assembly or even up to infinitely long in a pure size based assembly.

After assembly, the burst is forwarded to an output queue. In this queue, the burst is buffered until it can be send to the core network. Thus, in this stage the burst is again delayed by a non-deterministic time. Concluding, the buffering in the assembly queues as well as in the output queue lead to an observable delay and delay jitter.

The remainder of this paper is structured as follows: in section 2 we introduce and discuss our model and parameters for evaluation of delays in the ingress edge node. The results of a numerical evaluation are presented in section 3. Finally, section 4 concludes the paper and presents an outlook.

## 2. SYSTEM MODELS AND PARAMETERS

The observed OBS edge node can be represented by the system model illustrated in Fig. 1. IP packets from the client networks are classified according to their traffic class and destination address into different Forwarding Equivalent Class (FEC) and distributed into correspondent assembly queues. Upon the first packet arrival at its empty assembly queue, a timer with timeout period  $\tau$  is activated. Packets are continuously accumulated in the assembly buffer until timeout  $\tau$  occurs or the backlog in the assembly queue is about to exceed the maximal burst size of  $S$ . When either of these two conditions is satisfied, the packets collected in the assembly queue are assembled into an OBS data burst and this is delivered to the FIFO buffer for transmission. As a practical design scheme, a dedicated transmission buffer is generally allocated to each wavelength. As a result, a single wavelength channel is considered in our system model. In our simulation study, we assume that there are totally 30 FECs and the IP packets are evenly distributed to each assembly queue at random. The bursts are assembled with a maximum burst size of 128 Kbytes. Furthermore, the transmission buffer has unbounded size, so no burst loss can occur and the wavelength channel capacity is fixed at 10 Gbps.

For the input traffic, three scenarios are considered, one based on a Poisson process and two based on a long range dependence (LRD) traffic model [6] differing in the user's access rate. For the Poisson scenario, the

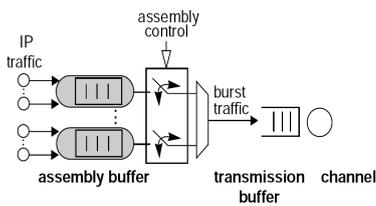


Figure 1

System model of OBS edge node.

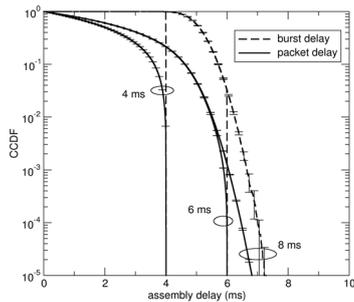


Figure 2a

Impact of timeout on assembly delay

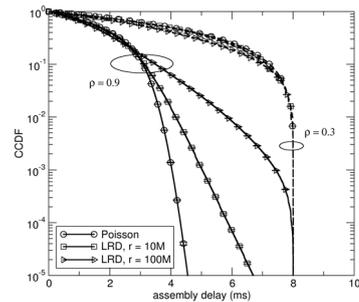


Figure 2b

Impact of load on assembly delay

packet inter-arrival time follows a negative exponential distribution and the packet size distribution is trimodal [7]. For LRD traffic, the M/Pareto model is used [8]. In this model, traffic sessions arrive according to a Poisson process and the session size follows a Pareto distribution. Each session is segmented to a series of IP packets with constant size  $L$  except the last packet of the session. The segmented packets are sent back-to-back with an interval of  $L/r$  where the parameter  $r$  denotes the link rate (in bps) of each individual access connection. In our simulation study, the mean of the Pareto distribution is set to be 10 Kbytes and the shaping parameter is 1.4. For the packet size  $L$ , we use 1000 bytes. Furthermore, access link rates  $r$  of 10 Mbps for the low access rate scenario and 100 Mbps for the high access rate scenario will be looked at. This setting of the M/Pareto model results in the LRD traffic with the Hurst parameter equal to 0.8.

The packet delay distribution in the edge node will be inspected by simulation with respect to the timeout parameter, system load and traffic models. The timeout period  $\tau$  can take the values of 2ms, 4ms, 6ms and 8ms, respectively, with the default value  $\tau = 8$ ms unless stated differently. The system load  $\rho$  ranges from a light load of 20% to a heavy load of 95% with the default value 60% unless stated differently.

### 3. DELAY EVALUATION

The transit delay in the edge node is composed of two parts: assembly delay in the assembly buffer and the queuing delay in the transmission buffer. In the following subsections, we will first investigate both individual delay components separately and then inspect the total transit delay.

It is worth to emphasize that the performance evaluation in this paper is focused on the delay experienced by the individual IP packets, instead of the OBS data burst, since the packet delay is more directly related to the end-to-end QoS provisioning [3]. This makes our work different to the study on the burst assembly delay in [9] and [10], where the assembly delay is defined as the latency between the start of the timer and the activation of the assembly operation. In the Subsection 3.1 the burst assembly delay and packet assembly delay will also be briefly compared to illuminate the difference.

#### 3.1 Assembly delay

The assembly delay with respect to bursts and packets in terms of the Complementary Cumulative Distribution Function (CCDF) is plotted in Fig. 2a for the Poisson scenario with a system load of 60% and for different assembly timeout  $\tau$ . It can be noted that the tail distribution of the packet assembly delay is up to one order of magnitude below the burst assembly delay. This is natural because the burst assembly delay is actually the maximal assembly delay for the packets composing that burst. This indicates that the burst assembly delay is a more conservative performance metric in the delay evaluation. Nevertheless, the evolution of the curves is similar for both packet and burst assembly delay. The timeout period  $\tau$  serves as a cutting bound for the assembly delay. In the cases of the enlarged  $\tau$ , the CCDF curve looks like a natural extension of the CCDF curve of the small  $\tau$ . Similar behaviors can be also observed under the M/Pareto traffic model, so they are not shown here. In the following, we will concentrate the attention solely on the packet delay.

In Fig. 2b, the influence of the system load on the assembly delay is plotted for fixed timeout period  $\tau$  of 8ms for different traffic scenarios. In general, it can be seen that the increase of the system load can bring a significant improvement in the delay performance. At light system load of 30% the CCDF curves look very much the same for all three scenarios due to the bounding of the timeout period. At heavy traffic load of 90% the LRD traffic leads to a “heavier” tailed delay CCDF than the Poisson traffic. This is because the burstiness of the LRD traffic causes larger variance in the assembly duration, which results in a wider bandwidth of the correspondent probability density function. Likewise, as a higher access link rate  $r$  leads to more variability in the aggregated traffic, a worse assembly delay can be expected as shown in the figure.

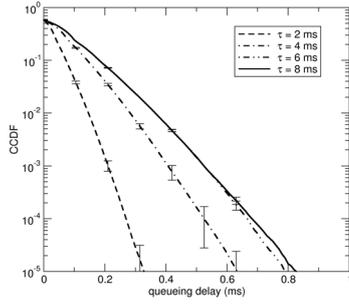


Figure 3a

Impact of timeout on queuing delay

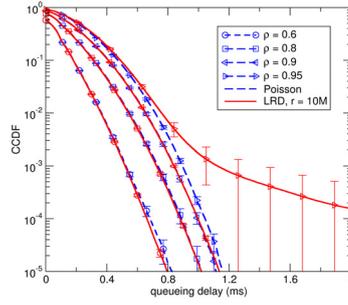


Figure 3b

Impact of load on queuing delay  
Low access rate

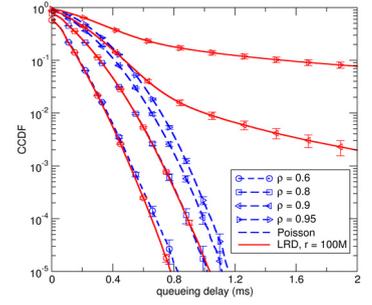


Figure 3c

Impact of load on queuing delay  
High access rate

### 3.2 Queuing delay

Analogous to the study on the assembly delay, the queuing delay will be evaluated with respect to the timeout period and system load respectively. In Fig. 3a, the CCDF is shown for the scenarios for different  $\tau$  at a fixed system load of 60%. As a representative case, only the results for the Poisson arrival process are presented. It is clear that the queuing delay increases with the increased timeout period ( $\tau = 2 \sim 6$  ms) and then converges to a constant level ( $\tau \geq 6$  ms). A closer investigation discovers that the resulting mean burst size equals to 50.4 Kbytes, 100.4 Kbytes, 127.3 Kbytes and 127.5 Kbytes for  $\tau = 2$  ms, 4ms, 6 ms, and 8 ms, respectively. This implies that the increase in the queuing delay is due to the larger resulting burst size from larger values of  $\tau$ . However, when  $\tau$  is so large such that the burst size bounds is always reached, the timeout period has no more influence on the queuing delay any more. Then in this parameter area, only the system load is relevant for the queuing delay.

In Fig. 3b and 3c, the queuing delay CCDF is shown for LRD traffic scenarios in comparison to the results of the Poisson arrival process for a fixed timeout of 8ms. It is interesting to see that at low and medium system load, the queuing delay is quite similar irrespective of the traffic model or the access link rate. Only in the heavy load case, degradation in the queuing performance turns up in the LRD models. This conforms to the study in [11] showing that LRD is only relevant for queuing performance at high system load. While for a access rate of 10Mbps the tail behavior is still amenable up to the load of 90%, it begins to go wild at in the case of a access rate of 100Mbps. Again, a high access link rate imposes a prominent negative effect.

A general observation from Fig. 3 is that the queuing delay is minor in comparison to the assembly delay shown in Subsection 3.1, as long as the system load is not extremely high.

### 3.3 Transit delay

In this subsection, the total packet delay in the edge node is evaluated. In Fig. 4a and 4b, the transit delay comparison between LRD traffic and Poisson traffic is illustrated at light, medium and heavy load. It can be observed that in most cases, the transit delay behavior is quite similar to the assembly delay as depicted in Fig. 2b, except that the transit delay is a bit larger than the assembly delay under the same system setting. Especially noticeable is the case of LRD traffic with low access rate and  $\rho = 0.95$  in which a heavy tail occurs in the queuing delay (Fig. 3b). In spite of the large queuing delay, the transit delay is still dominated by the assembly delay. Only in the case of LRD traffic with high access rate and  $\rho = 0.95$  the curve of the transit delay deviates from the assembly delay and possesses a heavy tail resulted from the queuing delay.

Connecting the delay distribution to the QoS parameter, we define the  $1-10^{-5}$  quantile of the transit delay as the delay jitter and illustrate it in Fig. 4c with respect to system load and timeout period. With Poisson arrival, the jitter slowly increases with the load first and then decreases. This is because the at light system load, the timeout period dominates the assembly delay. So, the jitter contributed by the assembly delay keeps equal to  $\tau$  while the relative small contribution of the queuing delay increases with the load. At high system load, the assembly delay is significantly reduced with high traffic rate, which exceeds the increase in the queuing delay. Therefore, the jitter sinks with the further increase of the load. For the LRD traffic with  $r = 10$  Mbps, there is a similar jitter behavior. When the access link rate is 100 Mbps, the jitter continuously increases with the load due to the slow decrease of the assembly delay with the load, as noticeable in Fig. 2b. At extremely high system loads, the heavy tailed queuing delay pushes the jitter of the transit time to an explosion.

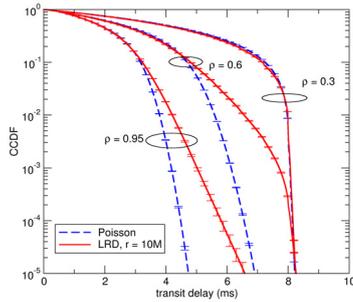


Figure 4a  
Impact of load on transit delay  
Low access rate

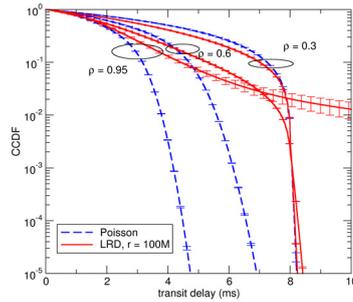


Figure 4b  
Impact of load on transit delay  
High access rate

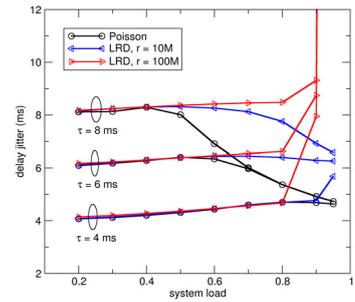


Figure 4c  
Delay jitter in the edge node

#### 4. CONCLUSIONS

In this paper, we presented a performance evaluation of the delay and delay jitter in OBS edge nodes focusing on the packet level. We investigated the system by simulation for different traffic models and load situations. We have shown that only for low load the timeout parameter serves as the upper bound of the assembly duration and thus impacts on the burst size. Under this situation, a small burst size leads to a small queuing delay. For high loads, the timeout parameter impacts neither on the assembly delay nor on the queuing delay. We have also shown that irrespective of the traffic model the queuing delay is very small even for very high load situations. The detrimental queuing behavior for LRD traffic only appears for extreme high system load. So, the transit delay is dominated in most cases by the assembly delay and only for high load situations and very bursty traffic, the impact of the queuing delay grows into considerable ranges. Furthermore, as long as the maximum load is controlled the delay jitter in the edge node is approximately bounded by the assembly timeout. Future work will extend this analysis to the impact of the core network. In the optical core, the data bursts are delayed during their transmission by the propagation delay, which is the same for all burst transmitted between an edge node pair as long as they are transmitted through the same path. Also concepts applied for contention resolution can introduce some additional delay and delay jitter, especially buffering bursts in Fiber Delay Lines (FDL) and deflection routing.

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